SUMMER 2013 - INTERNSHIP PROGRAM
Semiconductor Processing and Characterization Techniques - Lecture

TIMES and LOCATION:

Lecture

July 15 – Aug. 2rd 9:00-11:30; M, Tu, W, Th and F 331 Klamath Hall

INSTRUCTOR: Prof. Shannon Boettcher, email: swb@uoregon.edu,
office: Lewis Integrated Science Rm. 435, Phone: 541-346-2543

Prof. Boettcher is best contacted outside of class via email or by appointment.

TEXTBOOK: **(1)** Silicon Processing for the VLSI Era, Volume 1: Process Technology, Stanley Wolf, and Richard N. Tauber, Lattice Press, **(2)** Semiconductor Devices, Physics and Technology 3rd Ed., S.M. Sze.

GOAL: Introduce fundamentals of integrated circuit fabrication, including epitaxy, thin film deposition, oxidation, impurity diffusion and implantation, lithography, etching, chemical mechanical polishing, and analytical techniques employed in semiconductor-process development and monitoring.

This course will closely follow Semiconductor Processing and Characterization Techniques Laboratory (taught by Dr. Fuding Lin). Process meetings will be held to discuss progress and problems in the laboratory section and their relation to the lecture component at 8:00 am each day in the same room. Grading will be separate for the two courses.

PROBLEM ASSIGNMENTS:

2-3 problems will be assigned most days during the week. Neatness and clarity on your assignments is important, otherwise they are difficult to grade. Indicate your final answers (with units!!) with a box around them.

LECTURE COURSE GRADING:

CVD Virtual Lab - 10 %
DOE and SPC Report - 10%
Problem Sets - 10 %
Midterm Exam - 25%
Final Exam - 45%