CLOSE-SPACED VAPOR TRANSPORT AND PHOTOELECTROCHEMISTRY OF GALLIUM ARSENIDE FOR PHOTOVOLTAIC APPLICATIONS

by

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DISSERTATION ABSTRACT

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Doctor of Philosophy

Department of Chemistry and Biochemistry

March 2015

Title: Close-Spaced Vapor Transport and Photoelectrochemistry of Gallium Arsenide for Photovoltaic Applications

The high balance-of-system costs of photovoltaic installations indicate that reductions in absorber cost alone are likely insufficient for photovoltaic electricity to reach grid parity unless energy conversion efficiency is also increased. Technologies which both yield high-efficiency cells (>25%) and maintain low costs are needed. GaAs and related III–V semiconductors are used in the highest-efficiency single- and multi-junction photovoltaics, but the technology is too expensive for non-concentrated terrestrial applications. This is due in part to the limited scalability of traditional syntheses, which rely on expensive reactors and employ toxic and pyrophoric gas-phase precursors such as arsine and trimethyl gallium. This work describes GaAs films made by close-spaced vapor transport, a potentially scalable technique which is carried out at atmospheric pressure and requires only bulk GaAs, water vapor, and a temperature gradient to deposit crystalline films with similar electronic properties to GaAs prepared using traditional syntheses.

Although close-spaced vapor transport of GaAs was first developed in 1963, there were few examples of GaAs photovoltaic devices made using this method in the literature

at the onset of this project. Furthermore, it was unclear whether close-spaced vapor transport could produce GaAs films appropriate for use in photovoltaics. The goal of this project was to create and study GaAs devices made using close-spaced vapor transport and determine whether the technique could be used for production of grid-connected GaAs photovoltaics. In Chapter I the design of the vapor transport reactor, the chemistry of crystal growth, and optoelectronic characterization techniques are discussed. Chapter II focuses on compositional measurements, doping, and improved electronic quality in CSVT GaAs. Chapter III describes several aspects of the interplay between structure and electronic properties of photoelectrochemical devices. Chapter IV addresses heteroepitaxial growth of GaAs on “virtual” Ge-on-Si substrates. This is a topic of importance for the broader III-V community as well as the photovoltaic community, as Si is the substrate of choice in many areas of industry.

This dissertation includes unpublished and previously published co-authored material.

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Dedicated to my family and friends.

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CHAPTER I

CLOSE-SPACED VAPOR TRANSPORT OF GALLIUM ARSENIDE

Portions of this chapter were previously published as Ritenour, A. J.; Cramer, R. C.; Levinrad, S.; Boettcher, S. W. "Efficient n-GaAs Photoelectrodes Grown by Close-Spaced Vapor Transport from a Solid Source." ACS Applied Material Interfaces 2012, 4, 69-73. A. J. R. wrote the paper, made the samples, performed the experimental work, and made the figures. R. C. C. and S. L. assisted with building the close-spaced vapor transport system. S. W. B. provided editorial assistance and was the principal investigator.

Introduction

The excellent optoelectronic properties of gallium arsenide (GaAs) make it an attractive material for solar energy conversion.[1,2] It has a high optical absorption coefficient, absorbing >92% of above band gap (E_g) photons within 1 μm of film thickness (Figure 1.1).[3] It has an ideal direct bandgap $E_g = 1.42$ eV for solar energy conversion which can also be tuned by alloying (*e.g.* with Al or P) for multijunction photovoltaic (PV) or photoelectrochemical (PEC) applications.[4] Indeed, GaAs is used to make the most efficient singlejunction PV known, with recent champion cells achieving 28.8% efficiency under standard one-sun test conditions.[5] Unfortunately, the scalability of GaAs photovoltaics is limited by the high cost of metal-organic chemical vapor deposition (MOCVD), which employs toxic and pyrophoric gas-phase precursors.[2] Low-cost routes to high-quality GaAs are needed.

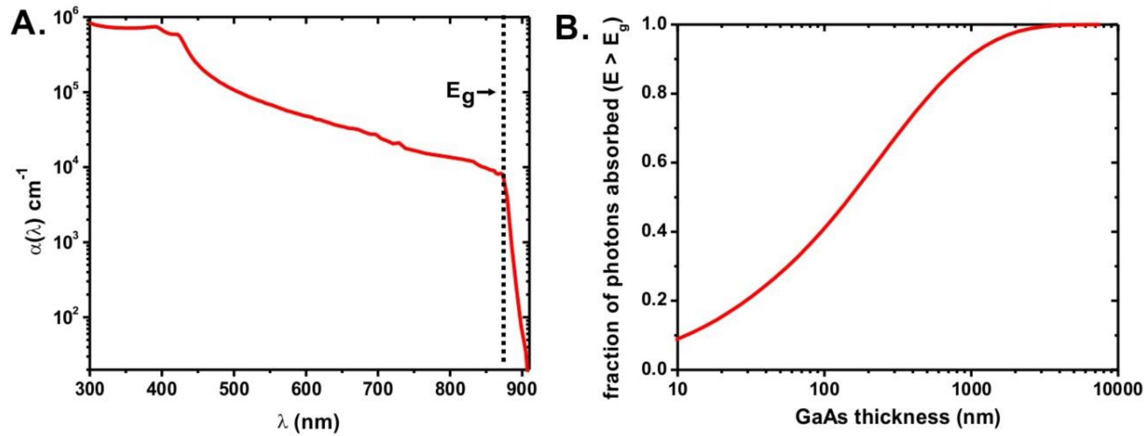
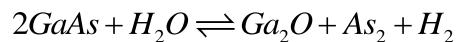


Figure 1.1. (A) The wavelength dependent absorption coefficient of GaAs showing the position of E_g. (**B)** The attenuation of E > E_g AM1.5 photons passing through GaAs as a function of thickness.

Close-space vapor transport (CSVT) is an alternative technique for depositing GaAs that uses bulk GaAs as the only precursor.[6] The use of a solid precursor circumvents challenges associated with the handling of toxic and pyrophoric gas-phase starting materials. The CSVT reactor consists of a bulk GaAs source and a planar substrate sandwiched between graphite blocks and separated by a thin quartz spacer. The entire assembly is enclosed in a quartz tube. The source is heated in a reducing atmosphere (hydrogen or forming gas) containing water vapor as a transport agent. The water reacts with the GaAs source to produce the volatile species as shown:[7-9]



$$2GaAs + H_2O \rightleftharpoons Ga_2O + As_2 + H_2$$

The temperature gradient between the heated GaAs source and the cooler substrate provides a driving force for vapor transport of GaAs. Diffusion of the gas-phase reactants through the temperature gradient results in supersaturation at the cooler substrate surface, causing As_2, Ga_2O, and H_2 to decompose into GaAs and H_2O. The process is carried out

at atmospheric pressure, which allows for growth rates up to 1 μm min^{-1} with ca. 95% yield.[6] The overall deposition process and apparatus are similar to the vapor-transport process used commercially for the high-throughput/low-cost growth of CdTe thin-film photovoltaics.[10,11] CSVT is therefore a potentially scalable cost-effective route to GaAs thin films.[12-15] A schematic of the process is shown in Figure 1.2.

Despite the potential advantages of CSVT, its use for optoelectronic devices remains limited. Since its initial development in 1963, epitaxial films of GaAs have been grown by CSVT on GaAs, Ge, and Si.[6,16] Electrical properties of these films such as dopant density ($N_D = 1 \times 10^{16}$ to 1×10^{17} cm^{-3}), mobility (μ_e = 3000−4200 cm^2 V^{-1} s^{-1}), and photoluminescence (PL) intensity have been measured and indicate that CSVT GaAs films may be suitable for solar-energy conversion.[17−19] However, the only reported PV device fabricated using CSVT GaAs was that of Mauk and co-workers; an Au-GaAs-on-Si Schottky barrier PV which yielded a short-circuit current density of 7 mA cm^{-2} under one sun of solar simulation (no open-circuit-voltage or efficiency was reported).[20] A key question is whether or not it is possible to achieve sufficient performance using CSVT GaAs to motivate the further development of more complicated device architectures.[16,17] To evaluate this possibility, we grew n-GaAs thin films with varying concentration of

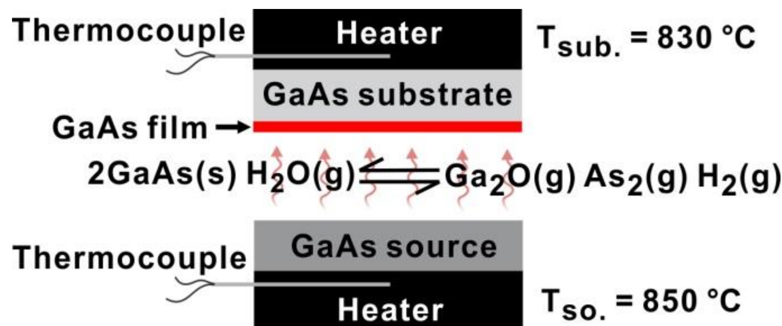


Figure 1.2. Detail of key parts of the CSVT reactor and GaAs transport chemistry.

water vapor, [H_2O], and measured their PEC energy conversion properties. The PEC characterization approach enabled measurement of standard PV device parameters including short-circuit current density (J_{SC}), spectral response, open-circuit voltage (V_{OC}), fill-factor (*ff*), and power conversion efficiency (η), without the need to fabricate solid-state p-n junctions, top contact grids, or address other device-related engineering issues (Figure 1.3).

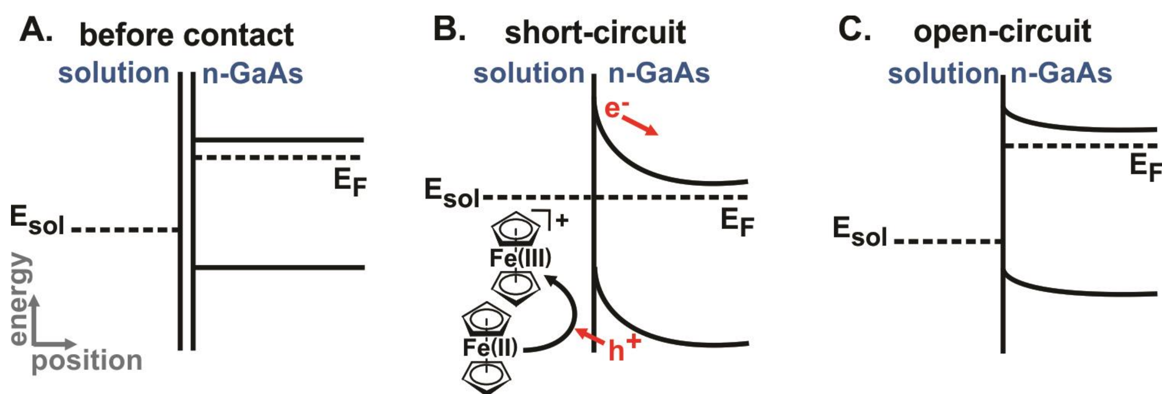


Figure 1.3. Band-bending diagrams for the n-GaAs PEC system with ferrocene/ferrocenium electrolyte (A) before contact (B) in short-circuit operation and (C) open-circuit operation. The rectifying solution contact enables a range of semiconductor characterization measurements.

Methods

CSVT Reactor Design

The reactor was operated in a 2” quartz tube. The tube was equipped with vacuum feed-throughs for thermocouples and resistive heater power. Proportional integral differential (PID) units were used to control current being passed through machined graphite coils which served as heaters (Figure 1.4). Step-down transformers were used to lower the AC line voltage to 10 V. The temperatures of the source and substrate were

monitored by type K thermocouples embedded inside graphite blocks directly above and below the source and substrate, respectively. The source and substrate wafers were physically separated by a quartz ring 0.7 mm in thickness with an 11 mm interior diameter. Control of water vapor concentration in the reactor was accomplished by combining a stream of hydrogen that was flowed through a temperature-controlled bubbler containing saturated aqueous NaCl solution (functional temperature range -15 °C to 20 °C) with a stream of dry hydrogen. Thus water vapor concentration was decreased by a combination of lowering the bubbler temperature and increasing the flow rate of dry hydrogen relative to wet hydrogen. This system allowed humidity control over three orders of magnitude.

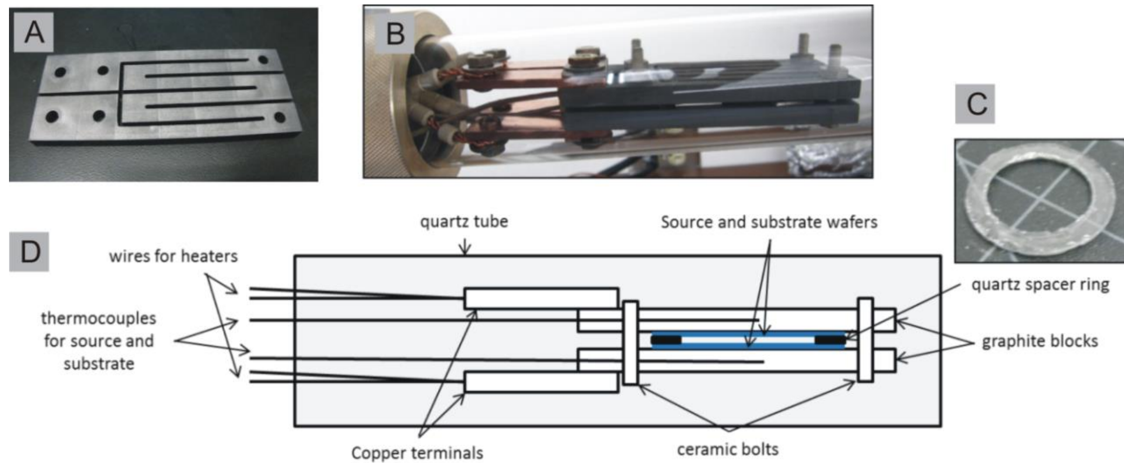


Figure 1.4. (A) Photo of a heater machined from pyrolitic graphite. (B) Photo of the CSVT reactor assembled and placed in quartz tube. (C) Photo of quartz spacer ring. (D) Diagram of the CSVT reactor.

GaAs Wafer Preparation

All GaAs wafers were obtained from Wafer Technology Ltd. (United Kingdom). The source (moderately doped *n*-GaAs) and substrate (highly doped n^+-GaAs) were cut to 12 mm squares and thoroughly cleaned before growth. The cleaning process consisted of;

(1) isopropanol rinse, (2) blow dry with nitrogen, (3) 1 minute dip in concentrated HCl, (4) rinse with deionized water, and (5) blow dry with nitrogen. After each cleaning the wafers were inspected to ensure the surfaces were free of dust and debris. The same source wafer and a different substrate wafer were used for each deposition. A superior cleaning procedure was developed for later studies: (1) 1 min dilute basic piranha etch (50:1:0.1 water, ammonium hydroxide, H_2O_2); (2) rinse with deionized water, (3) rinse with HPLC-grade isopropyl alcohol, and (4) spin dry (3000 rpm) on a vacuum chuck.

Film Deposition

Before heating, the system was evacuated to ca. 16 mTorr and purged with hydrogen with the desired water vapor concentration, [H_2O]. At least two reactor volumes of hydrogen were passed before turning on the heaters. During growth the total hydrogen flow rate was maintained between 820 and 1,400 sccm, depending on [H_2O]. During the heating ramp the substrate was kept slightly warmer than the source wafer to prevent spurious deposition. After reaching the desired temperature range the gradient was reversed to initiate film growth. After growth, the temperature gradient was then reversed and the system was cooled and purged with nitrogen for 30 min. The vacuum system's leak rate was approximately 2 mTorr s^{-1}. The film thicknesses were measured using a Zygo 7300 3D optical profilometer.

X-Ray Diffraction Analysis

Epitaxial growth on the [100] GaAs substrate was confirmed by x-ray diffraction (XRD) analysis using a Philips Panalytical diffractometer. The beam was aligned with the substrate planes by setting 2θ to the Bragg condition for the [400] reflection and rocking the stage angle (ω) to find the maximum intensity. All samples showed only a single

sharp peak for the rocking curve, indicating the film was oriented with the substrate. Following alignment to the [400] planes, a scan of 2θ revealed only GaAs peaks in the [100] family of planes, indicating that the GaAs film was aligned with the [100] GaAs substrate (Figure 1.5). 2θ-ω scans over the [400] reflection yielded the same peak shape for the CSVT films and the substrate.

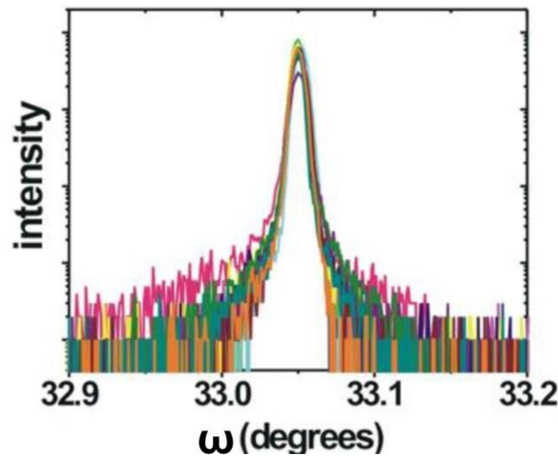


Figure 1.5. ω scans (rocking curves) of the GaAs [400] reflection showing the same line shape for GaAs films and the bare substrate. The full width at half max (FWHM) is ~0.01° or ~30 arcsec for all samples. Note that the y-axis is a log scale.

Scanning Electron Microscopy

Cross-sectional scanning electron microscopy (SEM, ZEISS Ultra-55) of the GaAs films was used to investigate surface morphology of the CSVT films (Figure 1.6). Plan-view and cross-sectional imaging revealed a largely smooth surface with minor inhomogeneities. These inhomogeneities were present in all CSVT samples and did not appear to correlate to any trends observed in the photoanode performance or in the optical reflectance.

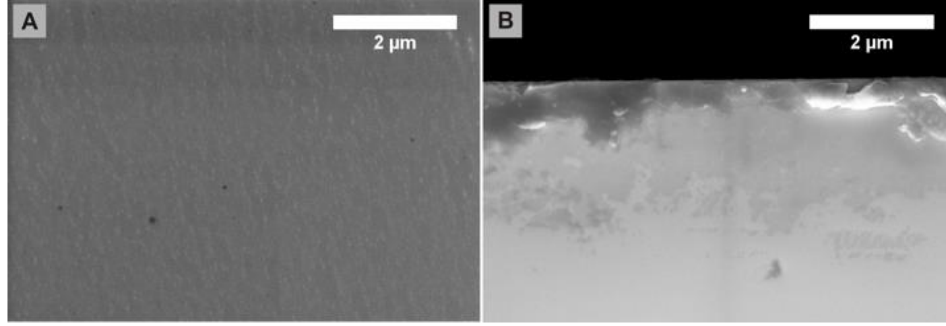


Figure 1.6. (A) Plan-view SEM image of CSVT GaAs film grown in 1,700 ppm water vapor. (B) Cross-sectional SEM image of the same CSVT GaAs film.

Reflectance Measurements

The reflectance of each GaAs sample was measured in air using an integrating sphere attachment on a Perkin Elmer Lambda-1050 UV/Vis/NIR spectrophotometer. The CSVT GaAs samples were smaller than the instrument's sample window opening, so a mask with a smaller opening was used. The mask was a 1.6-mm-thick sheet of polished aluminum with a beveled hole 2 mm in diameter. In order to account for the reflectance of the mask, we measured the current on the integrated photodetector with respect to wavelength under three different setups: (1) the mask with the hole covered by a GaAs sample, (2) the mask with a piece of silicon (taken to represent the known reflectance of silicon), and (3) the mask alone with an uncovered hole (taken to represent 0% reflectance). We then calculated the reflectance of the GaAs using

$$R_{GaAs} = \frac{I_{mask,GaAs} - I_{mask,0\%}}{I_{mask,Si} - I_{mask,0\%}} R_{Si}$$

where $I_{mask,GaAs}$, $I_{mask,Si}$, and $I_{mask,0\%}$ represent the signal (in mA) recorded by the detector for setups (1), (2), and (3) respectively. As a control experiment, a piece of commercial GaAs that was large enough to fill the sample window was measured. We determined that both measurements matched the known reflectance of GaAs. Slight variations from 850-

900 nm in sample measurements with the mask were also present in commercial n-GaAs wafers when using the mask and can be attributed to poor signal-to-noise. These variations were absent when measuring commercial *n*-GaAs wafers without the mask.

Electrode Fabrication

Ohmic contacts were fabricated by evaporating 20 nm of AuGe alloy (88:12) on the back of the GaAs wafers followed by a thermal anneal in a forming gas atmosphere at 450 °C for 90 s. A thin wire (0.6 mm diameter) was used to mask a portion of the wafer (11 mm wide squares) so that the ohmic contact could be tested. Probes contacting the gold film on both sides of the masked line were used to measure current-voltage curves to estimate the contact resistance (Figure 1.7). Contact resistance to both n-GaAs and n^+-GaAs wafers were < 3 Ω for contacts ~0.03 cm^2 in size. This corresponds to a negligible potential drop of ca. 2 mV at the highest current measured from an electrode in this study.

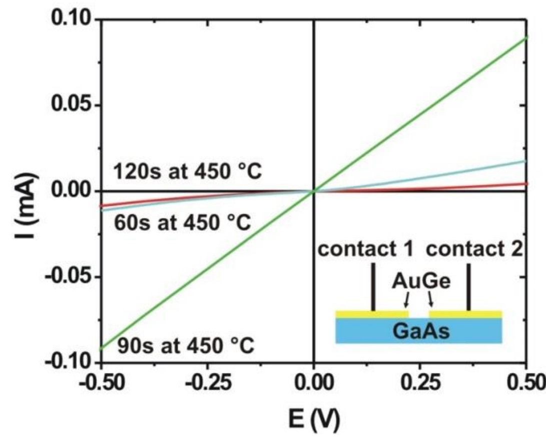


Figure 1.7. (A) Current-voltage (I-V) response of AuGe ohmic contacts to n-GaAs. The anneal duration affects contact resistance of the film. A 90 s anneal was found to be optimal in this case.

The wafers with ohmic contacts were cut into ca. 0.1 cm^2 pieces and electrically contacted by attaching a flattened tinned-copper wire to the back side with silver paint.

The wire was threaded through a glass tube (0.25” diameter) and the back and sides of the wafer were bonded to the tube with epoxy. After curing, an area 0.3 – 0.5 cm^2 on the front of the wafer was defined using a second coat of epoxy, which was then cured (Figure 1.8). The area of the electrode was measured by scanning images of the electrode faces into a computer and measuring the area versus a standard using the ImageJ analysis package.

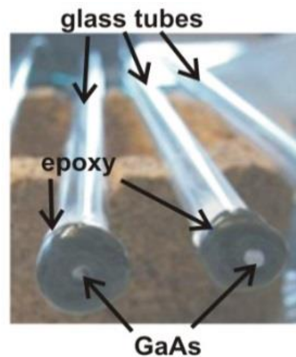


Figure 1.8. Photograph of finished electrodes with defined area of GaAs exposed.

Measurement of Photoelectrochemical J-E Curves

A 300 W Sylvania ELH bulb provided 100 mW cm^{-2} of illumination for the PEC measurements. Although there is some spectral mismatch between ELH and AM1.5 spectra, it was used in this case to compare with previous work on GaAs photoelectrodes and due to its small size which facilitates use inside an inert atmosphere glove-box. The light intensity was calibrated in air using a pyrometer (Thor Labs) by first finding the separation from the ELH source that gave 100 mW cm^{-2} and then replacing the pyrometer with a small photodiode (OSI optoelectronics UV005) which was bonded to the end of a glass tube with epoxy as was done with the photoelectrode samples. The photocurrent measured from the diode under 100 mW cm^{-2} ELH illumination (as measured by the

pyrometer) was 1.80 mA. Placing the photodiode in the glass electrochemical cell reduced the current to 1.72 mA. Filling the cell with electrolyte further reduced the photocurrent to 1.56 mA due to parasitic absorption of the colored electrolyte (Figure 1.9). Before measuring GaAs electrodes, the photodiode was always placed in the cell and the lamp adjusted until this value (1.56 mA) was reached. Thus the stated 100 mW cm^{-2} of illumination includes photons that are absorbed in the solution and/or reflected by the air-glass interface of the cell and correction for these factors would increase the measured efficiencies.

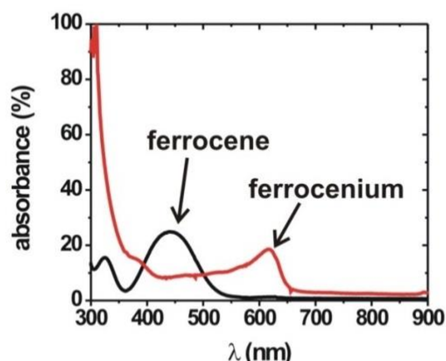


Figure 1.9. UV-Vis absorption spectra for ferrocene (10 mM) and ferrocenium (3.6 mM) in a 1 cm path length cell. Note that these concentrations/path-lengths differ from those in the actual electrochemical cell.

Before measurement, finished electrodes were dipped in concentrated HCl for 5 seconds to etch the native oxide. This etching procedure was determined to yield the best PEC performance. Two additional etching procedures for the GaAs were tested; 5% Br_2 in methanol, and 1:8:40 sulfuric acid:hydrogen peroxide:water (dilute piranha). HCl etching described above resulted in the highest energy conversion efficiencies. We were also concerned that the control wafers might have lower performance due to surface

damage from the polishing process. However, etching 130 nm from an *n*-GaAs control electrode using dilute piranha did not improve its performance, nor did etching the electrode with dilute piranha followed by dipping it in HCl.

Following etching, electrodes were immediately transferred to a nitrogen-filled glove box (< 0.5 ppm O_2 and < 0.1 ppm H_2O) and immersed in electrolyte. The electrolyte consisted of 1.0 M $LiClO_4$ (Sigma-Aldrich, battery-grade, used as received from a sealed glass ampoule opened in the glove box), 0.1 M ferrocene (Fc, Sigma-Aldrich), and 0.5 mM ferrocenium dissolved in acetonitrile (henceforth, Fc/Fc^+/ACN). The ACN was obtained from a solvent purification system and stored on freshly activated 3 Å molecular sieves. The Fc was sublimed at 60 ºC under vacuum. The Fc^+ was chemically oxidized using HBF_4 and bezoquinone from sublimed Fc, recrystallized in tetrahydrofuran, and dried under vacuum.

Measurements were performed in a three-electrode cell. The GaAs sample was the working electrode (WE), a Pt mesh the counter electrode (CE), and a Pt wire positioned near the sample the reference electrode (RE). The WE was illuminated from the bottom by reflecting the ELH light with a 45° angle mirror. The tabulated data collected from all 18 electrodes is given in Table S1. Values of J_{SC} calculated by convolution of the spectral responsivity with the spectral irradiance of two light sources (ELH and AM1.5) are also included for reference. Care was taken to bring the reference electrode as near as possible to the working electrode without blocking any incident light. The working electrode was held about 1 mm from the bottom of the cell. This was found to give the highest energy conversion efficiency as moving the electrode away from the bottom improved mass transport but caused more light to be absorbed by the solution.

The stir bar was stirred with the aid of a magnet epoxied to the rotating shaft of a miniature electric motor, which was driven by a variable DC power supply. The use of this miniature stirring device simplified optimization of the stirring without blocking the light path.

Correcting Mass Transport Overpotential Losses of J-E Data

The corrected *J*-E curves were produced by calculating the corrected potential (E_{corr}) and re-plotting as J vs. E_{corr}. E_{corr} was calculated by subtracting the ohmic losses and concentration overpotential (η_{conc}) from each data point on the curve, as shown:

$$E_{corr} = E - \eta_{conc} - IR$$

Where E_{corr} is the corrected potential, I is the current, R is the resistance determined using Ohm's law by finding the slope of a *J*-E curve of a planar Pt electrode and correcting for η_{conc}. η_{conc} was determined from the limiting currents measured on a planar Pt electrode (similar in shape, construction, and dimensions to those in Figure 1.8) using

$$\eta_{conc} = \frac{RT}{nF}\left\{\ln\left(\frac{J_{l,a}}{-J_{l,c}}\right) - \ln\left(\frac{J_{l,a} - J}{J - J_{l,c}}\right)\right\}$$

where J is the current density at the semiconductor electrode and $J_{l,a}$ and $J_{l,c}$ are the mass-transport-limited anodic and cathodic current densities, respectively.[2]

Mott-Schottky Capacitance-Voltage Analysis

Capacitance-voltage (Mott-Schottky) measurements were carried out in the dark in the same cell with the same electrolyte as described for the *J-E* measurements. The total impedance and phase angle of the semiconductor-electrolyte interface was measured as a function of the working electrode potential and frequency of the AC bias (10 mV amplitude). Data from electrodes that yielded linear Bode plots and phase angles near -90° over several decades in frequency (such as shown in Figure 1.16) were fit to an

equivalent circuit. This was done in order to extract the depletion region capacitance as a function of working electrode bias. The capacitance-voltage data was then analyzed using the Mott-Schottky equation to extract the dopant density. The Mott-Schottky equation is given by

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V_{app} - kT/q\right)}{q\varepsilon N_D A^2}$$

where V_{app} is the electrode potential relative to the solution potential, V_{bi} is the built in potential, A is the electrode area, and ε is the static dielectric constant of GaAs. k, T, and q have the usual meanings. The resulting data is given in Table 1.1.

Table 1.1. Results from Mott-Schottky analysis of GaAs electrodes.

Sample	N_D /cm^{-3} (measured)	N_D /cm^{-3} (vendor specified)	W at $E_{WE} = 0$ V vs. E_{sol} /nm
Substrate n^+-GaAs	$2.4 – 2.7 \times 10^{18}$	$2 – 7 \times 10^{18}$	24 – 25
Source n-GaAs	$2.1 – 2.7 \times 10^{17}$	$1 – 4 \times 10^{17}$	75 – 85
CSVT 1700 ppm	$0.6 – 1.2 \times 10^{17}$	N/A	113 – 160
CSVT 430 ppm	$4.5 – 6.4 \times 10^{17}$	N/A	49 – 58
CSVT 170 ppm	$2.8 – 4.2 \times 10^{17}$	N/A	60 – 74
CSVT 20 ppm	$1.3 – 2.4 \times 10^{17}$	N/A	80 – 109

Spectral Response Measurements

Spectral response was measured using a Bentham PVE300 PV device characterization system. The measurements were performed in the same Fc/Fc^+/ACN used for PEC measurements, diluted 1:10 with acetonitrile to decrease solution

absorbance. The solution was kept stirring as we noted increased absorption by ferrocenium if the solution was left stagnant (see Figure 1.9 for absorption spectrum). Measurements were performed under short circuit conditions with the WE (GaAs) potential referenced to the CE (Pt mesh).

The light from the monochromator was directed and focused on the sample using two 45° angled mirrors and a lens (Thor Labs). All light was incident on the sample. The light was chopped at 52 Hz and the photoresponse of the electrodes was fed into a lock-in amplifier. The unprocessed signal was recorded in nA and converted to external quantum efficiency using a calibrated responsivity standard (Bentham DH-Si 11677) which was interchanged with the cell and measured periodically to ensure conditions were constant throughout the experiment. A second Si photodiode standard (UV-005, OSI Optoelectronics) was calibrated and periodically measured inside the cell to ensure conditions within the cell were also constant.

In order to confirm our chopping frequency was appropriate for this photoelectrochemical system we measured a control electrode at three chopping frequencies, and no differences were found (Figure 1.10). We also determined that the signal was a square wave free of transients by digitizing the chopped photocurrent directly at 10 and 100 Hz (Figure 1.11). Internal quantum efficiency calculations account for reflection at the GaAs/acetonitrile interface and at the air/glass interface. They do not account for solution absorbance, which varied depending on the precise distance of the electrode from the bottom of the cell. Reflective losses at the acetonitrile/glass interface was neglected (R = 0.0018).

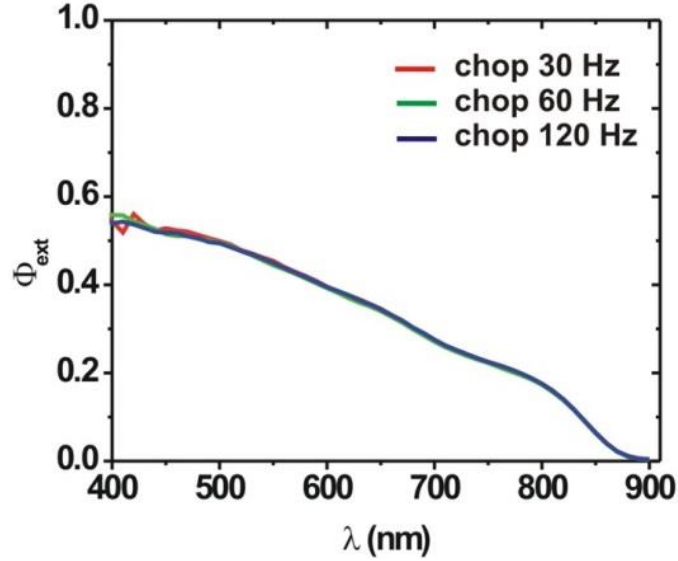


Figure 1.10. External quantum efficiency (Φ_{ext}) of an n^+-GaAs control electrode (n^+-GaAs:Si wafer) measured at a range of chopping frequencies.

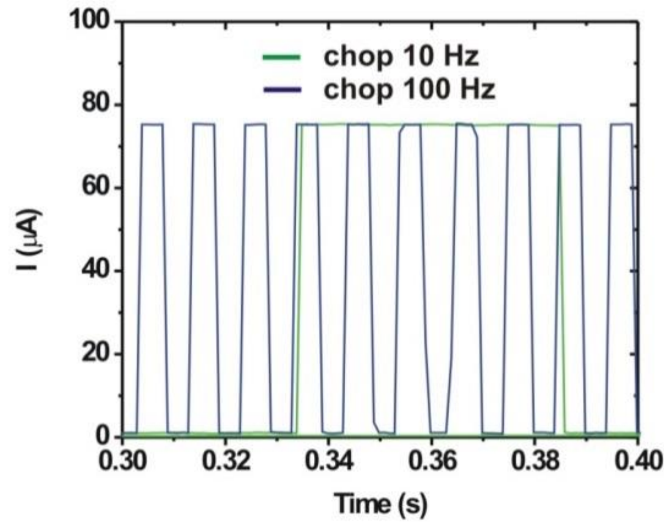


Figure 1.11. Chopped short-circuit photocurrent of a GaAs photoanode showing square wave response to a chopped light source at 10 and 100 Hz.

The internal quantum efficiency (Φ_{int}) was fitted to the Gärtner model to extract the hole diffusion length (L_D) using

$$\Phi_{int} = \left(1 - \frac{e^{-\alpha(\lambda)W}}{1+\alpha(\lambda)L_D} \right)$$

where W is the depletion layer width[3] and α(λ) is the known wavelength-dependent absorption coefficient of GaAs.[4] The previously published literature value for V_{bi} of 1.1 V was used in this calculation.[5] The depletion layer width was determined using,[3]

$$W^2 = \frac{2\varepsilon}{qN_D}\left(V_{bi} - V_{app} - kT/q\right)$$

Computer Simulation of Back Surface Fields

One possible difference between the CSVT films and the *n*-GaAs control wafers is that the films are grown on an n^+-GaAs substrate which could act as a back surface field (BSF). However, the ohmic contacting procedure used for all samples also creates n^+/n junctions that could act as BSFs. Qualitatively, we only expect the BSF to influence carrier collection if the film thickness is less than the minority carrier diffusion length, because minority carriers would need to diffuse to the back surface, get reflected, and then diffuse to the front surface. For every sample tested the film thickness (or wafer thickness) was much larger than the measured diffusion length, so we do not expect the location of the back surface field to influence the measurements. In order to support this qualitative argument we performed simulations using a 1D device-physics simulation program, PC1D.[6] The simulations show that no significant difference in the spectral response is expected with and without a BSF for the device geometry studied experimentally. The results of the simulation are shown in Figure 1.12.

Results

Deposition of GaAs Films

All films were grown in a custom CSVT reactor (Figure 1.4). A moderately doped ($N_D \sim 10^{17}$ cm^{-3}) n-GaAs wafer held at 850 °C was used as the source and a highly

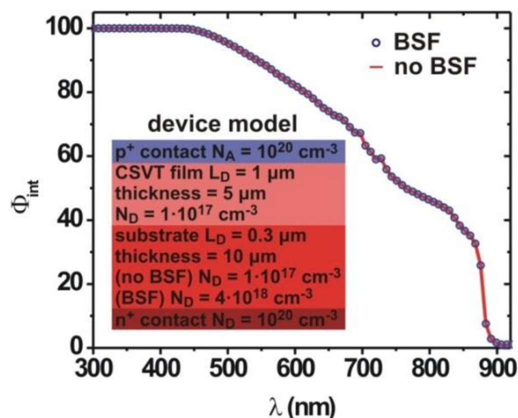


Figure 1.12. Internal quantum efficiency modeled for a CSVT GaAs film both with and without a back surface field (BSF). Parameters such as thickness diffusion length and dopant density are listed on the figure.

doped ($N_D \sim 10^{18}$ cm^{-3}) n^+-GaAs wafer held at 840 °C as the substrate. The films were grown epitaxially on GaAs substrates in order to isolate any defects associated with the CSVT growth process from those associated with the growth of GaAs on a nonlattice-matched substrate. Observed growth rates were 70−420 nm min^{-1} depending on [H_2O], which was varied from 20−1700 ppm (Figure 1.13). The linear dependence of growth rate on [H_2O] suggests that the transport rate is dictated by [H_2O] in this growth regime.

Film thicknesses, which ranged from 1.3−5.5 μm, were sufficient to ensure that effectively all incident light of energy greater than the GaAs band gap was absorbed in the CSVT film and not in the substrate wafer (Figure 1.1 B).

Photoelectrochemical J-E Measurements

Rectifying contacts were made to n-GaAs by immersing it in an electrolyte consisting of 1 M $LiClO_4$, 100 mM ferrocene, and 0.5 mM ferrocenium in dry acetonitrile. This electrolyte is known to yield reasonable PEC performance for n-GaAs.[21,22] 100 mW

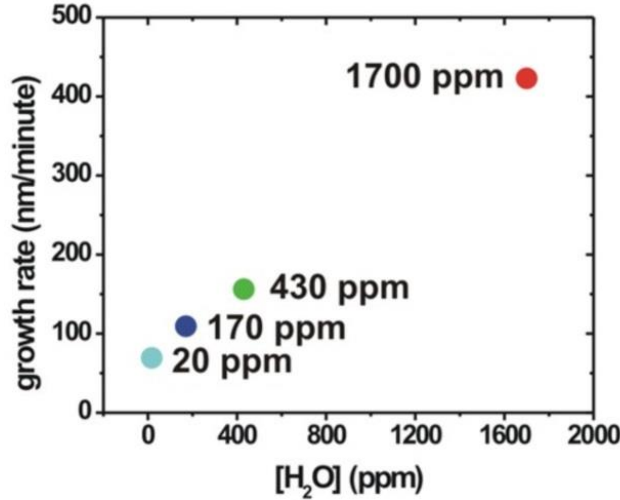


Figure 1.13. Growth rate of GaAs films as a function of [H_2O] shows a linear dependence.

cm^{-2} of solar simulation was provided by a 300 W Sylvania ELH lamp (Fig. 1.14). A Pt wire poised at the solution potential was used as a reference electrode and a separatePt mesh was used as the counter electrode. The solution was rapidly stirred during measurements to aid mass transport. Figure 1.15 shows the current-density versus potential (*J-E*) data collected for CSVT and control GaAs samples, both before and after the typical corrections for solution resistance and concentration overpotential.23 The corrected *J-E* curves were produced by calculating the corrected potential (E_{corr}) and re-

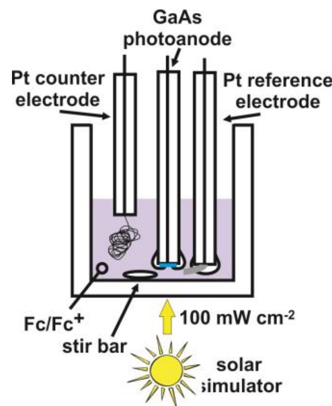


Figure 1.14. Diagram of the PEC setup used to measure GaAs optoelectronic properties.

plotting as J vs. E_{corr}. E_{corr} was calculated by subtracting the ohmic losses and concentration overpotential (η_{conc}) from each J-E data point using

$$E_{corr} = E - \eta_{conc} - IR$$

where E_{corr} is the corrected potential, I is the current, and R is the resistance determined using Ohm's law by finding the slope of a J-E curve of a planar Pt electrode. η_{conc} was determined by measuring the limiting with of planar Pt electrode and using the relation

$$\eta_{conc} = \frac{RT}{nF}\left\{\ln\left(\frac{J_{l,a}}{-J_{l,c}}\right) - \ln\left(\frac{J_{l,a} - J}{J - J_{l,c}}\right)\right\}$$

where J is the current density at the semiconductor electrode and $J_{l,a}$ and $J_{l,c}$ are the mass-transport-limited anodic and cathodic current densities, respectively.

The complete data set of measured electrode parameters for all 18 electrodes measured is given in Table 1.2. The predicted J_{SC} under 100 mW cm^{-2} ELH illumination ($J_{SC,ELH,calc}$) was determined by convolving the measured external quantum efficiency (Φ_{ext}) of the electrode with the spectral irradiance of the ELH light source. Likewise, the predicted 1-sun J_{SC} ($J_{SC,AM1.5,calc}$) was obtained by convolving Φ_{ext} with the AM1.5 spectral irradiance. ff and ff_{corr} are the as-measured fill factor and the fill-factor after correcting for series resistance and mass transport overpotential, respectively. η and η_{corr} are the as-measured overall power conversion efficiency and the overall power conversion efficiency after correcting for series resistance and mass transport overpotential, respectively. The J-E data shows that films grown with higher [H_2O] (and thus at higher growth rates) yield higher current densities, photovoltages, and efficiencies. Interestingly, the CSVT-grown GaAs films are better than the specific commercial n-GaAs control wafer, which was also used as a source to grow the CSVT

Table 1.2. Measured electronic and optoelectronic paramters of n-GaAs photoanodes.

Sample	$[H_2O]$ (ppm)	V_{OC} (V)	J_{SC} (mA cm^{-2})	$J_{SC,ELH,calc}$ (mA cm^{-2})	$J_{SC,AM1.5,calc}$ (mA cm^{-2})	η (%)	*ff*	η_{corr} (%)	ff_{corr}	L_D (nm)
CSVT film	1700	-0.72	20.2	22.1	18.6	7.8	0.53	10.2	0.70	930
CSVT film	1700	-0.70	20.2	21.9	18.7	8.6	0.61	10.5	0.74	950
CSVT film	1700	-0.72	21.6	21.8	19.3	9.3	0.59	12.8	0.72	1020
CSVT film	430	-0.71	18.6	20.8	17.7	6.7	0.51	8.7	0.67	870
CSVT film	430	-0.69	18.6	20.0	17.1	7.3	0.57	9.1	0.71	730
CSVT film	430	-0.68	19.6	20.8	17.7	7.0	0.53	9.5	0.72	900
CSVT film	170	-0.69	18.2	19.0	16.3	7.8	0.62	9.2	0.74	550
CSVT film	170	-0.71	17.9	18.8	16.2	6.8	0.54	8.8	0.69	520
CSVT film	170	-0.69	17.3	18.6	16.0	6.8	0.57	8.6	0.73	500
CSVT film	20	-0.65	16.5	16.1	14.3	5.6	0.52	7.8	0.73	260
CSVT film	20	-0.67	17.5	16.7	14.7	5.8	0.49	8.1	0.69	300
CSVT film	20	-0.63	17.5	16.7	14.7	5.8	0.52	8.3	0.75	300
n^+-GaAs wafer	N/A	-0.72	17.3	15.5	13.8	5.6	0.46	7.1	0.65	250
n^+-GaAs wafer	N/A	-0.71	16.7	15.4	13.8	5.7	0.48	7.4	0.62	260
n^+-GaAs wafer	N/A	-0.71	17.6	15.4	13.7	5.8	0.47	7.6	0.60	250
n^+-GaAs wafer	N/A	-0.60	12.1	11.7	10.7	3.5	0.49	4.9	0.68	180
n^+-GaAs wafer	N/A	-0.58	13.0	10.6	9.8	3.4	0.46	4.9	0.66	150
n^+-GaAs wafer	N/A	-0.60	12.1	11.6	10.7	3.9	0.49	5.2	0.67	170

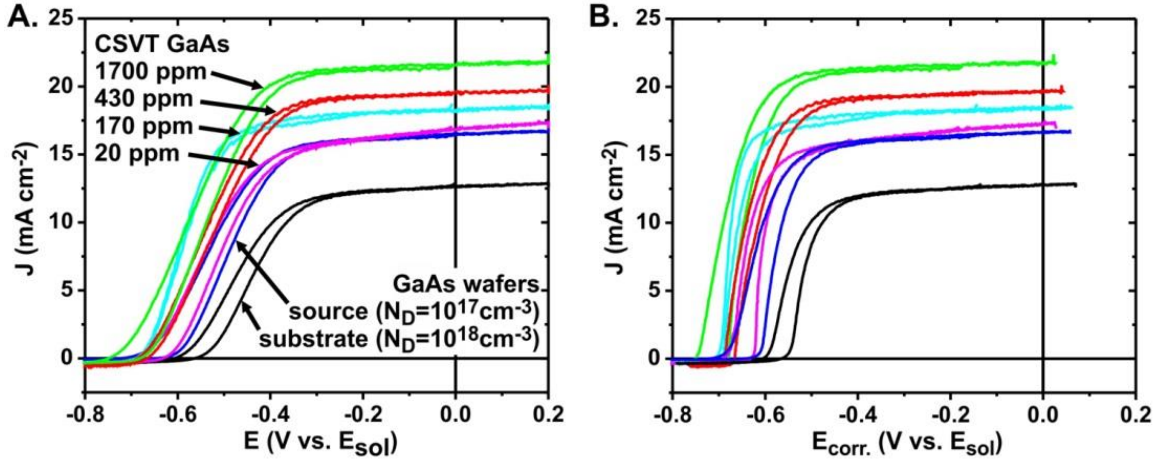


Figure 1.15. **(A)** J−E curves obtained from CSVT n-GaAs films grown at four different water concentrations and two different control wafers measured under 100 mW cm^{-2} of solar simlulation in ferrocene/ferrocenium/acetonitrile. **(B)** The same data after correction for solution resistance and concentration overpotential showing improved fill factors.

films. The n^{+}-GaAs control samples (the material which was also used as a substrate for the CSVT films) showed the lowest performance, indicating that the small amount of light absorbed within the substrate (<1% for all films) does not impact the observed performance of the CSVT samples. The lower performance of the n-GaAs control electrodes is similar to that previously measured for untextured photoelectrodes made from commercial n-GaAs.[21]

Capacitance-Voltage "Mott-Schottky" Measurements

It was hypothesized that the variations in observed J_{SC} of the CSVT GaAs samples could be caused by differences in the dopant density, which can degrade the mobility and decrease the minority carrier diffusion length, leading to increased bulk recombination losses. However, the capacitance−voltage studies showed there was no significant or systematic difference in doping between the series of CSVT GaAs samples. All samples yielded N_D between $1 - 5 \times 10^{17}$ cm^{-3} (Figure 1.16). Two other possible causes for the observed J_{SC} trend are: (1) differences in reflectance and (2) changes in

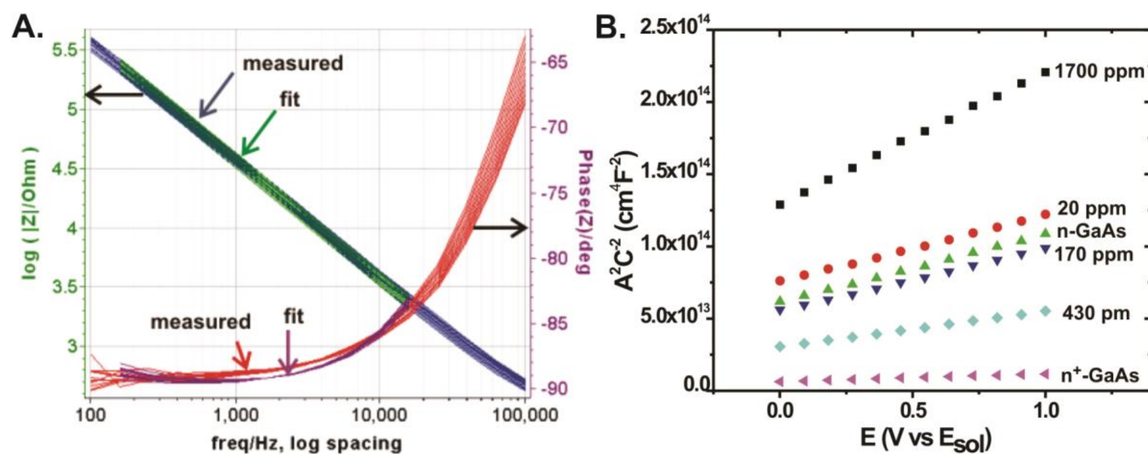


Figure 1.16. (A) Impedance data from an n-GaAs sample with a computer-generated fit. (B) Plot of area-normalized capacitance vs. applied bias for CSVT n-GaAs electrodes in Fc/Fc+/ACN (labeled according to the water vapor concentration under which they were grown) and single-crystal commercial wafers versus working electrode potential.

carrier collection efficiency that are due to differences in L_D, and associated with other nonradiative defects. It was initially hypothesized that the n-type impurities were introduced either via the Si-doped GaAs source or by diffusion from the Si-doped GaAs substrate. Neither hypothesis was correct and the n-type impurity was revealed to be sulfur using secondary ion mass spectrometry (see Chapter II).

Optical Reflectance Measurements

The reflectance of each GaAs sample was measured in air using an integrating sphere attachment on a Perkin Elmer Lambda-1050 UV/Vis/NIR spectrophotometer (Figure 1.17 (A)) in order to evaluate the reflectance of the GaAs wafers and CSVT samples and determine whether they were similar and consistent with that predicted for smooth GaAs-air interfaces based on the known optical constants of GaAs. We conclude from the reflectance measurements that observed differences in the measured J_{SC} are not due to R differences (Figure 1.17 (B)).

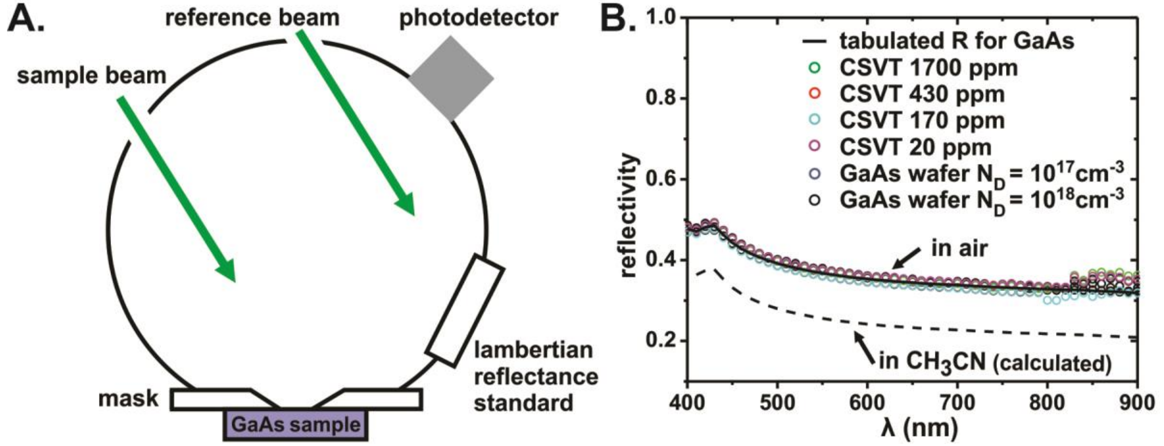


Figure 1.17. (A) Schematic of the integrating sphere with aluminum mask showing the position of sample (not to scale). **(B)** Reflectance of CSVT GaAs and commercial wafers as measured in the integrating sphere. Reflectance of GaAs in acetonitrile based on the Fresnel equations is also shown for comparison.

Spectral Response Measurement and L_D *Determination*

Spectral response measuremeasurements showed significant differences between the electrodes (Figure 1.18). The wavelength dependence of the GaAs absorption coefficient, α(λ), causes low-energy photons to be absorbed deeper in the film than high-energy photons. Thus, reduced response for lower energy photons is indicative of a shorter L_D. To quantitatively analyze the spectral response data, the external quantum efficiency (Φ_{ext}) was converted to internal quantum efficiency (Φ_{int}) using the relation,

$$\Phi_{\text{int}} = \frac{\Phi_{ext}}{(1-R_1)(1-R_2)}$$

where R_1 is the reflectance of the air/glass interface and R_2 is the reflectance of the acetonitrile/GaAs interface. R_1 and R_2 were calculated using the Fresnel equation and the known optical constants of GaAs, acetonitrile, glass, and air. The reflectance of the glass/acetonitrile interface is negligible. The dependence of Φ_{int} on excitation wavelength

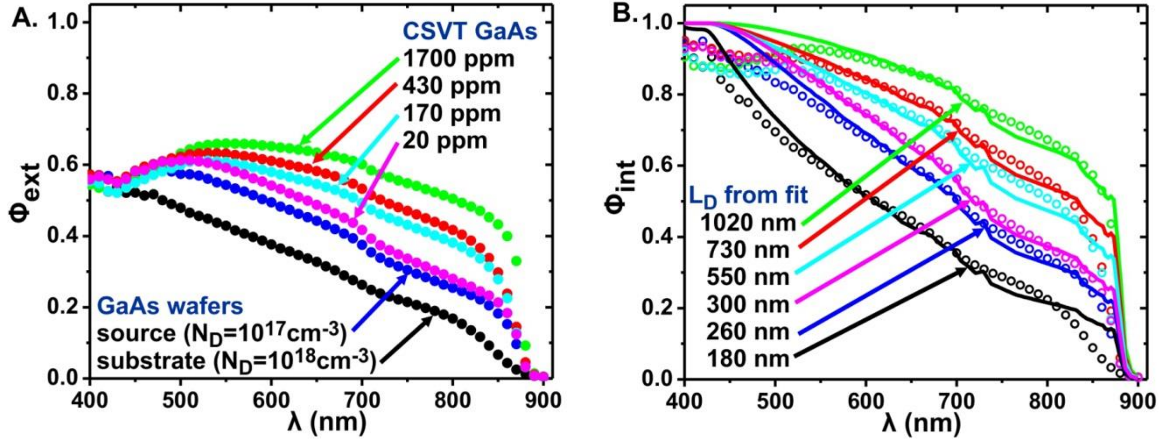


Figure 1.18. (A) External quantum efficiency and (B) internal quantum efficiency of CSVT-deposited samples and wafer controls with calculated Gartner fits and corresponding L_D values.

was fit to the Gärtner model for carrier collection in order to extract L_D according to the relation where W is the depletion layer width, as estimated by capacitance measurements, and the value of α(λ) was obtained from tabulated data (Figure 1.1 A).[3,24,25] The Gärtner model assumes perfect collection efficiency for carriers generated in the semiconductor depletion region with carrier collection in the quasi-neutral region governed by L_D and has been used to extract diffusion lengths from n-GaAs that are identical to those measured directly using electron-beaminduced- current techniques.[26] Consistent with the J−E curves, the L_D values increased with increasing growth rate and [H_2O], up to 1,020 nm for the best CSVT sample (Table 1.2). These values compare well with previous measurements on a variety of GaAs single crystals that ranged from 350 to 1200 nm.[26]

The observation that GaAs films grown with higher [H_2O] performed better than those grown with low [H_2O] is unexpected. Mimila-Arroyo and co-workers observed that the PL intensity of CSVT GaAs thin films could be improved by reducing [H_2O] during growth to less than 100 ppm and suggested this was related to reduced incorporation of oxygen defects that are known to reduce the minority carrier lifetime in GaAs.[18,27]

Increased PL is typically associated with reduced nonradiative recombination that should indicate longer L_D. We note that the films in Mimila-Arroyo's study were deposited using a higher temperature gradient of 80−130 °C, compared to the 10 °C used here. The larger driving force for deposition may have resulted in increased oxygen incorporation relative to the conditions used here. PL experiments are also highly dependent on surface recombination and thus differences in the precise surface chemistry/passivation could be important.[28] Our findings indicate that, under the present growth conditions, defects originating from the water vapor are not limiting carrier collection. Additional work is required to identify and quantify all defects and impurities as a function of growth conditions. Convolution of the spectral response data with the American Society for Testing and Materials Air Mass 1.5 Global spectrum (ASTM AM1.5G) yields photocurrents that were on average 15% lower than those measured under the ELH lamp (Table 1). These differences are due to the known differences between lamp spectra and the reference spectra.[29,30]

Conclusions and Bridge

The results reported here suggest that the electronic quality of CSVT GaAs is sufficient for use in solar energy conversion applications and motivate significant further study. The best CSVT GaAs photoanodes yielded an efficiency of 9.3%, which approaches that achieved in previous studies using the same electrolyte and illumination source with high-quality MOCVD grown GaAs epi-layers (where up to 11% efficiency was observed).[22] Correction for cell-related solution losses, that could be eliminated in a solid-state cell design, yield corrected efficiencies for the CSVT films near 13% (Table

1).[31] Furthermore, the external quantum efficiency of the CSVT GaAs thin-film devices as well as that of the control wafers could be substantially improved through the use of surface texturing both to decrease reflective losses (~24% of above band gap photons for the GaAs/ACN interface) and boost carrier collection via three-dimensional structuring.[25,32] Higher photoanode efficiencies (ca. 15%) for Ru or Os-modified, surface-roughened n-GaAs wafers have been obtained in aqueous selenide electrolytes.[33,34] Use of these electrolytes would enable higher absolute efficiencies for CSVT n-GaAs as well. Efforts to passivate the CSVT GaAs surface to increase the photovoltage in PEC cells and to enable applications in PEC water splitting are underway.[35–37] We also note that it should be possible to grow GaAs nanostructures by controlling the nucleation and growth pathways in this simple CSVT reactor without requiring molecular beam epitaxy or MOCVD equipment.[38] Because the use of single-crystal GaAs wafers as growth substrates is prohibitively expensive for practical solar energy conversion applications, we are studying the growth of CSVT GaAs on non-lattice-matched substrates and metal foils.[7,20,39]

High efficiency single-crystal solar cells solar cells generally require both a p- and n-type semiconductor, thus it is also of critical importance to develop strategies which will enable growth of a range of p- and n-type doping densities. Although n-type films were demonstrated in this study, all were doped similarly and no p-type films were grown. In Chapter II we will explore the issue of doping GaAs by CSVT as well as additional characterization techniques which can help to quantify the comparison of CSVT GaAs to MOCVD GaAs.

CHAPTER II

DOPING AND ELECTRONIC PROPERTIES OF GALLIUM ARSENIDE GROWN BY THE CLOSE-SPACED VAPOR TRANSPORT METHOD

Portions of this chapter were previously published as Ritenour, A. J.; Boucher, J. W.; DeLancey, R.; Greenaway, A. L.; Aloni, S.; Boettcher, S. W. "Doping and Electronic Properties of GaAs Grown by Close-Spaced Vapor Transport from Powder Sources for Scalable III-V Photovoltaics." Energy Environ. Sci. 2015, 8, 278-285. A. J. R. wrote the paper, made the figures, made the samples and performed the experimental work. R. D. assisted with EBIC measurements. J. B. assisted with sample synthesis. A. L. G. assited with editing. S. W. B. and S. A. provided editorial assistance and were co-principal investigators.

Introduction

Despite the merits of the CSVT technique, few CSVT GaAs devices have been reported.[19-21] We previously demonstrated CSVT *n*-GaAs films with minority carrier diffusion lengths (L_D) > 1 μm[22] and overall $\eta = 9.3\%$ in a photoelectrochemical (PEC) cell,[23] nearly equivalent to MOCVD *n*-GaAs photoanodes ($\eta = 11\%$).[24] These CSVT *n*-GaAs films were grown from Si-doped GaAs sources and exhibited free electron concentrations of $0.5\text{-}2\times10^{17}$ cm^{-3}. We have since determined that these are doped by S (which outgasses from the graphite heaters upon heating) rather than transport of Si dopants from the Si-doped GaAs source. The S doping is discussed further below (see Results and

Discussion). Controlling the dopant type and dopant density of CSVT GaAs films is a key step toward fabrication of solid-state PV devices. For PV applications, the films must also possess high carrier mobilities and $L_D > \alpha(\lambda)^{-1}$.

Here we report *n*- and *p*-GaAs films with a range of free electron and free hole concentrations (N_D and N_A, respectively) grown using CSVT from potentially low-cost powder sources. Mixing powders could also be used to access related ternary III-V materials such as $GaAs_xP_{1-x}$.[25] N_D and N_A determined from impedance and Hall-Effect measurements agree with dopant concentrations obtained from secondary ion mass spectrometry (SIMS), and demonstrate control over the dopant concentration from ~10^{16} cm^{-3} to ~10^{19} cm^{-3}. The L_D was up to ~3 μm for *n*-GaAs films and up to ~8 μm for *p*-GaAs films, determined independently *via* analysis of the internal quantum efficiency Φ_{int} and electron beam induced current (EBIC). These L_D are long with respect to $\alpha(\lambda)^{-1}$ and consistent with the measured one-sun photocurrents in the PEC configuration (> 20 mA cm^{-2} with no antireflective coating). Hall mobilities of CSVT *n*- and *p*-GaAs approach the ionized dopant scattering limit[26] and are similar to what has been achieved using MOCVD.[27]

These results demonstrate that potentially inexpensive powdered GaAs can be used to deposit GaAs films suitable for high performance III-V based PV devices[28] at high growth rate, with ~95% precursor utilization, and at ambient pressures using a simple CSVT reactor.

Methods

GaAs Thin Film Deposition

The carrier gas for CSVT was H_2 (Industrial Source, 99.999%) with water concentration $[H_2O]$ = 2,000 ppm. $[H_2O]$ was controlled by combining a stream of dry H_2 with a stream of H_2O-saturated (dew point 10 °C) H_2 using mass flow controllers (SEC 4400) and monitored with a Panametrics MM4 Hygrometer. PID controllers (Omega CN7800) were used to set the growth temperature to 850 °C and 830 °C for the source and substrate, respectively, as shown in Fig 1.2. The temperature was monitored using type K thermocouples embedded in the resistive graphite heaters. A quartz ring 12 mm in diameter and 0.8 mm thick was used as a spacer between the source and substrate. The film thicknesses of all PEC samples were 5-11 μm (measurements obtained from a Zygo 7300 optical profilometer), ensuring all light was absorbed in the CSVT GaAs film rather than the substrate. The growth rate (which depends on $[H_2O]$ used during growth[23]) was ~ 0.3 μm/min. Single-crystal <100>-oriented GaAs wafers grown by the vertical gradient freeze technique[29] (AXT, Inc.) were used as substrates. The substrates were epi-ready as received and cleaned by blowing with N_2. More details about the CSVT reactor are provided in other publications.[22, 23]

Powder GaAs sources were obtained by grinding undoped GaAs wafers (AXT) in an agate mortar and pestle and pressing at 140 MPa in a 13 mm pellet die. The mortar and pestle were cleaned by submersing in aqua regia and rinsing with 18.2 MΩ·cm water. Zn powders were separately weighed and combined with the GaAs powder prior to pressing. Te-doped powders with $[Te] < 10^{19}$ cm^{-3} were

made by grinding and pressing Te-doped wafers. A source pellet containing [Te] = 10^{19} cm^{-3} was made by combining undoped GaAs and Te powder. Single-crystal wafers were also used as sources to provide a comparison to the powders. These were cut into 13×13 mm squares and cleaned by blowing with N_2.

Photoelectrochemical Measurements

Electrodes were fabricated using standard procedures.[23] Ohmic contacts were formed on the back of the substrates by thermal evaporation of Au/Zn/Au (20 nm, 30 nm, 50 nm) for *p*-GaAs or AuGe eutectic (100 nm) for *n*-GaAs. Contacts were annealed at 450 °C for 2 min in 95% N_2 / 5% H_2.[30] Ohmic contacts were connected to Sn-Cu wire with conductive Ag adhesive (Pelco 16040-30) and attached to 6 mm diameter glass tubes with non-conductive epoxy (Hysol 1C). A circular electrode active region (~0.05 cm^2) was defined using non-conductive black epoxy (Hysol 9460).

Rectifying contacts to *n*-GaAs for current-voltage (*J*-*E*) measurements, impedance measurements, and spectral response measurements were obtained using an electrolyte consisting of 1 M $LiClO_4$ (Alfa-Aesar, 99%, anhydrous), 100 mM ferrocene (Aldrich, 98%, sublimed before use), and 0.5 mM ferrocenium tetrafluoroborate (obtained by oxidizing ferrocene with benzoquinone in the presence of HBF_4, recrystallizing in tetrahydrofuran, and drying under vacuum) in dry acetonitrile (Acros, 99.8%, distilled and dried with freshly-activated 3 Å molecular sieves).[24, 31] For spectral response measurements, the solution was diluted 1:10 with dry acetonitrile in order to reduce parasitic solution absorbance.

For one-sun *J*-*E* measurements of *p*-GaAs, an aqueous solution of 1 M HI

(Aldrich, 99.99%) and 0.125 M I_2 (Alfa-Aesar, 99.8+%) was used.[32, 33] For spectral response and impedance of *p*-GaAs a non-aqueous electrolyte consisting of 0.1 M NaI (Alfa-Aesar, 99+%, anhydrous), 0.0125 M I_2 (Sigma-Aldrich 99.99%, sublimed), and 0.1 M $LiClO_4$ in dry acetonitrile was used (see Results and Discussion below).

For all PEC measurements a potentiostat (Bio-Logic SP-200) in three-electrode configuration was used. The GaAs electrode potential (E) was referenced to the potential of a Pt wire poised at the solution potential (E_{sol}) and a Pt mesh was used as the counter electrode. The three electrodes were held in a glass 3-neck flask containing the appropriate electrolyte with the GaAs electrode < 1 mm from the bottom surface. Mass transport was aided by a magnetic stirrer. Illumination was provided by a solar simulator (Abet Technologies model 10500) for *J-E* experiments. The light intensity incident on the front face of the glass cell was 100 mW cm^{-2} as determined using a calibrated photodiode (OSI Optoelectronics UV-005). The photodiode was calibrating using an optical pyrometer (Thor Labs S310C).

Spectral Response

Spectral response of the PEC cells was measured using a Bentham PVE300 system. The monochromatic light was chopped at 35 Hz and the nA-range signal was measured using a lock-in amplifier. The chopped signal was free of transients and the amplitude of the signal was independent of chopping frequency from 10-50 Hz.[34] A calibrated photodiode (Bentham 11677) was used to determine the incident light intensity so that the nA signal could be converted to external

quantum efficiency (Φ_{ext}). The chopped photocurrent scaled linearly with the incident light intensity over five orders of magnitude (Figure 2.1).

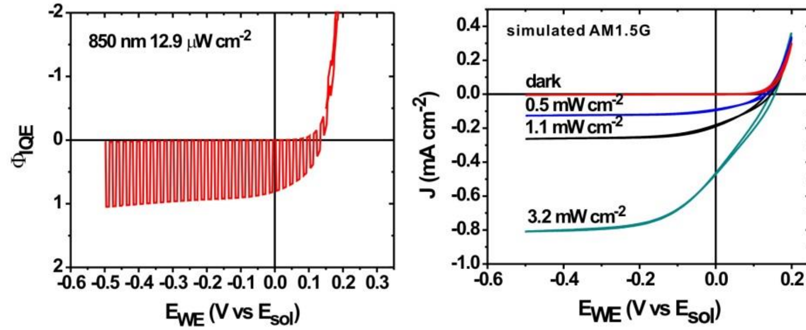


Figure 2.1. (A) Quantum efficiency vs applied bias of a p-GaAs sample measured in non-aqueous I^{-}/I^{3-} under 850 nm illumination provided by a chopped LED. The signal is free of transients and agrees with spectral response measurements done using a lock-in amplifier. (B) J-E response of a p-GaAs sample in non-aqueous I^{-}/I^{3-} measured under a solar simulator. The photocurrent scales with light intensity and is ~0 mA in the dark.

Reflectance, $R(\lambda)$, of the air|glass|acetonitrile|GaAs stack was measured (Figure 2.2) using a spectrometer with an integrating sphere (Perkin Elmer Lambda 1050).[34] This data was used to obtain Φ_{int} from $\Phi_{ext} = \Phi_{int}\,[1\text{-}R(\lambda)]$. Although films from wafer sources were not completely specular, all films possessed $R(\lambda)$ equivalent to a polished single-crystal GaAs wafer when measured in the integrating sphere. Therefore, although some of the films exhibited difffuse reflectance, the total $R(\lambda)$ was unchanged. All films grown from powder sources were specular.

Impedance Spectroscopy

Impedance measurements were conducted with a potentiostat on GaAs

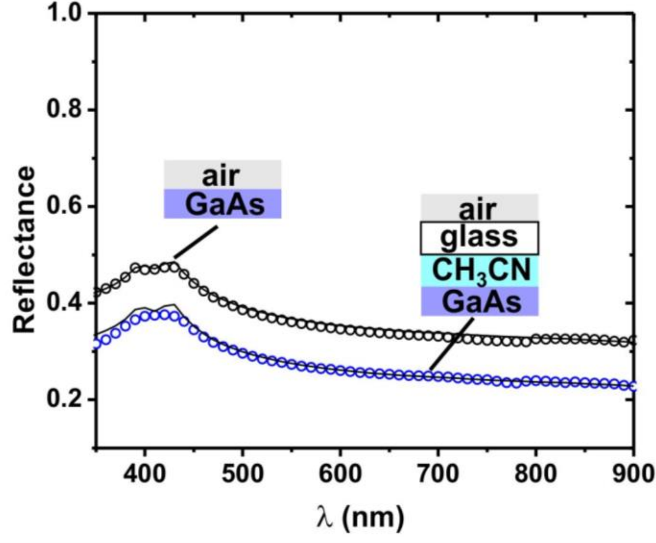


Figure 2.2. Reflectance of the air|GaAs and air|glass|acetonitrile|GaAs interfaces. The circles represent measured data while the solid curves are simulated reflectances.

electrodes in a dark box. The DC reverse bias was varied between 0 ~ 1 V in 10 steps for *n*-GaAs and 0 ~ -0.5 V in 10 steps for *p*-GaAs electrodes with a 10 mV AC bias amplitude. The impedance data were fit to the typical equivalent circuit model to extract the junction capacitance C (Figure 2.3).[35] Mott-Schottky analysis was used to determine N_D/N_A and the barrier height V_{bi} (Figure 2.4).[31, 36]

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V_{app} - kT/q\right)}{q\varepsilon NA^2}$$

The depletion region thickness W was obtained using:[37]

$$W = \sqrt{\frac{2\varepsilon}{qN}\left(V_{bi} - V_{app} - kT/q\right)}$$

where ε is the dielectric constant of GaAs, q is the fundamental charge, V_{app} is the applied bias, k is the Boltzman constant, and T is the temperature.

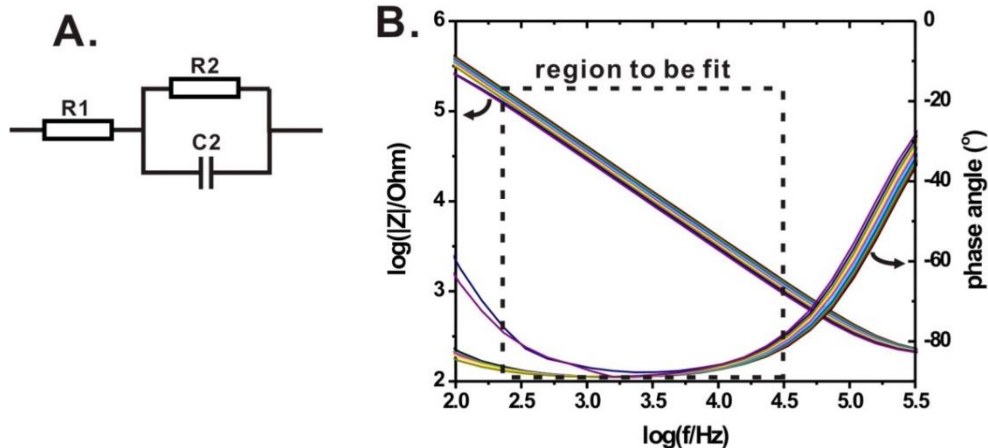


Figure 2.3. (A) Equivalent circuit used to extract junction capacitance from electrochemical impedance measurements. (B) Example of typical Z and phase angle response to DC voltage. Each colored curve represents a different DC bias.

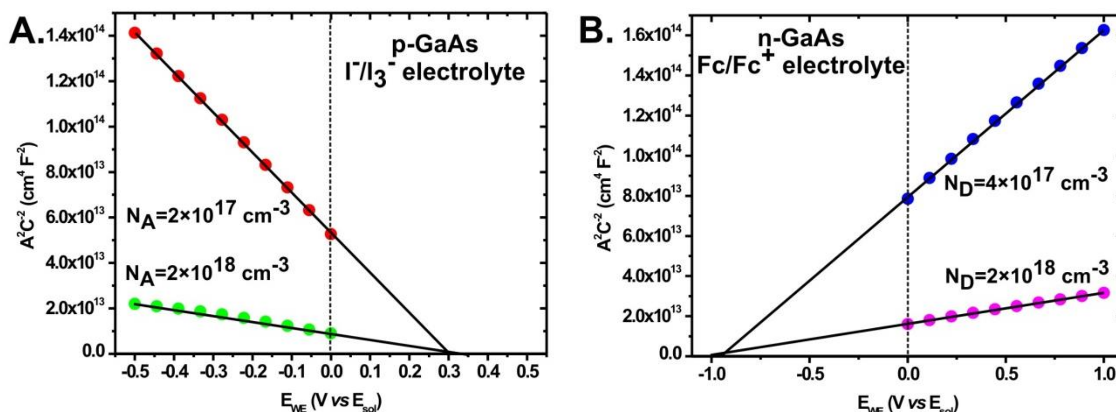


Figure 2.4. Representative Mott-Schottky plots for (A) p-GaAs and (B) n-GaAs.

Hall Effect Measurements

GaAs films deposited on undoped semi-insulating (resistivity $\rho > 10^7$ Ω·cm) substrates were cut into squares (0.49-0.64 cm^2) and ohmic contacts were applied to the corners. The carrier type, ρ, N_A or N_D, and majority carrier mobility (μ_e or μ_h for electron or hole mobility, respectively) were obtained using the Van der Pauw method.[38] Hall Effect measurements were conducted at 300 K on an Ecopia HMS-5000 Hall Effect system.

Time-of-Flight Secondary Ion Mass Spectrometry

Mass spectra were obtained from a Cameca ION-TOF mass spectrometer with Cs^+ sputter gun and Bi^+ analysis gun. Ion counts were converted to bulk impurity concentrations using relative sensitivity factors (RSF).

$$[E] = RSF_E \times \frac{I_E}{I_M}$$

where [E] is the concentration of the element being analyzed in units of cm^{-3}, RSF_E is the relative sensitivity factor of the element in the GaAs matrix, I_E is the signal of the element of interest, and I_M is the signal of the GaAs matrix. Values for *RSF* were obtained from the literature.[39] To confirm the validity of published *RSF* values with our experiment, we measured two ion implanted samples (one ^{28}Si-implanted and one ^{16}O-implanted to a dose of 5×10^{14} cm^{-2} at 1.2 keV) and compared the obtained *RSF* values (based on Monte-Carlo simulation of the [Si] depth profile) to the literature values. In both cases the values agreed (Figure 2.5).

We also used TOF-SIMS to measure the [Te] and [Si] of Te-doped and Si-doped GaAs wafers purchased from AXT. Measured [Te] and [Si] agreed with both the vendor specifications and with N_D determined from impedance analysis. One CSVT-deposited *p*-GaAs film was sent to QSPEC for [Zn] determination on a magnetic sector SIMS, which possesses higher sensitivity to Zn than TOF-SIMS (Figure 2.6).

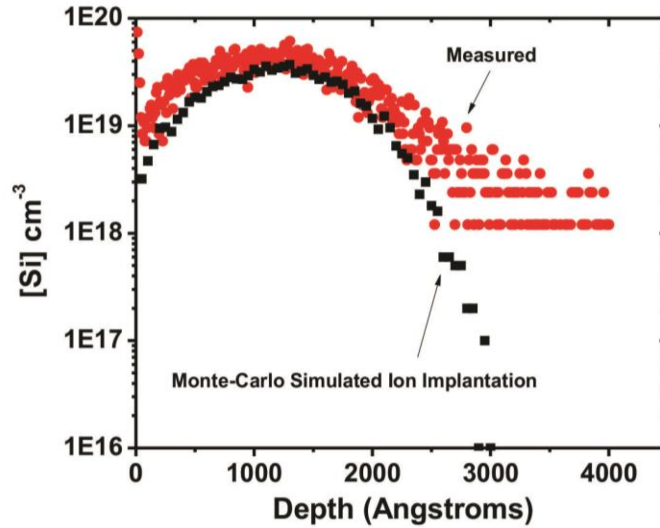


Figure 2.5. Measured and simulated Si depth profiles for an ion-implanted GaAs sample.

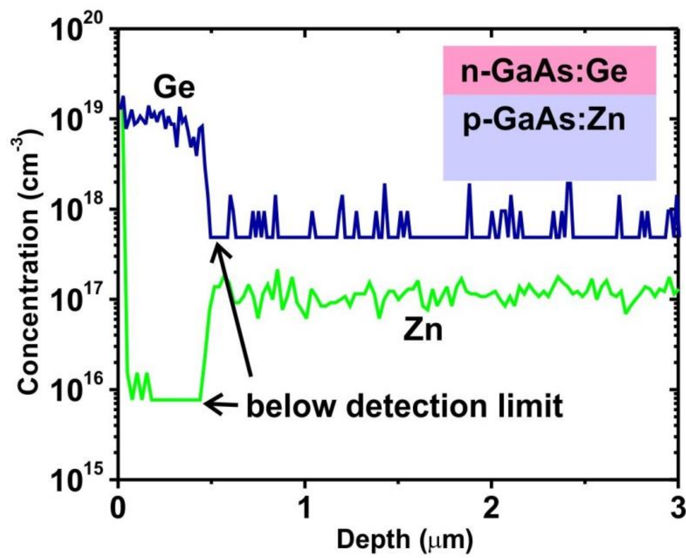


Figure 2.6. Magnetic sector SIMS profile of an n-GaAs:Ge on p-GaAs:Zn pn homojunction device. Zn profile confirms that the CSVT-grown absorber layer is Zn doped ~ 1×10^{17} cm^{-3}.

Where applicable, the identity of atoms were confirmed by matching the signal to the natural abundance of isotopes. Te has a variety of isotopes which are easily identified (Figure 2.7).

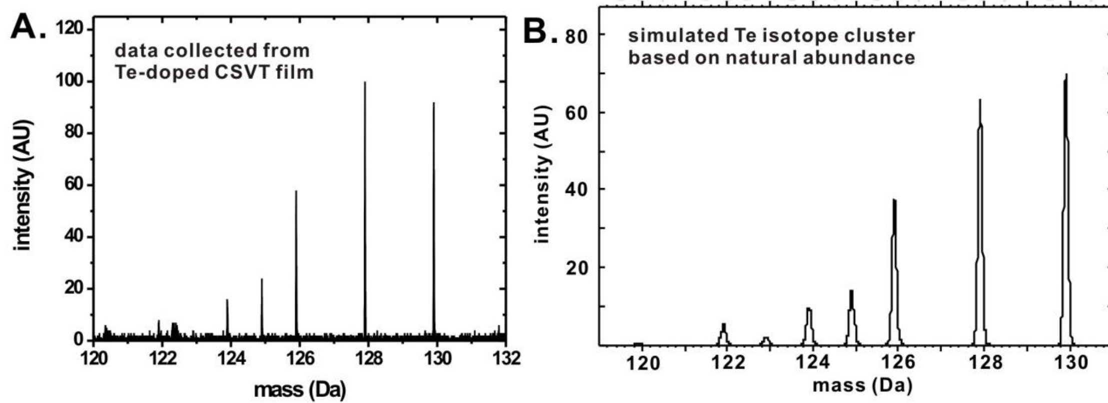


Figure 2.7. (A) Te distribution observed in SIMS. (B) natural isotopic distribution of Te.

Electron Beam-Induced Current

The EBIC measurements were conducted in a scanning electron microscope (FEI Quanta 200F). The electron beam was scanned toward the Schottky contact and the resulting current transients were recorded from a Matelect ISM-6A induced signal monitor. L_D was extracted from the decays according to:

$$I = qN_C e^{-x/L_D}$$

where the beam-induced current I is proportional to the exponential term, N_C is the number of minority carriers generated by the excitation beam per second, and x is the separation between the excitation beam target and the Schottky junction.[40] The Schottky contact pads were 50 μm gold squares patterned using photolithographic lift-off with a negative photoresist (AZ 5214E).

Prior to EBIC experiments, surface passivation was needed to lower the surface recombination velocity (SRV). Surface passivation was accomplished by etching with 5 M HCl, rinsing with 18.2 MΩ·cm water, immersing in aqueous 1M Na_2S,[41] rinsing with water and ethanol, and drying with N_2. Samples were

immediately pumped into the vacuum chamber and measured within 20 min after passivation. Results obtained without passivation varied as a function of accelerating voltage (V_{acc}) and did not produce reliable values of L_D (see Results and Discussion). The signal decays used to extract L_D fit the exponential equation over several orders of magnitude of current (Figure 2.8).

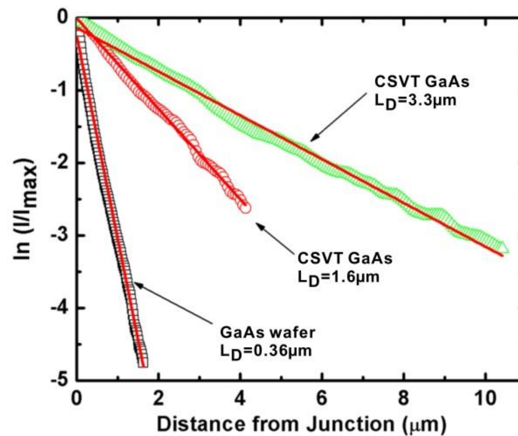


Figure 2.8. EBIC decays with linear fits used to extract L_D. These were obtained from passivated GaAs samples measured with low accelerating voltages of 2-5 keV.

Results and Discussion

Growth and Doping from Powder and Wafer Sources

In order to fabricate high-efficiency GaAs PV devices, it is important to be able to control both N_A and N_D while maintaining suitable electronic quality of the GaAs layers. Thus to demonstrate the utility of the CSVT technique, it is necessary to determine which dopants are transported by CSVT, how the source dopant concentration is related to the film dopant concentration, and how they affect the electronic quality of the layers.

We previously reported the growth of n-GaAs films by CSVT from Si-

doped wafer sources and hypothesized that the films were Si-doped since the ND of the films ($\sim 3\times10^{17}$ cm^{-3}) matched the [Si] in the source wafer. However, upon TOF-SIMS analysis we determined that the films were S-doped rather than Si-doped (Figure 2.9). The poortransport efficiency of Si is likely related to the low vapor pressure of SiO_2, which forms at high temperatures in the presence of H_2O. Unintentional S-doping of GaAs layers grown by CSVT has also been reported in other studies.[42, 43]

The unintentional S impurity is undesirable since it is a compensating defect in *p*-GaAs films. We used TOF-SIMS to determine that the graphite heaters were a source of S impurity (Figure 2.10). After fabricating purified heaters, the unintentional S-doping of the films decreased to $[S] \leq 7\times10^{16}$ cm^{-3} as determined by TOF-SIMS analysis of the films (Figure 2.11). Although the [S] could likely be further reduced by using non-porous, higher-purity heater materials (*e.g.* more-expensive pyrolysis-derived graphite), for this study the [S] achieved was low

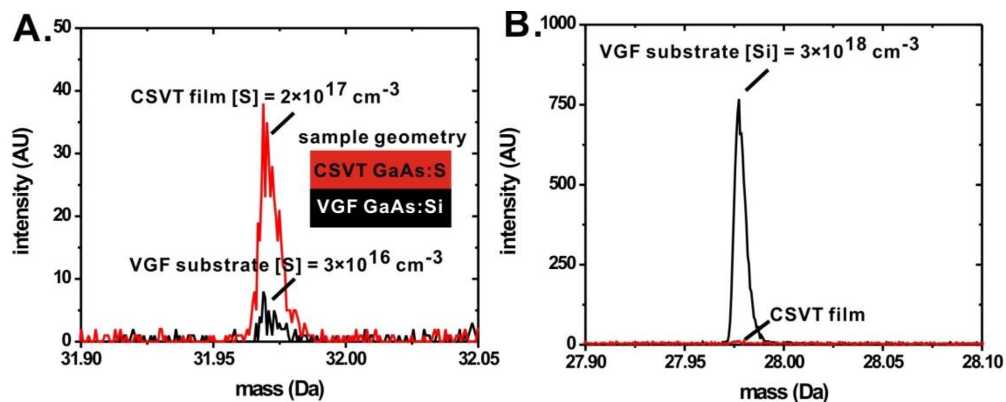


Figure 2.9. (A) ^{32}S region and (B) ^{28}Si region of the mass spectrum for a CSVT film deposited on a Si-doped n^+-GaAs substrate. The mass spectra indicate that the CSVT films are S-doped, not doped by diffusion of Si atoms from the substrate.

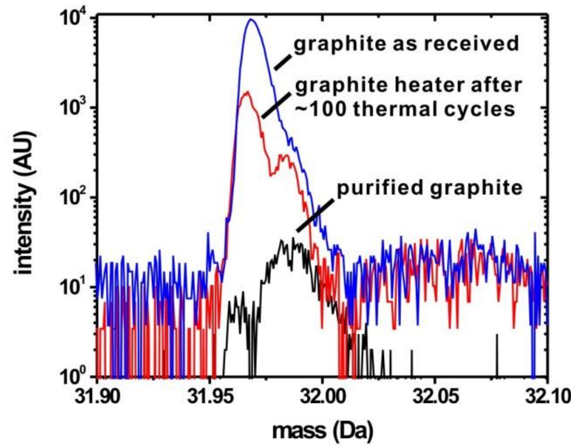


Figure 2.10. Mass spectrum of the ^{32}S region for the graphite heaters as received, after ~100 growth cycles, and after additional purification.

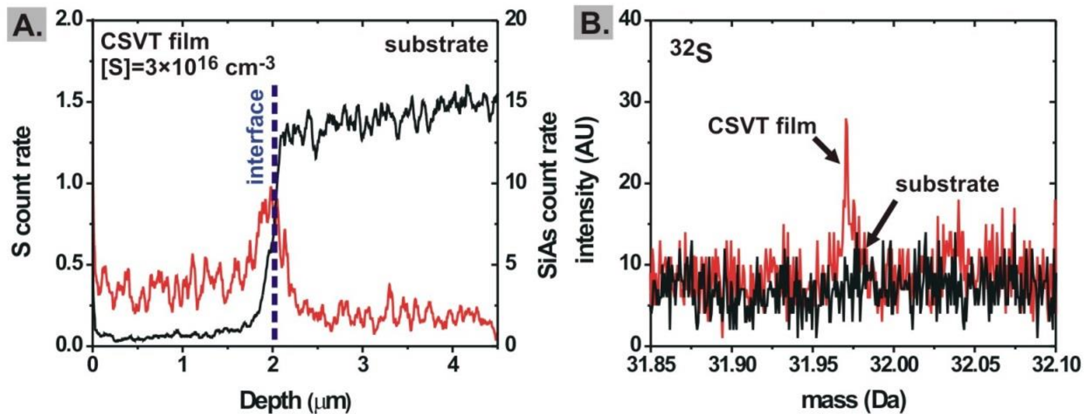


Figure 2.11. (A) TOF-SIMS depth profile of a CSVT GaAs film grown after purifying the graphite heaters which shows the S in the film (red line) and Si in the substrate (SiAs counts, black line). (B) Integrated signal in the ^{32}S region from the film and substrate indicating decreased sulfur contamination after heater purification.

enough to permit growth of *p*-GaAs films with $N_A \geq 10^{17}$ cm^{-3}, which is appropriate for use as a *p*-type absorbing layer in a PV device.

Zn is widely used as a *p*-type dopant in GaAs and has been shown to transport by CSVT.[43] GaAs films grown using CSVT from Zn-doped wafers possess ~1/100th the N_A of the source wafer.[43] Commercial GaAs wafers were available with [Zn] < 2×10^{19} cm^{-3},

setting an upper limit of $N_A \approx 2 \times 10^{17}$ cm^{-3} for CSVT films grown from commercially available sources (practically less, due to S compensation). This is problematic since some active photovoltaic device components (e.g. emitters and back surface fields) require $N_A > 2\times10^{17}$ cm^{-3}. In order to grow *p*-GaAs films with higher N_A, we mixed undoped GaAs (from undoped GaAs wafers) and Zn powders at the desired ratio and pressed the mixtures into pellets in a pellet press. These pellet sources possessed [Zn] up to 5×10^{21} cm^{-3}. GaAs wafers with this [Zn] are not readily available from commercial vendors, so the synthesis of these sources enabled us to grow *p*-GaAs:Zn films with higher [Zn] than could otherwise be obtained. These pellet sources yielded *p*-GaAs films with N_A up to ~2×10^{19} cm^{-3} (Table 2.1).

Table 2.1. Dopant densities (measured by impedance analysis and Hall Effect) and impurity concentrations (determined by TOF-SIMS analysis) of several CSVT GaAs films deposited from powder and wafer sources.

powder or wafer source	source dopant species (E)	source [E] (cm^{-3})^{*a}	Impedance analysis N_D-N_A (cm^{-3}) (average of three electrodes)	Hall Effect N_D-N_A (cm^{-3}) (one sample)	[E] from SIMS (cm^{-3}) (one sample)
wafer	Te	2-4 × 10^{18}	$3\times10^{18} \pm 1\times10^{18}$	--	2×10^{18}
powder	Te	2-4 × 10^{18}	$4\times10^{18} \pm 1\times10^{18}$	3×10^{18}	--
wafer	Te	3-6 × 10^{17}	$4\times10^{17} \pm 4\times10^{16}$	3×10^{17}	6×10^{17}
powder	Te	3-6 × 10^{17}	$7\times10^{17} \pm 2\times10^{17}$	6×10^{17}	--
powder	Zn	5×10^{21}	$-2\times10^{19} \pm 3\times10^{18}$	-4×10^{19}	--
powder	Zn	5×10^{20}	$-4\times10^{18} \pm 7\times10^{17}$	-4×10^{18}	--
wafer	Zn	1-2 × 10^{19}	$-2\times10^{17} \pm 1\times10^{16}$	-1×10^{17}	1×10^{17}
powder	S$^{\dagger b}$	-$^{\dagger b}$	$1\times10^{17} \pm 4\times10^{16}$	2×10^{16}	3×10^{16}
wafer	S$^{\dagger b}$	-$^{\dagger b}$	$7\times10^{16} \pm 3\times10^{16}$	8×10^{16}	7×10^{16}

*a: for wafer sources the dopant density was provided by the manufacturer; for Zn-doped powder sources the dopant density was calculated from the mass of the GaAs powder and the Zn powder used. †b: the S dopant was not intentionally added.

In order to control N_D, we used Te-doped GaAs sources It has been shown using impedance profiling that GaAs films grown using CSVT from Te-doped wafers possess N_D equivalent to the source wafers.[43-45] We reproduced these results by using two *n*-GaAs:Te sources with different [Te] to grow GaAs films on degenerately-doped GaAs:Si substrates and measuring N_D with impedance profiling. In order to confirm that the dopants were transported by CSVT and not diffused from the substrate, we also deposited *n*-GaAs:Te films on undoped, semi-insulating substrates. Hall Effect measurements of these samples confirm the same relationship, $N_D \approx$ source [Te]. We also show using TOF-SIMS that the films possess [Te] similar to the source's [Te] and contain no Si from the GaAs:Si substrate (Figure 2.12). All of this data is summarized in Table 2.1.

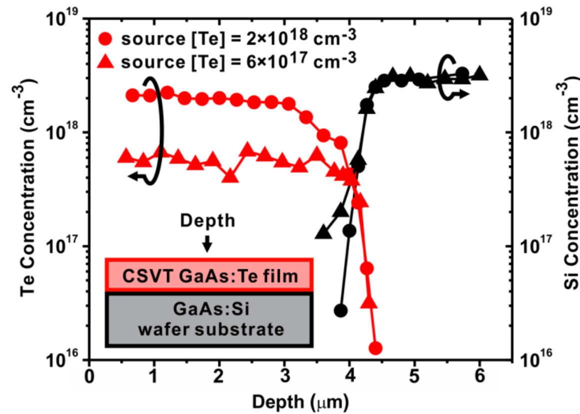


Figure 2.12. SIMS depth profiles of two *n*-GaAs films grown from differently-doped GaAs:Te sources on GaAs:Si substrates. The Te depth profiles are shown in red and Si in black. Circles denote the film was grown from a source containing [Te] = 2×10^{18} cm^{-3}, triangles denote the film was grown from a source with [Te] = 6×10^{17} cm^{-3}.

Photoelectrochemical J-E Analysis

The PEC GaAs|electrolyte junction is a convenient tool which enables the study of material properties such as photocurrent *vs* potential (*J-E*) response,

impedance spectroscopy, and Φ_{int} without fabrication of solid state devices.[23, 24, 31]

Electrodes of CSVT *n*-GaAs films were immersed in a non-aqueous ferrocene/ferrocenium electrolyte (Fc/Fc^+) and their *J*-*E* response was measured under 100 mW cm^{-2} of simulated AM1.5G irradiation.[24] Commercial <100>-oriented single-crystal wafers were measured as controls. The CSVT samples produced open-circuit voltages (V_{oc}) up to 0.83 V, equivalent to that attained by others using MOCVD *n*-GaAs.[46, 47] Short-circuit current density (J_{sc}) was ~20 mA cm^{-2} for moderately-doped samples having $N_D = 10^{16} \sim 10^{17}$ cm^{-3}. The performance of all samples exceed the respective bare substrates and similarly-doped GaAs control wafers (Figure 2.13). There were no significant differences between films grown from powder and wafer sources. Lower photocurrent was observed in highly-doped samples, which also exhibit lower μ_h (and consequently L_D) due to carrier scattering by ionized dopant atoms in the lattice (see Hall Effect measurements below).[48, 49]

Electrodes of CSVT *p*-GaAs films and control wafers were immersed in an aq. iodide/triiodide electrolyte (I^-/I_3^-) and their *J*-*E* response was measured under 100 mW cm^{-2} of simulated AM1.5G irradiation (Figure 2.13).[32, 33] The V_{oc} was 0.15 - 0.20 V *vs* E_{sol}, lower than the *n*-GaAs samples due to surface pinning of the *p*-GaAs Fermi level near the valence band edge.[32] The best samples exhibited J_{sc} ~20 mA cm^{-2}, similar to the best *n*-GaAs samples despite the higher parasitic light absorption of the I^-/I^{3-} electrolyte. All CSVT *p*-GaAs films (including those synthesized with $N_A > 10^{18}$ cm^{-3}) exhibited

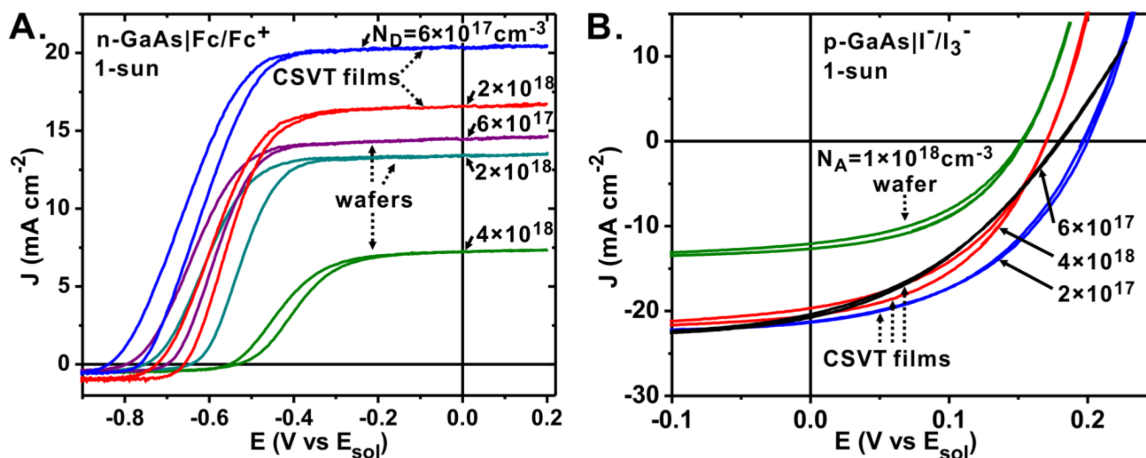


Figure 2.13. Photoelectrochemical *J-E* curves of (**A**) *n*-GaAs and (**B**) *p*-GaAs CSVT films and control wafers. The curves are labeled with the corresponding sample's free carrier concentration in cm^{-3}. The selected curves are representative of other electrodes obtained from the same samples and from other samples with similar free carrier concentrations.

higher photocurrent than the *p*-GaAs control wafer ($N_A = 1\times10^{18}$ $cm^{-3,}$ $J_{sc} = 12$ mA cm^{-2}) indicating lower bulk recombination and a longer L_D.

Spectral Response and L_D Determination

In order determine the L_D for each sample we measured the spectral response using the short-circuit PEC configuration ($E_{WE} = 0$ V *vs* E_{sol}) under low-intensity chopped monochromatic light. For the *n*-GaAs films such measurements in the Fc/Fc^+ electrolyte are well-developed. Spectral response measurements of *p*-GaAs in aqueous I^-/I^{3-}, however, were complicated by the solubility of GaAs in the acidic I^-/I^{3-} electrolyte.

No etching of *p*-GaAs was observed in the aq. solution after hours of sustained operation as long as illumination was provided. However, a nA-range anodic current was observed in the aqueous solution when under dark or low-light conditions (< 1 μW cm^{-2}). This was problematic for spectral response, (which uses

a nA-range chopped light source) and impedance analysis, which is conducted in the dark. We suspect the *p*-GaAs surface, while unstable in H_2O especially at low pH,[50] is cathodically stabilized by the photo-excited minority carrier electrons, causing it to act as a photo-gated battery.

Therefore we used a non-aqueous solution for the *p*-GaAs spectral response and impedance measurements. We used NaI to provide I^- rather than HI. We also reduced the concentration of redox couple in order to decrease parasitic light absorbance. The low-concentration of redox couple in non-aqueous solution was sufficient to support the nA-range signal and exhibited no photo-gated current (Fig. 2.1).

Trends for both *n* and *p*-type GaAs in J_{sc} were mirrored by the spectral response curves (Figure 2.14). Due to the wavelength dependence of $\alpha(\lambda)$, photons with energies near the band-gap E_g are absorbed further from the surface than those with higher energies (Figure 1.1). Thus Φ_{int} decays to zero at E_g. This can be modeled using the Gärtner equation, which assumes no depletion region recombination and that the L_D governs bulk recombination:

$$\Phi_{int} = \left(1 - \frac{e^{-\alpha(\lambda)W}}{1+\alpha(\lambda)L_D}\right)$$

where W is the width of the semiconductor depletion region.[51] This approach produces reliable estimates of L_D for GaAs[52] and other semiconductors.[53] Using

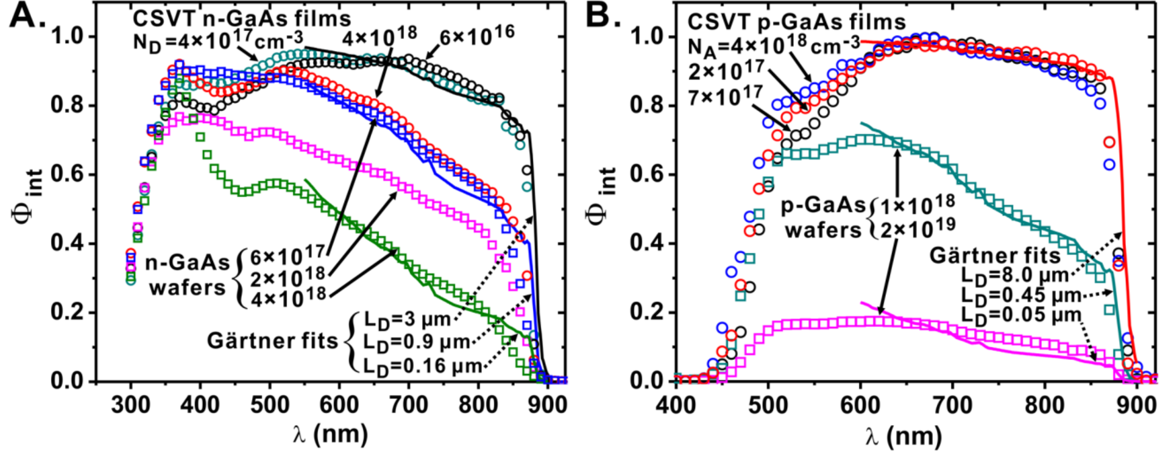


Figure 2.14. Φ_{int} measurements obtained using PEC on n-GaAs (A) and p-GaAs samples (B). Experimental data are plotted as circles and calculated L_D fits are plotted as solid curves. The selected curves are representative of other electrodes obtained from the same samples and from other samples with similar free carrier concentrations.

this technique we measured three electrodes of each film.

One parameter fits to Φ_{int} match the experimental data well (Figure 2.14). Moderately-doped *n*-GaAs CSVT films have $L_D \sim 2.9 \pm 0.2$ μm, while CSVT p^+-GaAs films possess $L_D = 5.4 \pm 0.1$ μm and moderately-doped p-GaAs films possess $L_D = 7.4 \pm 0.4$ μm. The L_D is higher in *p*-GaAs because μ_e is higher than μ_h, which in turn is due to the curvature of the conduction and valence bands.[54] For all CSVT samples, the measured L_D was significantly higher than that of the control GaAs wafers ($L_D = 0.42$ μm for *n*-GaAs:Te, 0.16 μm for n^+-GaAs:Si, 0.45 μm for *p*-GaAs:Zn, and 0.05 μm for p^+-GaAs:Zn) and consistent with one-sun Jsc measurements (see above).

Electron Beam-Induced Current

Because GaAs has a direct bandgap and large $\alpha(\lambda)$,[55] when L_D exceeds several μm, the fraction of photons absorbed deeper than $L_D + W$ is small, making determination of L_D by the Gärtner model less precise.

In EBIC analysis, the proximity of the excitation source to the charge separating

junction is controlled by rastering an electron beam toward a Schottky contact (Figure 2.15A), and is thus independent of $\alpha(\lambda)$. The beam-induced current is measured as a function of the distance between the junction and the excitation source, and L_D is determined by fitting the current decay.

After fabricating rectifying Au|*n*-GaAs junctions and measuring the EBIC response of the junctions, we observed that the response was a function of V_{acc} (Figure 2.15), complicating accurate extraction of L_D.

In an ideal EBIC experiment, the excitation volume (which is proportional to V_{acc}) is small with respect to L_D and the EBIC decay is dominated by bulk recombination with surface recombination playing a negligible role. These assumptions are invalid for unpassivated GaAs, which has a high SRV and a short L_D relative to indirect absorbers

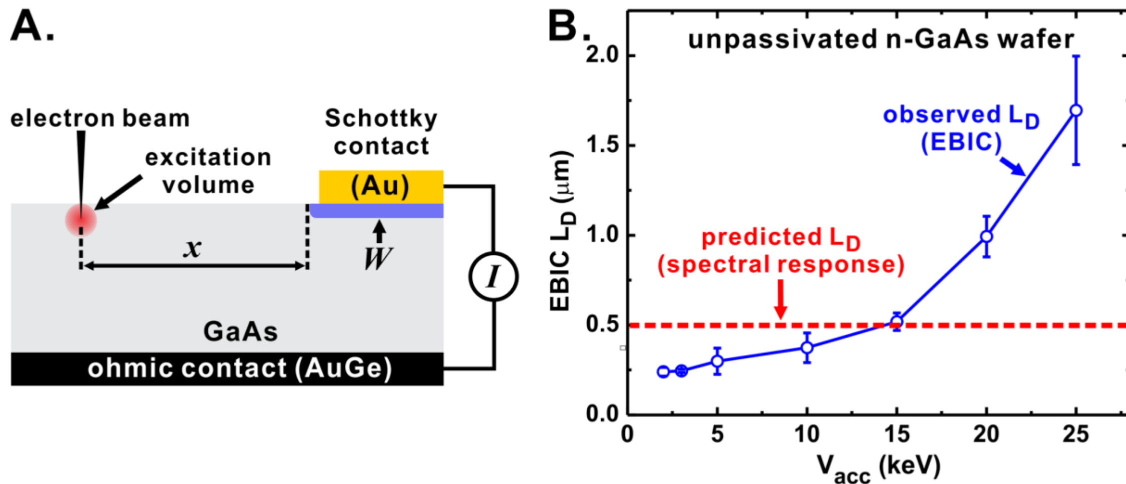


Figure 2.15. (A) Schematic of the EBIC experiment. X is the separation between the excitation source and the rectifying contact, I is the induced current, and W the depletion region. (B) The observed EBIC decay constant as a function of Vacc. The red dashed line indicates L_D predicted by spectral response using the Gärtner method. The sample was an unpassivated single-crystal n-GaAs:Te wafer.

like Si. Thus at low V_{acc} the EBIC decay is dominated by surface recombination yielding erroneously low L_D, while at high V_{acc} the excitation volume overlaps with the depletion region, yielding erroneously high L_D. We note that in the experiments with unpassivated GaAs, the L_D obtained from EBIC analysis coincidentally agrees with spectral response when V_{acc} = 10-15 keV is used, which matches the Vacc used in other studies.[52]

In order to obtain EBIC data which is fits the exponential decay model, we used Na_2S to passivate the GaAs surface thereby lowering the SRV.[56] We also used a low V_{acc} ≤ 5 keV in order to maintain a small interaction volume. After passivation, both spectral response and EBIC yielded similar values of L_D for V_{acc} ≤ 5 keV (Fig. 2.16). Comparing the two techniques we observe more dispersion in the EBIC results (Fig. 2.16), but similar overall trends. We suspect the EBIC and spectral response results differ because spectral response averages the current over a relatively large region (generally 0.05 cm^2), while EBIC measures the current decay of a line-scan and is therefore more sensitive to local recombination-inducing surface/bulk defects. Nonetheless, the direct measurement

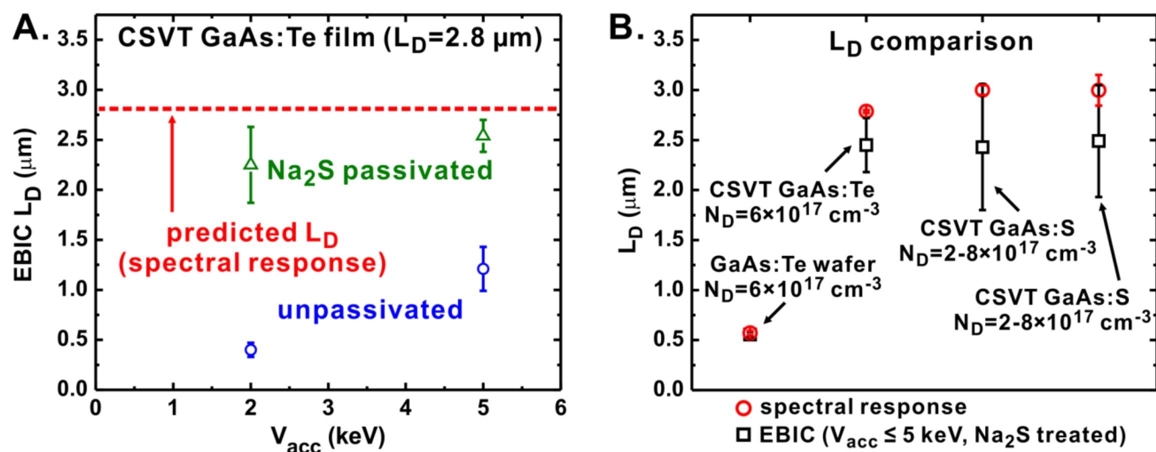


Figure 2.16. (A) L_D measured by EBIC on the same CSVT GaAs film before and after passivation by Na_2S. The dashed line indicates the L_D predicted by spectral response. (B) Comparison of L_D obtained by spectral response and EBIC techniques.

of L_D by EBIC using Na_2S passivation confirms the long L_D obtained from fitting PEC spectral response curves.

Hall Mobility and Dopant Density

Films grown from a variety of p- and n-GaAs sources were deposited on undoped semi-insulating GaAs for Hall-Effect measurements. The data indicates that *n*-GaAs and *p*-GaAs films deposited using CSVT (from both powder and wafer sources) have similar μ_e and μ_h to films deposited by MOCVD (Figure 2.17).[27, 57]

As N_D and N_A are increased, μ_e and μ_h decrease due to increased scattering from the ionized dopant atoms in the lattice (Figure 2.17).[26, 48, 49] The measured μ_e and μ_h of CSVT GaAs films deviate from the MOCVD values more for lightly-doped samples than for highly-doped samples. This is likely because at lower N_D/N_A, the influence of trace compensating impurities and crystal defects becomes important relative to the dopant atom scattering. Overall, these results indicate that CSVT

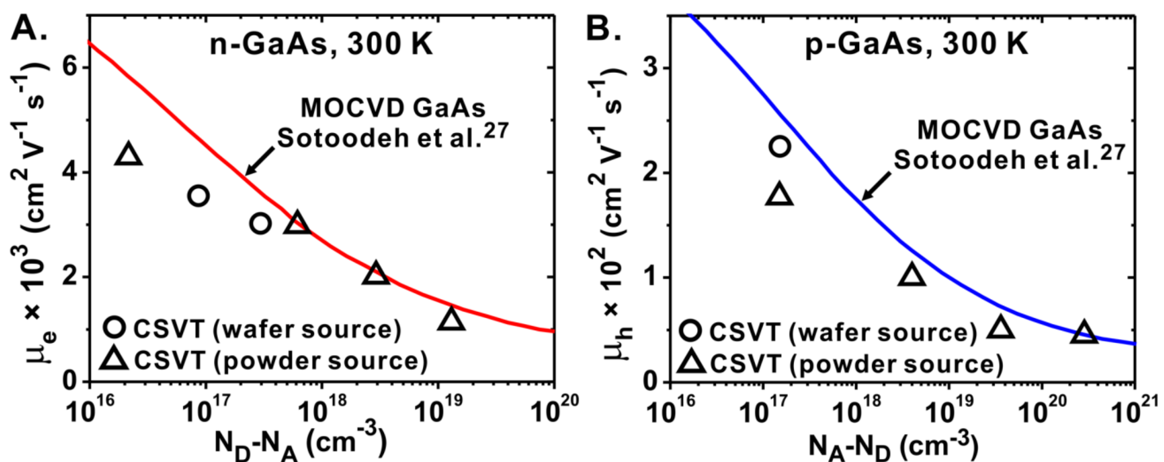


Figure 2.17. Hall mobilities of n- and p-GaAs films as a function of N_D and N_A. Solid curves represent the Hall mobility of high-quality epitaxially-grown MOCVD GaAs.[27]

from GaAs powder sources is competitive with MOCVD in terms of the achievable μ_e and μ_h for a wide range of N_D/N_A.

No significant differences were observed between films deposited from powder between substrate and the gas phase. This reult is expected because the growth takes place at the interface between the substrate and the gas phase. Thus the source's crystalline quality should not affect the CSVT process as long as it does not affect the ability of the surface to be etched by H_2O to produce vapor phase As_2 and Ga_2O. This implies that there is no need for crystalline powder sources, and lower quality powders could potentially be used as sources, for example those made by reaction of Ga and As at low temperatures.[58]

Conclusions

Epitaxial films of GaAs possessing a wide range of N_D and N_A were deposited *via* H_2O-mediated CSVT with growth rate > 0.3 μm min^{-1} at ambient pressure from powdered GaAs precursors. N_D and N_A were measured and confirmed using complementary analyses which gave equivalent results (impedance spectroscopy, Hall Effect measurements, and TOF-SIMS). This is an important step toward the fabrication of more complex device architectures such as *p-n* junctions.

The room temperature mobilities of CSVT GaAs films were similar to those produced in the literature using MOCVD, despite the relatively high growth rates and use of H_2O vapor as a transport agent. Due to the high $\alpha(\lambda)$ of GaAs,[55] the L_D (2-3 μm for *n*-GaAs and 5-8 μm for *p*-GaAs) was sufficient to yield $J_{sc} \approx 20$ mA

cm^{-2} which is near the one-sun limit (22.5 mA cm^{-2}) for specular GaAs with no anti-reflective coating in acetonitrile. For this μ_e and L_D we estimate an electron lifetime of $\tau_e \sim 7$ ns for the $N_A = 1\text{-}2\times10^{17}$ cm^{-3} *p*-GaAs films. According to previously published simulations[28] using this lifetime, $\eta \approx 25\%$ single-junction photovoltaics could be fabricated if other device-engineering challenges (such as how to create rectifying solid-state junctions and passivate the surfaces) can be solved. Initial efforts to produce GaAs *p-n* junction PV solar cells using CSVT have produced promising results with $V_{oc} > 0.9$ V and $\Phi_{int} > 0.9$, but they are beyond the scope of this study.[59]

Bridge

In addition to the high capital cost associated with MOCVD production of GaAs, lattice-matched substrates are also expensive relative to Si wafers. Tandem architectures which utilize the larger indirect band-gap and smaller lattice constant (closer to Si) of $GaAs_xP_{1-x}$ could yield $\eta > 35\%$ devices on Si substrates if challenges associated with the thermal and lattice mismatch can be addressed.[60] Growth techniques such as heteroepitaxy, selective area epitaxy[12] and the synthesis and use of engineered strain relaxation areas[61] may be required for such efforts. In chapter IV we will explore the use of Ge/Si epitaxial layers to seed the growth of GaAs and potentially enable GaAs/Si or other III-V/Si devices. In Chapter III we address fundamental relationships between structure and performance of GaAs photoelectrodes.

CHAPTER III

ELECTROCHEMICAL NANOSTRUCTURING OF N-TYPE GALLIUM ARSENIDE PHOTOELECTRODES

Portions of this chapter were previously published as Ritenour, A. J.; Levinrad, S.; Bradley, C.; Cramer, R. C.; Boettcher, S. W. "Electrochemical Nanostructuring of n-GaAs Photoelectrodes" Energy Environ. Sci., 2013, 7, 8, 6840-6849. A. J. R. wrote the paper, made the figures, made the samples and performed the experimental work. R. C., C. B., and S. L. assisted with electrode fabrication and electrochemical measurements under the direction of A. J. R.. S. W. B. provided editorial assistance and was the principal investigator.

Introduction

Methods to simultaneously optimize carrier collection and light in-coupling in semiconductors are important for developing low-cost, high-efficiency photovoltaics and photoelectrodes. We anodically etched nanostructures into planar <100> *n*-GaAs wafers with different bulk minority carrier diffusion lengths L_D. The structures were varied by changing the anodization parameters. A ferrocene/ferrocenium electrolyte provided a conformal rectifying contact to the anodized *n*-GaAs and enabled the measurement of carrier generation and collection as a function of nanostructure geometry and L_D. Internal quantum efficiency Φ_{int} of photoelectrodes varied with nanostructure geometry and L_D. External quantum efficiency Φ_{ext} also depended on the reflectance of the

nanostructured GaAs-electrolyte interface. Reflectance was minimized using anodization current densities of 100-150 mA cm^{-2}, which etched sub-wavelength trigonal prismatic nanostructures ~400 nm in width at their base. For Si-doped n-GaAs with L_D = 170 nm, peak Φ_{ext} of ~75% and Φ_{int} of ~85% was achieved using J_{anod} = 150 mA cm^{-2}. Control of both surface nanostructure (to minimize reflection) and pore depth and spacing (to optimize 3D carrier collection) *via* two-step anodization yielded photoelectrodes with peak Φ_{ext} of ~85% and peak Φ_{int} of ~95% for Te-doped n-GaAs with bulk L_D of only 420 nm. The measured short-circuit current densities for the nanostructured photoelectrodes were up to 2.5 times that of planar controls, demonstrating that appropriate nanostructuring significantly improves carrier collection even for direct bandgap materials with large absorption coefficients like GaAs.

Understanding the interplay between nanostructure, optical reflectance (R), and carrier collection is important for the design of photoelectrochemical (PEC) and photovoltaic (PV) devices.[1-3] The ideal structure minimizes both light reflection at the surface and electron-hole recombination in the bulk.[4, 5] Bulk recombination occurs when light is absorbed in the semiconductor at a depth greater than the collection length, given by the bulk minority carrier diffusion length L_D plus the depletion width W, *i.e.* $L_D + W$ (Figure 3.1). One method to reduce bulk recombination is to increase L_D by using a material pure and free of defects, which contributes to the cost of the final device. For PV devices, R is reduced by anti-reflective coatings with optimized thicknesses and indices of refraction (n). For PEC applications, the requirement of direct solution-semiconductor contact precludes the use of such coatings (Figure 3.1). Therefore, architectures which

maximize optical in-coupling from low-*n* (solution or air) to high-*n* (semiconductor) media while simultaneously minimizing bulk recombination losses, and can be implemented without adding expensive or slow processing steps, are needed.

Three-dimensional (3D) structuring provides a mechanism to minimize *R*. For example, arrays of nanoscale cones and pillars nearly eliminate reflection from Si films.[3] This is caused by a gradient in the effective *n* at the air-semiconductor interface due to the sub-wavelength (λ) size and tapered nanostructure shape.[3] In the Si PV industry anisotropic wet etching of crystalline Si is used to provide pyramidal surface textures which reduce *R* of commercial PV devices.[6, 7]

Enhanced carrier collection in 3D radial-junction PV devices relative to planar ones has been modeled by Kayes *et al*.[4] The optical absorption coefficient $\alpha(\lambda)$ determines the depth to which photons are absorbed in the semiconductor, $\propto \alpha(\lambda)^{-1}$. When $L_D + W < \alpha(\lambda)^{-1}$, significant recombination losses occur (Figure 3.1). The optimal height

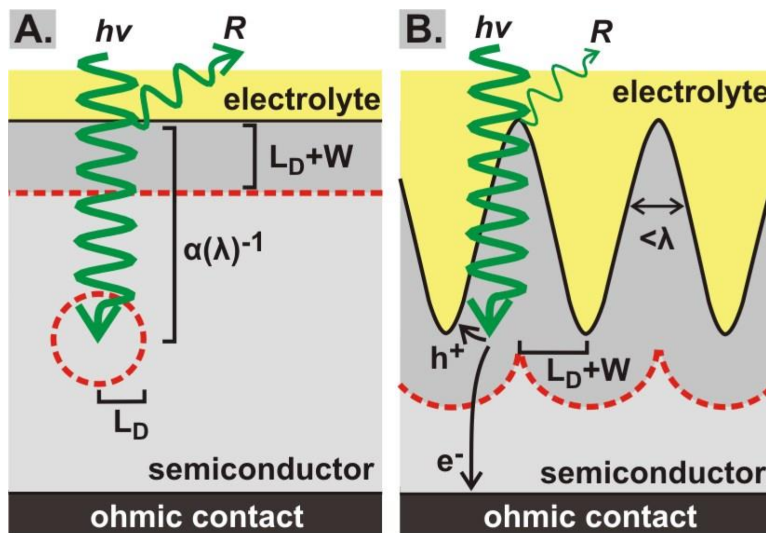


Figure 3.1. (A) In a planar photoelectrode significant bulk recombination losses occur when light is absorbed at a depth > $L_D + W$. (B) Lateral carrier collection in a nanostructured photoelectrode enables collection of minority holes that would otherwise recombine. Surface features with sub-λ dimensions also decrease *R* losses.

and spacing of the nanostructures are thus expected to depend on both $\alpha(\lambda)$ and $L_D + W$.[4] When $L_D + W >> \alpha(\lambda)^{-1}$, bulk recombination does not significantly affect the internal quantum efficiency (Φ_{int}). When $L_D + W < \alpha(\lambda)^{-1}$ (as is typical in many low-cost semiconductors) 3D structure has a large effect on Φ_{int}.[8] Because $\alpha(\lambda)$ decreases as the photon energy approaches the semiconductor bandgap E_g, it is expected that nanostructuring will yield the greatest improvement in Φ_{int} for photons with energy

slightly above E_g.For indirect bandgap semiconductors with long $\alpha(\lambda)^{-1}$ such as Si[9, 10] and GaP[11] the relationship between 3D structure and carrier collection has been studied in VLS-grown nano/microwire systems[2, 10] and nanostructures etched from single-crystal wafers using dry,[12] wet,[13-15] and electrochemical anodization processes.[16-18]

The correlation between 3D structure and photoelectrode performance in direct bandgap absorbers with short $\alpha(\lambda)^{-1}$, such as GaAs, has not been well explored. GaAs and related III-V compounds are important solar materials due to high mobilities (μ), high $\alpha(\lambda)$, and compositionally tunable bandgaps.[19] GaAs is of particular interest due to the demonstration of world-record single-junction PV devices with 1-sun $\eta = 28.8\%$,[20] as well as the ability to deposit solar-quality GaAs thin films by plausibly inexpensive and scalable vapor transport techniques.[21-24] Parkinson and coworkers showed that the photocurrent obtained from *n*-GaAs electrodes can be enhanced through a 'matte' etch using a H_2SO_4/H_2O_2 solution. The increased photocurrent was attributed to reduced R.[13] However, re-inspection of the published scanning electron microscope (SEM) images shows random roughening on the ~ 0.5 μm length scale which suggests that 3D carrier collection also likely contributed to improved carrier collection. Electrochemical anodization has also been shown to create nanoporous GaAs structures with a variety of

pore geometries,[25-28] but the influence of nanostructure on photoelectrode performance has not been explored. Recently MOCVD-grown epitaxial GaAs and other III-V nanowire/nanopillar array solar devices have been reported.[29-32] However, the variable surface and bulk properties of these materials make it challenging to separate the influences of R, bulk recombination, and surface defects on the measured photoresponse.

Herein we report a combined PEC and optical R study of nanostructured *n*-GaAs photoelectrodes created using electrochemical anodization. The surface nanostructure depth and coverage was controlled by adjusting the anodization current density (J_{anod}) and time (t) without using lithography.[25-28] Photoresponse was analyzed using a ferrocene/ferrocenium electrolyte which makes a conformal rectifying contact to *n*-GaAs.[22, 33, 34] The R of the air/glass/solution/GaAs interface was directly measured using an integrating sphere. We used two *n*-GaAs wafers with different L_D to study how the nanostructure's influence on Φ_{int} changes with L_D. A two-step anodization procedure[25, 26] was used to control pore depth and spacing, which allowed us to optimize surface nanostructure based on $\alpha(\lambda)$ and L_D. This study compliments the previous work on anodized indirect bandgap semiconductors and demonstrates that rational nanostructuring can dramatically improve performance of photoelectrodes even when fabricated from materials with direct bandgaps and high $\alpha(\lambda)$.

Methods

Sample Preparation

Ohmic back contacts (50 nm evaporated AuGe eutectic diffused at 450 °C for 90s in 5% H_2 95% N_2) were made to commercial <100>-oriented vertical-gradient-freeze

(VGF) grown n-GaAs wafers with different L_D. One wafer was doped n-type with Si (L_D = 170 nm, $N_D = 3\times10^{18}$ cm^{-3}) and the other was doped with Te (L_D = 420 nm, N_D = 7×10^{18} cm^{-3}). The samples were sealed in a custom PTFE cell containing 1 M sulfuric acid. The cell made a seal to the wafer surface with a compressed O-ring (inner area of 0.54 cm^2). Galvanostatic experiments were performed in two-electrode mode using a Biologic SP-200 potentiostat.

Figure 3.2 shows the voltage required to drive the anodization current from the n-GaAs working electrode to the Pt counter electrode, which is related to the series resistance of the cell, the voltage drop across the reversed biased n-GaAs solution interface, and the kinetic and mass transport resistances associated with GaAs oxidation at the working electrode and hydrogen evolution at the counter electrode. The area to be anodized was defined using a PTFE cell with a recessed O-ring. The defined area was 0.54 cm^2. The anodization current density is referred to as J_{anod}, while the applied bias is referred to as $V_{applied}$.

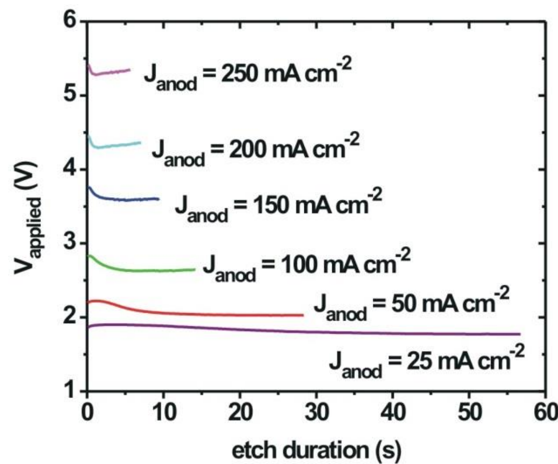


Figure 3.2. Applied potential versus the counter electrode during the galvanostatic anodization of n-GaAs samples as a function of J_{anod}.

J-E Characterization

Photoelectrodes utilizing planar and anodized *n*-GaAs were constructed using standard methods.[22] AuGe ohmic back contacts were attached to tinned-copper wires using silver paint and the wires were fed through glass tubes. The GaAs wafers were bonded to the wire/glass assembly and an active device area of ~ 0.03 cm^2 was defined with non-conductive epoxy (Loctite Hysol 9460). Electrode areas were individually measured with a digital scanner and ImageJ software. For *J-E* measurements, electrodes were immersed in an electrolyte containing 100 mM sublimed ferrocene, 0.5 mM recrystallized ferrocenium, and 1 M $LiClO_4$ (Alfa Aesar, 99%) in dry acetonitrile. All samples and controls were dipped in aq. 1 M HCl, rinsed with 18.2 M□ water and blown dry with N_2, immediately before all PEC and spectral response measurements to remove the native oxide.[45] *J-E* measurements were conducted in three-electrode mode under 100 mW cm^{-2} of AM1.5G solar simulation (Abet Technologies 10500). *J-E* curves were recorded at a scan rate of 20 mV s^{-1}. The counter electrode was Pt mesh and the reference electrode was a Pt wire poised at the solution potential positioned ~1 mm from the working electrode to minimize uncompensated series resistance. Hysteresis in the forward and backward *J-E* curves is likely related to chemical differences of the GaAs surface (*e.g.* surface charge) after the anodic and cathodic portions of the potential sweep. Hysteresis is typical for GaAs PEC measurements.[33, 34, 46]

Reflectance Characterization

The *R* of anodized GaAs samples was measured in an integrating sphere. We measured the air/GaAs interface, and the air/glass/acetonitrile/GaAs interface which is relevant to the PEC measurements (which were conducted in a glass cell containing

acetonitrile). The R of the air/glass/acetonitrile/GaAs interface was measured by placing a drop of acetonitrile between the etched GaAs surface and a glass slide and loading the assembly onto the integrating sphere.

SEM Characterization

The nanostructure of the anodized *n*-GaAs samples was characterized using a Zeiss Ultra-55 SEM with in-lens detector. Cross sections were prepared by cleaving the etched wafers and mounting the cleaved surfaces vertically in the SEM holder. The working distance was ~ 5 mm, and an accelerating voltage of 5 kV was used.

Spectral Response Determination of Φ_{ext}, Φ_{int}, and L_D

Spectral response was measured at short-circuit (0 V *vs.* Pt) using the electrolyte described above diluted by a factor of 1:10 with dry acetonitrile. The monochromatic light was chopped at 35 Hz and the nA-range signal was measured using a lock-in amplifier (Bentham PVE300). The chopped signal from samples and controls produced a signal free of transients with amplitude independent of chopping frequency in the range studied (Figure 3.3). The light intensity was measured using a calibrated Si reference photodiode (Bentham Si-11677) to determine Φ_{ext}. The Φ_{int} was calculated according to eq 5, where R is the normal-incidence R of the air/glass/acetonitrile/GaAs interface as discussed in section III. The calculation of Φ_{int} did not compensate for solution absorbance.

The values of L_D reported throughout were determined by fitting Φ_{int} of the planar wafers (Figure 3.4) to the Gärtner model of carrier collection over the region from550 - 870 nm which is nearly unaffected by solution absorbance:

$$\Phi_{\text{int}} = \left(1 - \frac{e^{-\alpha(\lambda)W}}{1+\alpha(\lambda)L_D}\right)$$

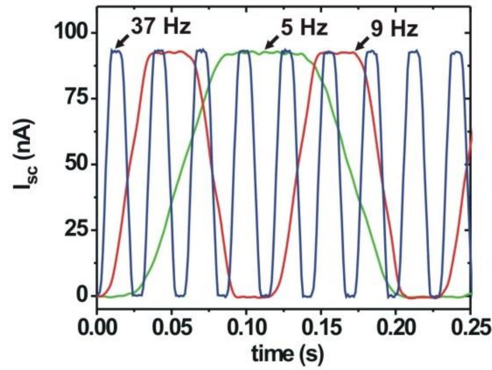


Figure 3.3. Chopped photocurrent of an electrode (sample Te-2.8) measured in the spectral response setup. The chopped photocurrent is free from transients and does not depend on chopping frequency below 37 Hz.

The Gärtner model assumes no recombination within the depletion width (*W*) and that recombination in the quasi-neutral region is governed by L_D.[47, 48] This technique yields values of L_D that are similar to those obtained by electron beam induced current measurements for *n*-GaAs.[49]

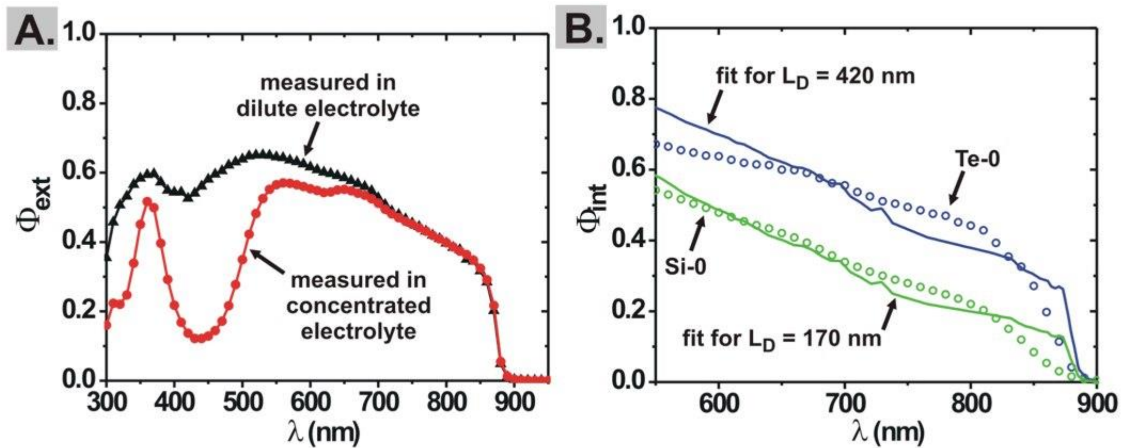


Figure 3.4. (A) The Φ_{ext} of an *n*-GaAs photoanode was measured both in concentrated electrolyte (used in AM1.5G *J-E* measurements) and diluted electrolyte (used in spectral response measurements) to show the solution absorbance. (B) The measured Φ_{int} and Gärtner model fits used to determine L_D of the two wafers used in this study.

Results and Discussion

Anodization and Structure Characterization

The use of anodization to form pores in GaAs is well-known.[25, 26, 28] Application of an oxidizing potential to *n*-GaAs causes tunneling breakdown[35] of the space-charge layer,[26] providing holes at the semiconductor surface which subsequently oxidize the Ga and As and form species which are soluble in acidic or alkaline solution.[36] Using this technique both J_{anod} and the voltage applied during anodization (V_{app}) have been shown to influence the crystallographic orientation[28] and density[25] of pores.

In this study, pores were etched into the *n*-GaAs wafers by passing an anodic galvanostatic current density (J_{anod}) through the 1 M H_2SO_4 electrolyte as shown in Figure 3.5. Based on the Pourbaix diagrams,[36] anodization of GaAs in 1 M H_2SO_4 at potentials greater than ~0.5 V *vs.* NHE is expected to yield aqueous Ga^{3+} and H_3AsO_4. We used a two-electrode anodization cell with the Pt counter electrode evolving H_2.

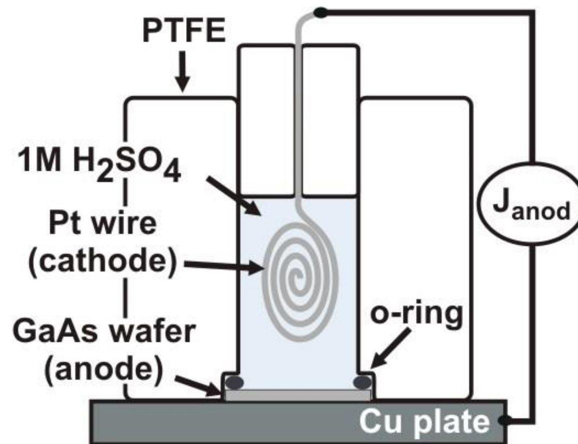
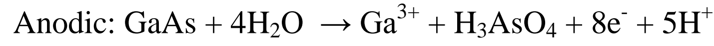
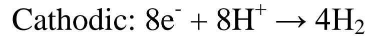


Figure 3.5. Schematic of the anodization cell used to fabricate nanostructured GaAs.

Because Pt is a good catalyst for H_2 evolution, the counter electrode potential is maintained near NHE. Given the observed range of V_{app} (1.8 - 5.4 V), the GaAs working electrode was undoubtedly positive of 0.5 V vs. NHE. The anodic etching and cathodic counter electrode reactions are thus given below.





Anodization parameters facilitated control of both the etch rate (which depends on J_{anod}) and the volume of material etched (v). As shown below, v depends on the charge passed per unit area, $Q = J_{anod} \cdot t$.

$$\mathrm{v} = \frac{QMA}{n_e q N_A \rho}$$

where t is the etch duration, M is the molecular weight of GaAs, n_e is the number of moles of electrons per mole of GaAs oxidized, q is the fundamental charge, N_A is Avogadro's number, and ρ is the density of GaAs.

Two wafers with different L_D (Si-doped GaAs with L_D = 170 nm and Te-doped GaAs with L_D = 420 nm) were used to investigate the relationship between nanostructure, Φ_{int}, and L_D. To study the effect of the etch rate on nanostructure, we adjusted J_{anod} and t (and measured V_{app}) while keeping Q constant at 1.4 C cm^{-2} (Table 3.1). From SEM analysis we find that as J_{anod} increased, the pore depth decreased (Figures 3.6 and 3.7). We note that samples prepared with $J_{anod} \leq 100$ mA cm^{-2} retained some planar areas on the surface. It has previously been shown that after a surface is covered with features to nucleate pores (such as etch pits[25] or surface texture[28]) a high pore density can be achieved by anodization. We thus also used a two-step anodization to fabricate samples having different pore depths while maintaining complete surface nanostructure coverage.

Table 3.1. Anodization parameters used to fabricate nanostructured GaAs.

Sample name	L_D (nm)	planar, 1-step or 2-step etch	J_{anod} (mA cm^{-2})	V_{app} (V)	t (s)	Q (C cm^{-2})	avg. pore depth (μm)
Si-0	170	planar	--	--	--	--	--
Si-25	170	1-step	25	1.8	56	1.4	1.7
Si-50	170	1-step	50	2.0	28	1.4	1.2
Si-100	170	1-step	100	2.6	14	1.4	0.6
Si-150	170	1-step	150	3.6	9.4	1.4	0.5
Si-200	170	1-step	200	4.4	7	1.4	0.3
Si-250	170	1-step	250	5.4	5.6	1.4	0.2
Te-0	420	planar	--	--	--	--	--
Te-50	420	1-step	50	2.6	28	1.4	4.0
Te-150	420	1-step	150	3.5	9.4	1.4	1.5
Te-1.4	420	2-step	150/50	3.5/2.5	3/20	1.4	3.2
Te-2.8	420	2-step	150/50	3.5/2.5	3/47	2.8	3.9
Te-4.2	420	2-step	150/50	3.5/2.5	3/74	4.2	5.6

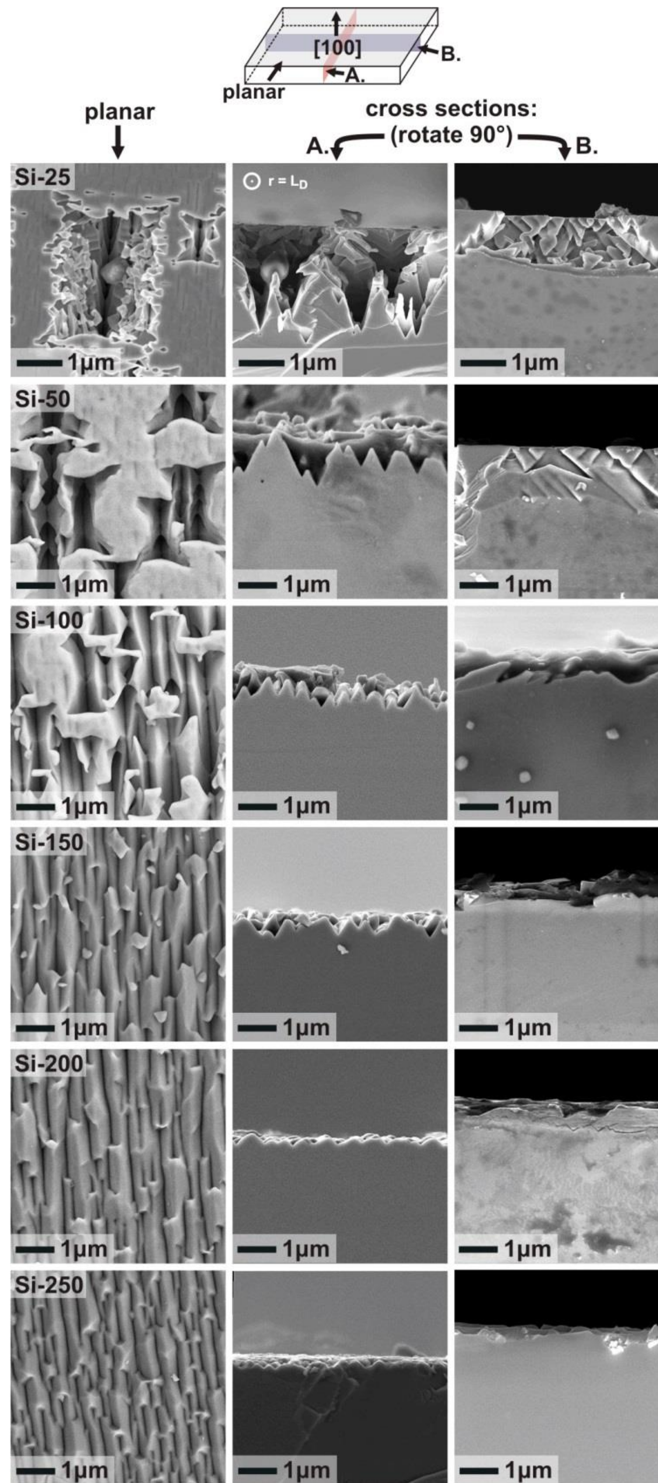


Figure 3.6. SEM micrographs of the anodized Si-doped (L_D = 170 nm) *n*-GaAs wafer viewed top-down (left column), in cross-section perpendicular to the long dimension of the pores (middle column), and in cross-section parallel to the long dimension of the pores (right column). The faces exposed in the two cross-sections belong to the {110} of family of planes.

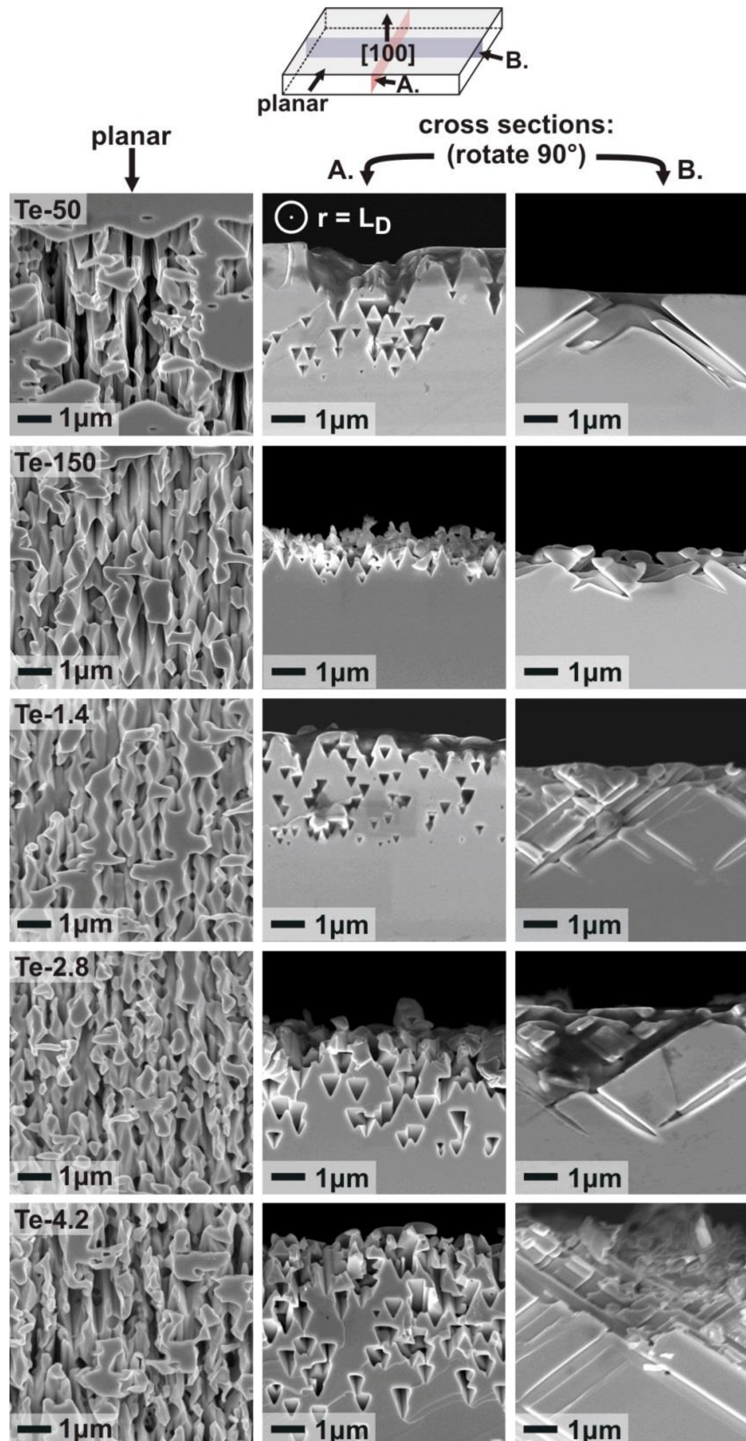


Figure 3.7. SEM micrographs of the anodized Te-doped (L_D = 420 nm) *n*-GaAs wafer viewed top-down (left column), in cross-section perpendicular to the long dimension of the pores (middle column), and in cross-section parallel to the long dimension of the pores (right column). The faces exposed in the two cross-sections belong to the {110} of family of planes.

The two-step anodization consisted of a brief pore nucleation step used to form a high density of shallow pores (J_{anod} = 150 mA cm^{-2} and t = 3 s) followed by a separate pore growth step used to deepen the existing pores (J_{anod} = 50 mA cm^{-2} and 20 s ≤ t ≤ 76 s) for which t was varied to change Q (see Table 3.1).[26] Throughout the text we refer to GaAs samples by the n-type dopant present in the wafer (Si or Te) and the relevant anodization parameter, *i.e.* the value of J_{anod} (in mA cm^{-2}) for samples anodized using one step, or the value of Q (in C cm^{-2}) for samples anodized using two steps (Table 3.1).

SEM analysis revealed that pores nucleated randomly across the surface but grew preferentially in the [111]B direction as has been previously observed by Föll and co-workers.[27] Figure 3.6 shows that the etching is more uniform and isotropic with a larger number of pores for increased J_{anod}. The etched nanostructures give rise to sub-λ trigonal prismatic features, which are expected to reduce R. The nanostructure depths of 0.2 - 5.6 μm are appropriate for studying lateral carrier collection based on the high $\alpha(\lambda)$ of GaAs.[37] These data suggest that anodization can be used to tailor n-GaAs nanostructures for solar devices, as we show below.

Photoelectrochemical Current-Potential Analysis

An electrolyte of ferrocene/ferrocenium in acetonitrile was used to provide conformal rectifying contacts to the n-GaAs photoelectrode (see Methods).[22, 33, 34] Current-potential (J-E) measurements were carried out under 100 mW cm^{-2} of AM1.5G solar simulation (1-sun) with rapid stirring to increase solution mass transport. All anodized samples showed improved short-circuit photocurrent (J_{SC}) relative to the planar n-GaAs controls (Figure 3.8). For anodized photoelectrodes Si-150 and Te-1.4, J_{SC} was

improved by 250% and 195%, respectively, compared to planar controls made from the same wafers (Si-0 and Te-0).

The measured fill factor (*ff*) provides further insight into the operation of the nanostructured *n*-GaAs photoelectrodes. Unlike PV devices, the *ff* of PEC devices is affected by a voltage loss associated with the concentration overpotential (η_{conc}) required to drive the diffusion of redox species from the bulk solution to the photoelectrode surface.[38] η_{conc} increases for the anodized samples relative to planar controls because the

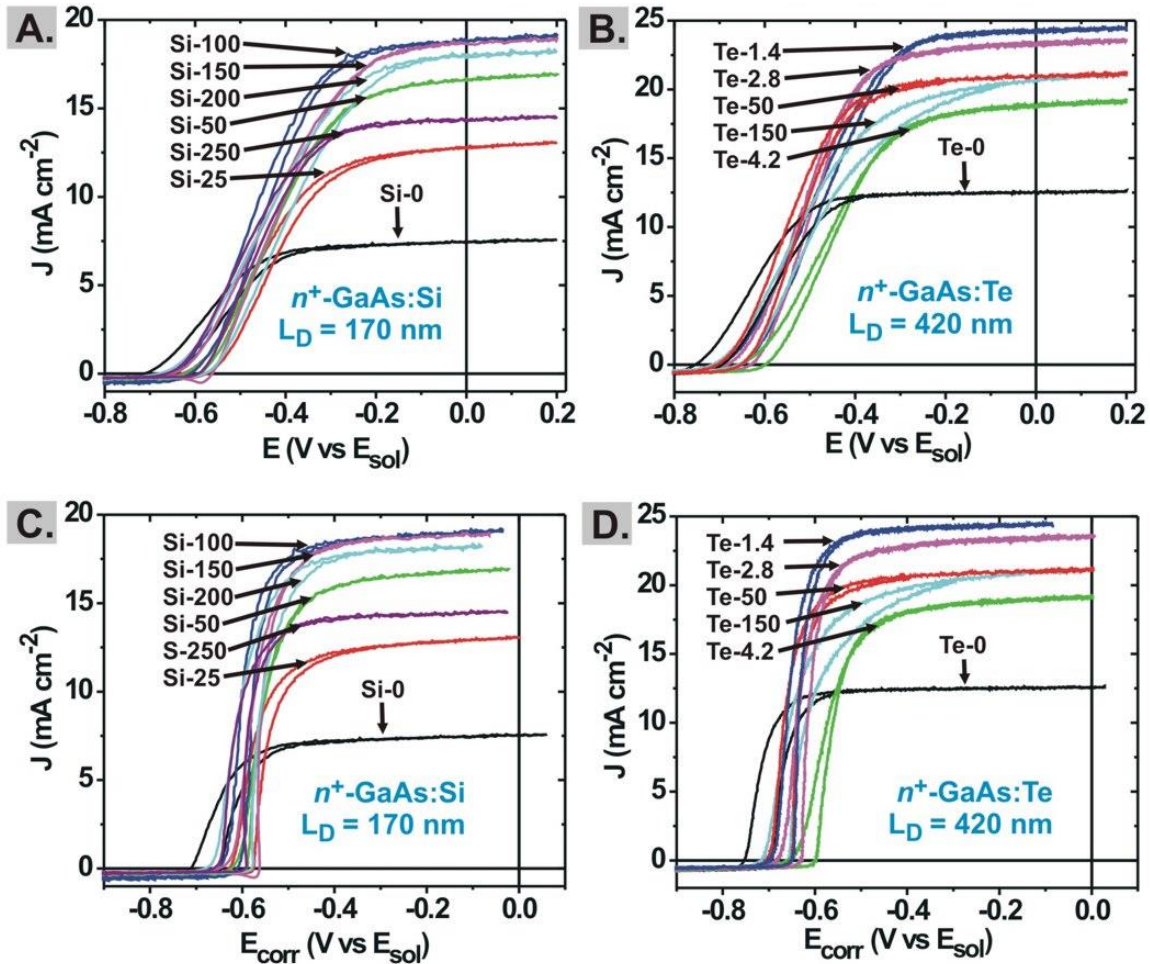


Figure 3.8. *J*-*E* curves of (A) anodized *n*-GaAs:Si (L_D = 170 nm) and (B) anodized *n*-GaAs:Te (L_D = 420 nm). The same data corrected for series resistance and concentration overpotential are shown in panels (C) and (D).

photocurrent is higher. Correcting for η_{conc} results in *ff* between 0.6 - 0.7 for all anodized samples, independent of J_{anod} and similar to the planar controls (Figure 3.8). This indicates that the *ff* in the uncorrected *J*-*E* data is affected by mass transport and series resistance losses inherent to the PEC technique and not due to degradation of the anodized *n*-GaAs relative to the planar controls. The series resistance and overpotential losses can be reduced by either using higher concentrations of redox couple and supporting electrolyte, or by using thin-layer electrolyte geometries.[39]

Optical Reflectance as a Function of Nanostructure

The *R* of each photoelectrode surface was measured to determine how much of the increases in J_{SC} can be attributed to changes in *R*. To measure *R*, we used an integrating sphere with a custom holder that incorporates GaAs, acetonitrile, and a glass slide to duplicate the interfaces present in the PEC cell (*i.e.* air/glass/acetonitrile/GaAs).

All anodized samples had lower *R* than the planar controls (Figure 3.9). Although increases in J_{SC} correlate with decreased *R*, the change in *R* by itself does not account for the amount of increase in J_{SC}. The *R* of the air/glass/acetonitrile/GaAs interface for planar controls is approximately 0.27. J_{SC} for anodized samples increased up to 250% relative to planar controls (Figure 3.8). Thus, the enhanced J_{SC} for anodized samples relative to planar samples is due to decreased bulk recombination (resulting from 3D carrier collection) in addition to the decreased *R*.

At normal incidence, *R* is expected to be independent of sample orientation. However, because the sample holder in the integrating sphere is 8° off-axis (Figure 3.9 (B) inset), *R* for the anodized GaAs was found to vary when the samples were rotated around the <100> direction (Figure 3.9 (B)). The etched nanostructures are anisotropic

with respect to rotation of the (100) plane (Figures 3.6 and 3.7) which results in the observed rotational dependence of *R*. The normal incidence *R* (for the purpose of calculating Φ_{int}) was approximated by averaging the *R* measured at 0° and 90° rotation

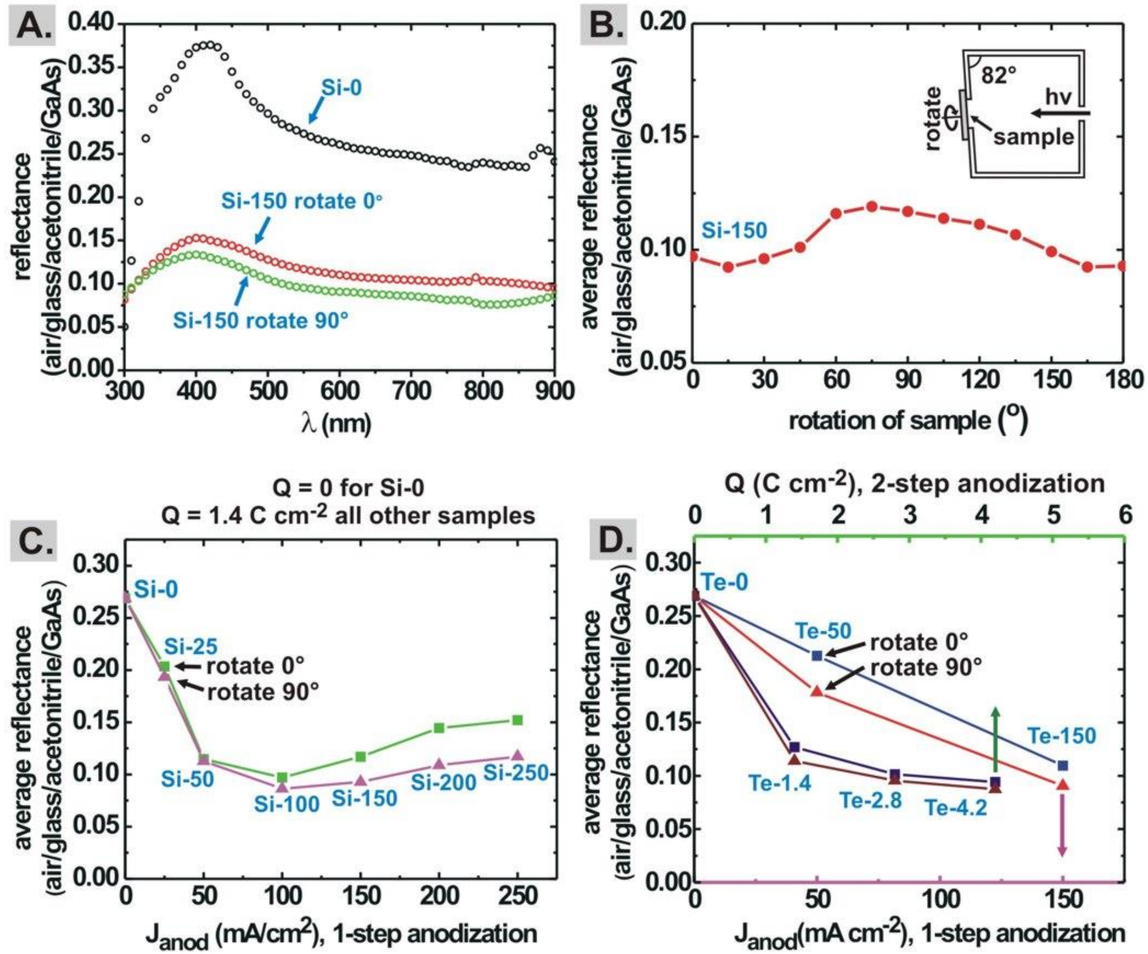


Figure 3.9. Measured *R* of the air/glass/acetonitrile/GaAs interface for all samples. (A) Reflectance of a planar GaAs control and sample Si-150 rotated 0 and 90°. (B) Average reflectance (300 nm < λ < 900 nm) of sample Si-150 measured as a function of rotation of the (100) surface. The inset depicts the sample position in the integrating sphere. (C, D) Average reflectance over λ = 300 - 900 nm for planar and anodized samples demonstrating the effects of J_{anod}, *Q*, and rotation on *R*. For 6D, the bottom axis is for samples anodized with 1 step (Te-50 and Te-150) and the top axis is for samples anodized with 2 steps (Te-1.4, Te-2.8, and Te-4.2).

(Figure 3.9 B inset). The error in this approximation is small and of the same order as the error resulting from slight deviations from normal incidence encountered when making the physical electrodes, clamping the PEC cell in place, and positioning the solar simulator, and was therefore neglected.

The R of samples decreased with increasing J_{anod} until reaching a minimum at J_{anod} = 100 mA cm^{-2} and then increased up to J_{anod} = 250 mA cm^{-2} (Figure 3.9). For samples Te-1.4, Te-2.8, and Te-4.2, which were etched using the two-step process, we observed a slight decrease in R as Q was increased (Figure 3.9). The trends in R are consistent with analysis of the SEM images. The surfaces of the lowest R samples consist of V-shaped pores ~0.5 μm deep with sub-λ lateral dimensions. The highest R samples all possessed either pores shallower than λ or unetched flat regions (see Figures 3.6 and 3.7), both of which present an abrupt change in n for incident photons and thus increased R at the semiconductor/solution interface relative to the optimally-etched samples.

Minority Carrier Collection

To understand the influence of nanostructure on the collection of photo-generated minority carriers, we measured the external quantum efficiency (Φ_{ext}) (Figure 3.10 (A) and (B)) and corrected it for R to obtain the internal quantum efficiency (Φ_{int}):

$$\Phi_{\text{int}} = \frac{\Phi_{ext}}{1-R} \tag{4}$$

If changes in J_{SC} were solely due to decreased R of the anodized GaAs, Φ_{int} would be identical for all samples. However, the Φ_{int} of anodized samples is higher than the Φ_{int} of planar controls. Thus increased J_{SC} for the anodized samples is due not only to reduced R, but also due to improved collection of minority carriers, particularly of those generated by photons with energy slightly above E_g (Figure 3.10 (C) and (D)). The combination of

the enhanced optical in-coupling and carrier-collection results in significantly increased Φ_{ext} for the anodized samples relative to the planar controls Si-0 and Te-0. Over the range of nanostructures explored, the relative improvement from control to anodized samples was greatest for Si-doped GaAs with L_D = 170 nm. The Φ_{ext} was highest, however, for the optimally anodized Te-1.4 which had a longer L_D = 420 nm.

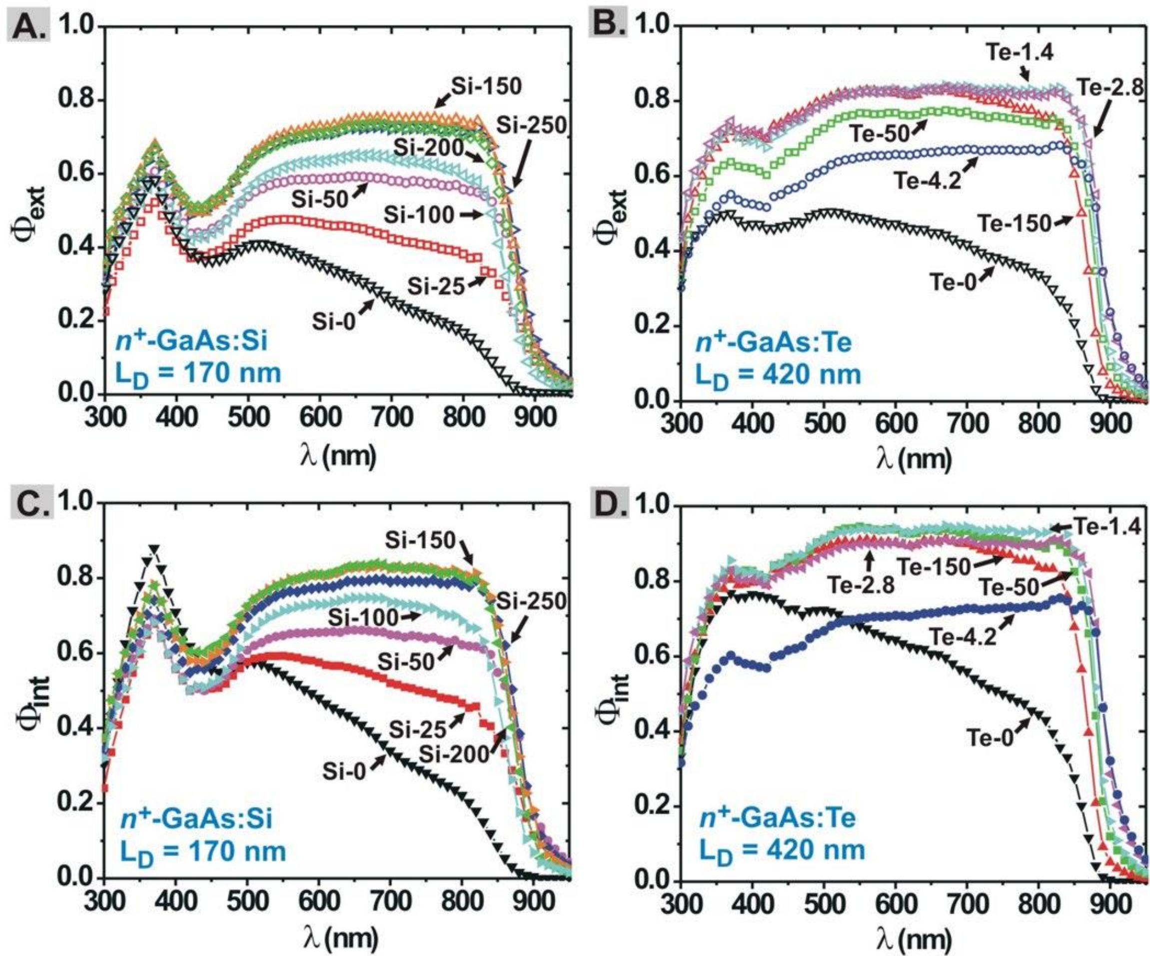


Figure 3.10. External quantum efficiency Φ_{ext} for n-GaAs with (A) L_D = 170 nm and (B) L_D = 420 nm. Internal quantum efficiency Φ_{int} for n-GaAs with (C) L_D = 170 nm and (D) L_D = 420 nm.

Overall Photoelectrode Structure-Performance Trends

Observed trends in R, Φ_{ext}, and J_{SC} are plotted as a function of the anodization variables J_{anod} and Q in Figure 3.11. The observed trends in R are consistent with enhanced optical in-coupling due to the v-shaped sub-λ nanostructures observed *via* SEM. The trends in Φ_{ext} are the result of enhanced light absorption and decreased bulk recombination due to 3D carrier collection.

To check the consistency of the quantum efficiency and *J-E* data, Φ_{ext} was used to calculate the expected J_{SC} under 1-sun illumination ($J_{SC,calc}$) by integrating the product of the solar flux and Φ_{ext} over all photons with energy > E_g = 1.42 eV. Trends in $J_{SC,calc}$, J_{SC}, wavelength averaged normal-incidence R in air, and wavelength average normal-incidence R of the air/glass/acetonitrile/GaAs interface are compared in Figure 3.11. The values of $J_{SC,calc}$ are 2-3 mA cm^{-2} higher than J_{SC} measured under 1-sun illumination. This discrepancy is due to light absorption by the concentrated electrolyte used in the 1-sun measurements, which was required to sustain the mA-range photocurrent. In contrast, Φ_{ext} was determined from nA-range photocurrent measurements, which made it possible to reduce the concentration of the light-absorbing electrolyte by diluting 1:10 with dry acetonitrile. Re-measuring Φ_{ext} in undiluted electrolyte yielded values of $J_{SC,calc}$ within +/- 0.5 mA of the observed J_{SC} (Figure 3.4 (A)). Therefore, the 1-sun J_{SC} attainable in optimized cells without parasitic electrolyte absorption is expected to be 2-3 mA higher than what was measured here.

Besides Φ_{ext} and *ff*, the photovoltage is an important performance metric. At constant light flux, the ideal diode equation predicts that the photovoltage will decrease by 59 mV times the diode ideality factor n_{dio}, per order-of-magnitude increase in charge-

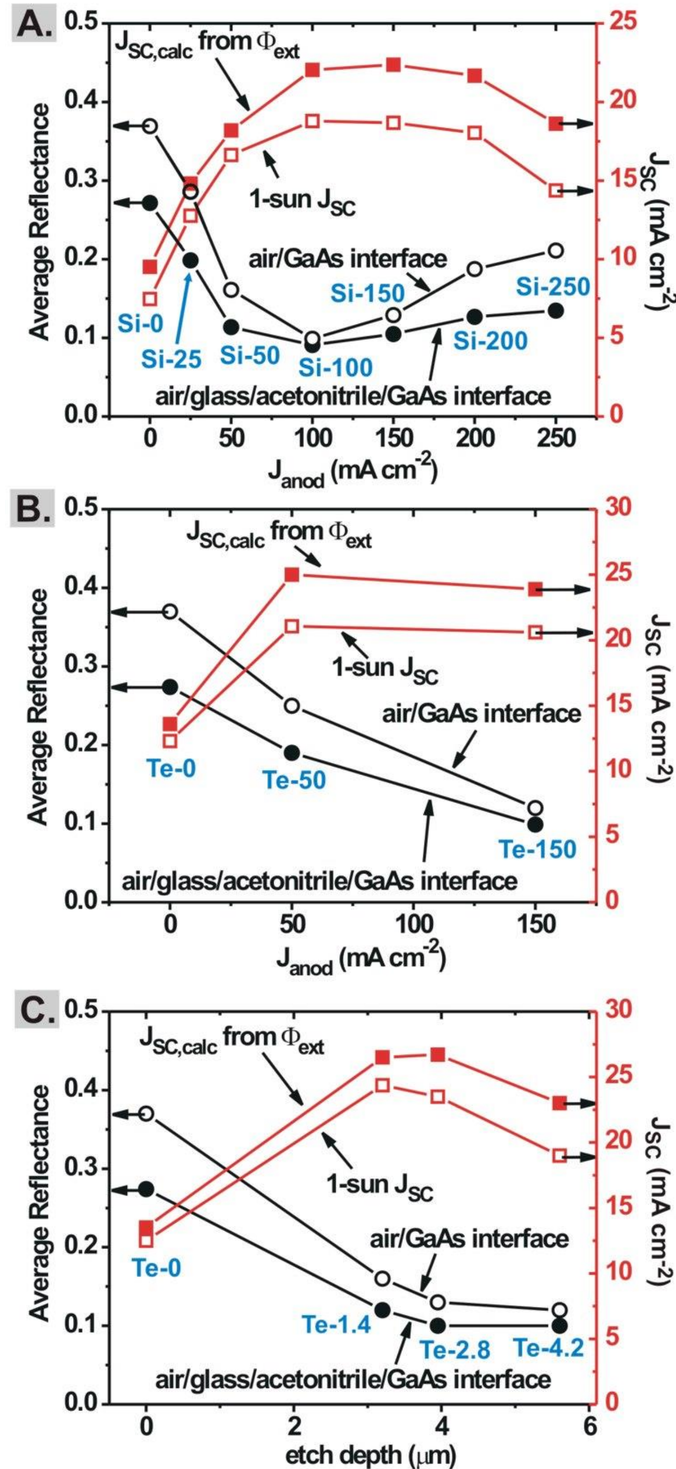


Figure 3.11. Trends in photoelectrode response as a function of anodization parameters. On each panel is plotted: J_{SC} calculated from Φ_{ext} measurements, J_{SC} under AM1.5G solar simulation, average R in air, and average R of the air/glass/acetonitrile/GaAs interface. (A) Samples Si-0 through Si-250 (one-step anodization). (B) Samples Te-0 through Te-150 (one-step anodization). (C) Samples Te-0 through Te-4.2 (two-step anodization).

separating junction area, in this case the area of the electrode-electrolyte interface.[1, 4] As expected, the anodized samples exhibited lower photovoltages than planar controls. Based on SEM cross-sections, the roughness factor of the anodized Si-doped *n*-GaAs samples range from 1.3 (Si-25) to 2.5 (Si-150). Based on this increased junction area, the predicted decrease in photovoltage should be 7 mV to 25 mV times n_{dio}. The observed photovoltages decreased by 20 mV to 50 mV relative to the planar controls, suggesting $n_{dio} \approx 2$.

Sample Te-1.4 was etched *via* the two-step anodization and had the highest Φ_{int} measured, 0.94 at λ = 830 nm, despite having L_D = 420 nm, which is short relative to $\alpha(\lambda)^{-1}$. This represents a 2.8-fold Φ_{int} enhancement relative to the planar control Te-0. This near-ideal structure, which was introduced without lithography *via* potentially inexpensive and rapid anodization, had pores with almost ideal spacing of ~ $2\times L_D$ and depth > $\alpha(\lambda)^{-1}$ (Figure 3.1). Further increases to Φ_{ext} could be achieved by treating the glass/air surface ($R \approx 0.04$) with an anti-reflective coating. For comparison, Te-150 was etched with a one step anodization and showed similar Φ_{int} to Te-1.4, except for λ between 800-900 nm where deeper pores in Te-1.4 provide 3D carrier collection pathways for weakly-absorbed photons (photons having energy near E_g). Te-4.2, which had pores roughly twice as deep as Te-1.4, showed significantly lower Φ_{int} for all λ, which is inconsistent with the simple radial junction model.[4] Figure 3.7 shows that Te-4.2 also contained smaller near-surface features (*e.g.* < 50 nm) than Te-1.4 after the longer etching process. Photogenerated minority carriers in such features smaller than the depletion width (here ~ 40 nm) may be subject to increased recombination.[9] The highest Φ_{int} for the Si-doped samples was ~0.82. The Φ_{int} for the Si-doped samples is likely lower

than for the Te-doped samples because the natural dimensions of the etched nanostructures are larger than $2\times L_D$, and because of increased depletion-region recombination (due to the lower L_D).

Conclusion and Bridge

We have demonstrated the use of electrochemical anodization to introduce controllable surface nanostructure in *n*-GaAs photoelectrodes. Preferential etching in the [111]B direction[26] gives rise to triangular prismatic pores which result in reduced *R*, as predicted by effective medium theory and discussed by others.[2, 3] Internally consistent *R*, *J*-*E*, Φ_{int}, Φ_{ext}, and SEM analysis indicate that the high J_{anod} needed for low *R* interfaces is not suitable for making deep pores, as the surface is etched nearly as fast as the pore bottoms, possibly due to mass-transport limitations or a change in etching anisotropy.[28] Thus, moderate J_{anod} = 150 mA cm^{-2} led to effective optical in-coupling and low *R* but did not yield the highest Φ_{int} for GaAs with $L_D < \alpha(\lambda)^{-1}$. Low J_{anod} resulted in pores with controllable depth, but the barrier for nucleation of new pores prevented uniform texturing of the planar surface and resulted in relatively high *R*. A two-step anodization consisting of a high J_{anod} pore nucleation step and a low J_{anod} pore growth step was used to circumvent this problem and found to be optimal.

The methods reported here could have impact in several areas. The performance of low-cost GaAs deposited on foils or other substrates[40-43] could be substantially improved by controllably anodizing to reduce *R,* introduce nanostructuring at a length-scale appropriate for the material quality, and reduce the influence of grain boundaries. The performance of GaAs photoelectrodes possessing $L_D > \alpha(\lambda)^{-1}$, such as those deposited

by close-spaced vapor transport (CSVT),[22-24] could be improved by anodization at high-J_{anod} to introduce surface nanotexture optimized to minimize R. If applied as water-splitting photoelectrodes (after protection of the GaAs surface and incorporation of an electrocatalyst),[44] the decrease in photovoltage caused by increased junction area is expected to be compensated by the reduction of kinetic overpotential due to increased catalyst surface area.[1]

CHAPTER IV

GALLIUM ARSENIDE FILMS GROWN BY CLOSE-SPACED VAPOR TRANSPORT ON GERMANIUM-ON-SILICON SUBSTRATES

Portions of this chapter are being prepared for publication as Ritenour, A. J.; Nellist M. R.; Bachman, Bachman B. F.; Wood S. R.; Boettcher S. W. "Gallium Arsenide Photoelectrodes on Si Substrates Prepared by Close-Spaced Vapor Transport." Under A. J. R.'s direction M. R. N. and B. F. B. assisted with sample preparation and measurements. A. J. R. made the figures, wrote the manuscript, and developed the overall methodology. S. W. B. provided editorial assistance and was the principal investigator.

Introduction

GaAs has many properties desirable in a photovoltaic such as high absorption coefficient,[1] high carrier mobilities,[2] and the ability to efficiently dope both n- and p-type films.[3, 4] Owing to these properties, gallium arsenide solar cell efficiencies approach the single junction limit.[5] However, use of gallium arsenide photovoltaics for grid-connected applications remains cost prohibitive.[6] This is due in part to the cost of depositing films by metal-organic chemical vapor deposition (MOCVD) and also in part to the high cost of suitable substrates such as GaAs or Ge. GaAs can be grown by plausibly low-cost processes like close-spaced vapor transport (CSVT), but a suitable means to lower the substrate cost must also be found. The substrate cost could be amortized by reuse of the substrate via epitaxial lift-off or spalling,[7] but this process has not yet been demostrated to produce GaAs solar cells that are cost-competitive with conventional Si or CdTe solar

cells. The cost/watt of the substrate cost can also be reduced by concentrating light on the solar cell. However, concentrated photovoltaics require complex high efficiency multi-junction architectures, light-tracking mounts, and direct sunlight. Thus an inexpensively deposited (e.g. by CSVT), non-concentrating GaAs solar cell grown on an inexpensive substrate is desirable. Si is especially interesting as a substrate for GaAs epitaxy since a tandem photovoltaic utilizing a highly efficient, low-cost III-V GaAs-based top cell with band gap $E_g = 1.7$ eV deposited on a Si solar cell Eg = 1.1 eV base has a nearly optimal two-junction theoretical limiting efficiency ($\eta = 38\%$).[8]

Si is widely used in photovoltaics and is a relatively inexpensive single-crystal material, but there are numerous challenges to achieving high quality heteroepitaxial GaAs/Si films. The main challenge for high-quality GaAs/Si heteroepitaxy is the 4% lattice mismatch between GaAs and Si, which causes a high density of threading dislocations for heteroepitaxial GaAs/Si films.[9] This can be addressed by nanopatterning, which reduces the strain below the critical threshold for dislocation formation,[10] but nanopatterning is costly and not ideal for large-area high-throughput processes. Second, the thermal expansion mismatch of Si and GaAs results in cracking of GaAs/Si films when the sample is cooled from the growth temperature. Third, if CSVT is to be used as the deposition process, SiO_x easily forms under the growth conditions (because H_2O is used as a transport agent), preventing epitaxial growth of GaAs on Si. Fourth, since Si is a nonpolar semiconductor material and GaAs is a polar semiconductor, the formation of antiphase domains (APD's) during growth may occur.[11] The primary effect of defects such as APD's and threading dislocations is an increase in the dark current, resulting in

decreased fill-factor (ff) and open-circuit voltage (V_{OC}), however the short circuit current (J_{SC}) is minimally affected.[12]

Ge is more amenable than Si for CSVT deposition of GaAs.[13] The 0.4% lattice mismatch is relatively small, as is the thermal expansion coefficient mismatch. Unlike SiO_x, GeO_x is voltatile meaning that under CSVT growth conditions an oxide layer does not form. Indeed, specular films of GaAs/Ge wafers have been obtained using CSVT and exhibited X-ray diffraction (XRD) patterns indestinguishable from homoepitaxial GaAs films, indicating similar crystalline order.[14] Although Ge wafers are cost-prohibitive as a substrate, thin layers of Ge can be inexpensively placed on an inexpensive substrate (such as Si, ceramic, or metal foil) to create a so-called "virtual Ge" substrate.[15] Ge can be deposited on Si by a variety of techniques including thermal evaporation,[16] sputtering,[17, 18] chemical vapor deposition,[19] or CSVT.[20] These films can be crystalline as deposited[21, 22] or the film may be amorphous as deposited and crystallized in a subsequent step.[18, 23, 24] The quality of the Ge film is generally assessed by measuring the threading dislocation density (TDD), the surface roughness, and the lattice strain.[25] Treatments such as thermal annealing,[26] two-step growths with low nucleation and high growth temperatures,[19] laser annealing,[27] and cyclic annealing[28] have all been shown to improve the quality of Ge/Si films by reducing the TDD from ~10^{10} cm^{-2} to as low as ~10^{6} cm^{-2}.[25] Thermal treatments decrease the threading dislocation density near the surface of the Ge layer by enabling dislocations to glide to edges and annihilate. This effect can be further enhanced by patterning the Ge into "islands" less than 40 μm in size, substantially increasing the edge-to-area ratio.[19] A Ge island pattern of this scale would also serve to reduce the tensile

strain of a GaAs layer grown on a Ge/Si substrate at ~800 °C and cooled to room temperature to below the critical threshold for crack formation.

Here we report synthesis of Ge/Si virtual substrates and their use as substrates for CSVT GaAs deposition. The crystallinity of the Ge films was assessed using high-resolution XRD and Raman spectroscopy. GaAs was deposited on the virtual substrates by CSVT from solid sources using H_2O as a transport agent.[3, 29, 30] The optoelectronic properties of these GaAs/Ge/Si structures were measured using standard photoelectrochemical techniques. We discuss the results in the context of our ultimate goal of fabricating low-cost III-V/Si tandem photovoltaic devices.

Methods

Ge/Si Epitaxy

Prior to deposition of Ge, wafers of single-side-polished (100)-oriented n-Si:As were cleaned by piranha, rinsed with 18.2 MΩ water, rinsed with high performance liquid chromatography (HPLC) -grade isopropyl alcohol (IPA), and spin-dried on a vacuum chuck (3000 rpm). For epitaxial deposition, the native oxide was removed by HF treatment with 20:1 buffered oxide etch (BOE), the wafers were rinsed with 18.2 MΩ water and immediately immersed in HPLC-grade ethanol in order to preserve oxide-free surface while transporting the wafers to the deposition system. The wafers were then blow-dried (N_2) and mounted on a custom stage equipped with cartridge heaters and a thermocouple. The oxide removal step was omitted in order to produce polycrystalline control samples. The deposition chamber was pumped to 2×10^{-6} mBar and the stage was heated to 350 °C, which was maintained with an Omega PID temperature controller. The

Ge was deposited on the polished Si face to a thickness of 200 nm at a rate of 2 Å s^{-1} as monitored with a quartz crystal microbalance. The film thickness was verified by measuring the Ge edge thickness on a Dektak stylus profilometer.

Patterning Ge Islands

Ge islands were produced using photolithography (Figure 4.1). A negative photoresist was used (AZ5214) for this step. After patterning the Ge was removed from exposed regions in the pattern by etching with a solution of 50:1:0.1 H_2O, NH_4OH, H_2O_2. The photoresist was then removed by sonicating in HPLC-grade acetone for 2 min, rinsing with HPLC-grade IPA, and spinning until dry on a vacuum chuck (3000 rpm). Cyclic annealing was conducted after patterning in order to reduce threading dislocation density and provide a better surface for GaAs epitaxy.

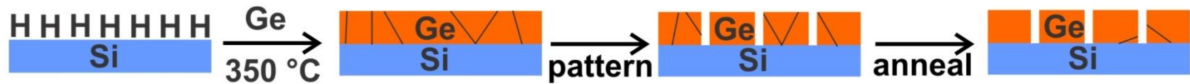


Figure 4.1. Diagram indicating how the patterned virtual Ge substrates were fabricated. The Ge is deposited on H-terminated silicon at 350 °C, patterned using photolithography, and annealed to reduce the dislocation density.

Annealing Virtual Ge Substrates

Substrates were placed in a 25mm diameter quartz tube which was pumped to a pressure of 5×10^{-7} mBar using a turbopump (Pfeiffer HiCube 80). The substrates were heated to the desired temperature in a tube furnace (Lindberg Blue) using a 1 hour ramp, the temperature was held for 5 min, and then cooled to room temperature. Cyclic annealing was done by cycling (with 1 hour ramps) between 200 °C and 800 °C five times. Samples were held at 800 °C for 5 minutes before initiating the cooling ramps.

GaAs Deposition

GaAs was deposited in a CSVT reactor comprised of two PID-controlled resistive heaters housed in a quartz tube equipped with hydrogen mass flow controllers. One mass flow controller was connected to a sealed H_2O bubbler to control [H_2O]. The [H_2O] was monitored with a hygrometer (Panametrics MMS). The CSVT system was the same system used in our previous publications. Dopants were not intentionally introduced, but generally CSVT GaAs films in our system incorporate ~ 3×10^{16} cm^{-3} of S, which is an n-type dopant. Furthermore we expect Ge from the substrate to transport into the GaAs film both by evaporation and co-deposition, and by diffusion. Ge is also generally an n-type dopant in GaAs.

Electrode Fabrication

Samples were cleaved into ~0.1 cm^2 squares. Ohmic contacts to Si were made using GaIn eutectic which was scratched into the Si with a diamond scribe. A wire was attached using Ag paint (Ted Pella). The wire was fed through a 6mm diameter glass tube and the edges were sealed to the tube with non-conductive epoxy (Hysol 1C). The face of the electrode was defined using black non-conductive epoxy (Hysol 9460), revealing a round area of sample with area ~0.05 cm^2. Electrode area was measured using a digital scanner and ImageJ software.

Reflectance Measurements

Reflectance ($R(\lambda)$) of the air|glass|acetonitrile|GaAs stack was measured on a UV-Vis spectrometer equipped with an integrating sphere (Perkin-Elmer).

Photoelectrochemical Measurements

Rectifying contacts were made to n-GaAs by immersing it in an electrolyte

consisting of 1 M $LiClO_4$, 100 mM ferrocene, and 0.5 mM ferrocenium in dry acetonitrile. This electrolyte is known to yield reasonable PEC performance for n-GaAs. 100 mW cm^{-2} of AM1.5 illumination was provided by a solar simulator (Abet 10500). A Pt wire poised at the solution potential was used as a reference electrode. Measurements were recorded using a potentiostat (BioLogic SP300).

Spectral response was carried out using a Bentham PVE300 spectral response system. The electrodes were immersed in diluted (1:10) electrolyte used for the 1-sun PEC measurements. The light source was chopped at 50 Hz, a potentiostat was used to confirm the absence of transients. The chopped nA-range signal was measured using a lock-in amplifier and converted to external quantum efficiency (Φ_{ext}) with the aid of a calibrated photodiode with known responsivity (Bentham Si11677). Φ_{ext} was converted to internal quantum efficiency (Φ_{int}) using:

$$\Phi_{\text{int}} = \frac{\Phi_{ext}}{1 - R(\lambda)}$$

Results

Deposition of Ge on Si

All films were mirror-like as deposited. The crystalline character varied according to the temperature of the substrate and whether the silicon was coated with a native oxide or hydrogen-terminated. Deposition of Ge on hydrogen-terminated Si at ambient temperature (~20 °C) yielded amorphous films. Increasing the substrate temperature to 350 °C provides sufficient energy for the Ge atoms to rearrange into a crystalline film in a layer-by-layer growth and yields epitaxial films. Depositing Ge on oxide-terminated substrates at 350 °C yielded polycrystalline films. These results were confirmed using X-ray diffraction[22] and

RAMAN spectroscopy.[16] The FWHM of the XRD rocking curve (Figure 4.2) and the shape and position of the RAMAN signal (Figure 4.3) are consistent with the literature and suggest These Ge epilayers possess ~10^6 cm^{-2} threading dislocation density.[16, 22]

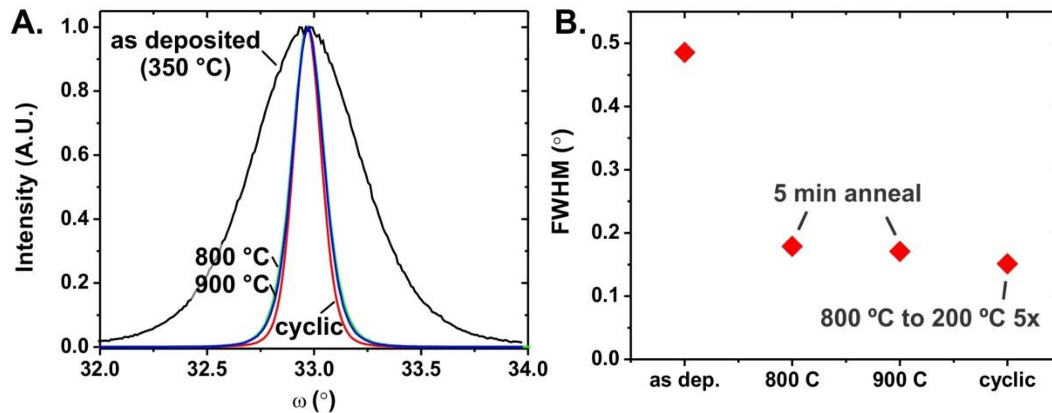


Figure 4.2. (A) XRD rocking curve of the Ge (400) line indicating highly-oriented Ge epitaxial layers. The FWHM of the peak decreases as a function of annealing temperature and is the smallest for cyclic annealed samples. (B) FWHM of the XRD rocking curves as a function of the anneal conditions.

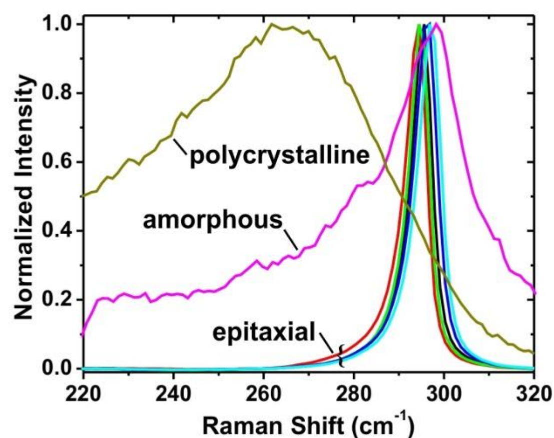


Figure 4.3. RAMAN spectroscopy of the Ge on Si virtual substrates. The narrow peaks indicate epitaxial Ge on Si. The broad peaks are indicative of amorphous or polycrystalline Ge, as indicated. These results are similar to those shown in the literature.

Growth of Epitaxial GaAs on Ge on Si Substrates

GaAs growth on the Ge substrate was achieved with a relatively large supersaturation. For epitaxial growth the difference between the source and substrate temperatures can be as low as 10 °C. In order to grow GaAs on Ge, 50 °C difference in temperature between source and substrate was required. This is due to the difference in lattice constants, which causes growth of GaAs on Ge less energetically favorable than growth of GaAs on GaAs. For this reason, once GaAs is nucleated on the Ge patterned regions, the GaAs epitaxial growth is favored over GaAs on Ge growth, leading to growth of individual crystallites rather than smooth GaAs/Ge films (Figure 4.4). GaAs deposition is almost entirely limited to the Ge patterned areas and very little nucleation is observed on the SiO_x surface.

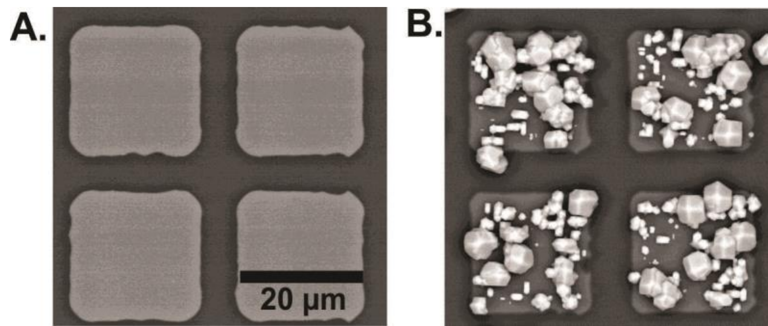


Figure 4.4. (A) SEM image of patterned Ge on Si after cyclic annealing. (B) SEM image of GaAs deposited on the annealed, patterned substrate in A. Crystals are faceted and anisotropic suggesting epitaxial growth.

Discussion

We have demonstrated a method of fabricating Ge patterned regions on Si substrates using standard semiconductor processing tools and a thermal evaporator. Analysis of the Ge by XRD and RAMAN layers indicate epitaxial growth with

about ~10^6 cm^{-2} threading dislocation density. In addition, the Ge layers appear smooth and free of surface defects by SEM analysis.

The deposition of GaAs by CSVT on these virtual Ge substrates has not yet been optimized. Crystallite growth is favored over smooth film growth due to the lattice mismatch of Ge and GaAs. Film growth could be promoted by increasing the supersaturation via increasing the temperature difference between the source and substrate, thereby decreasing the diffusion of Ga and As species on the Ge surface and causing them to deposit in a layer-by-layer manner.

Outlook

GaAs or other III-V semiconductors on Si could be potentially useful as either tandem photovoltaics or as photoelectrodes. Optimizing the growth parameters to yield smooth GaAs surfaces that are amenable to deposition of rectifying p-doped GaAs films would potentially enable fabrication of GaAs photovoltaics on Si substrates. This could be achieved by reducing the size of the Ge mesas to accommodate a single GaAs crystal per mesa. Optimizing the CSVT deposition parameters to prioritize GaAs crystal growth over nucleation could result in one GaAs crystal per Ge mesa yielding a GaAs-covered Si surface with zero grain boundaries. Further optimization of the Si|Ge|n-GaAs interface to form a tunnel junction will be required to eventually realize the goal of creating tandem III-V/Si photovoltaics. For this eventual goal careful management of the thermal treatment steps may be necessary to minimize thermal diffusion of dopants in the Si solar cell, which could degrade performance of the underlying Si pn junction solar cell.

A new CSVT reactor which possesses the capability to sequentially deposit multiple differently-doped layers of GaAs without opening the system to atmosphere may be required to achieve pn junction GaAs solar cells with V_{OC} exceeding 900 mV. Contamination by native oxide growth, dust, and other sources of contamination (e.g. adventitious hydrocarbons) introduced between subsequent growths using the CSVT apparatus described in this document are likely to contribute to electronically active defects which degrade the open circuit voltage. It seems likely that a new CSVT reactor design which does not depend on close spacing of source and substrate provided by a physical spacer (in this case a quartz ring) must be adopted to enable sequential deposition of layers.

A sublimation process similar to what is utilized for depositing the CdTe layer in CdTe solar cells could potentially be applied to GaAs deposition. In the CdTe process powder precursors are evaporated and carried by a stream of hot gas. The gas carries the vapor phase species to a cooler substrate where they deposit as polycrystalline CdTe. In the GaAs system, this could be achieved by a carrier gas which contains a small amount of a transport agent (e.g. HCl, H_2O, or $ZnCl_2$) needed to etch and volatilize the Ga. Using this technique, the substrate could easily be moved and positioned beneath different sources of powdered III-V's containing different dopants (if the source and dopants were held behind or under a quartz frit) in order to grow pn junctions or potentially different compositions (e.g. InGaP) to enable passivation of the GaAs solar cells.

Halogen containing transport agents are corrosive and potentially more hazardous than H_2O, which restricts the reactor chamber design to include only corrosion-resistant materials. However, they may potentially enable transport of Al-containing III-V

materials such as AlGaAs and AlAs. Transport of AlAs by vapor transport could be an important proof of concept since it can be selectively etched for lift-off processing, offering a potential pathway to amortize the GaAs substrate cost if sufficiently high-quality GaAs on Si tandem solar cells cannot be produced. AlGaAs is an important ternary III-V semiconductor owing to it’s usefullness as a window layer and passivating layer. Thus increasing the complexity of the vapor transport reactor to enable growth of Al-containing III-V’s is potentially of interest.

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