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Realizing Pb/s IO with Silicon Photonic Chiplets

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Abstract: We outline recent efforts to realize Pb/s optical IO using heterogeneously integrated silicon photonics. Preliminary demonstrations ranging from device- to system-level validate our approach and present an appealing path towards achieving petabit-scale escape bandwidths.

The past decade has seen unprecedented growth of the digital world, spearheaded by the rapid rise to ubiquity of data-intensive workloads such as deep learning. Simultaneously, as Moore's Law draws to a close and computing systems will no longer be able to rely on predictable advances in transistor density, the interconnect bandwidth in these systems will still continue to lag behind compute performance. Without significant intervention, the concert of these roadblocks will severely constrain future computing systems and lead to stagnation in performance which will be insufficient to keep pace with rapidly accelerating workload demands. Silicon photonics is poised to alleviate this bandwidth bottleneck through providing highly scalable optical interconnects directly co-packaged with compute electronics, effectively removing current constraints on the highly distance-dependent bandwidth density-energy efficiency product (Fig. 1). However, commercial silicon photonic solutions in the current co-packaged optics roadmap fundamentally lack avenues for extreme scaling to realize petabit-scale package escape bandwidths, which will be necessary in the coming decades to keep pace with exponentially growing workloads. Here, we outline a comprehensive, massively parallel co-designed electronic-photonic interconnect capable of realizing 100 Tb/s/fiber data transmission while consuming as low as 100 fJ/b. While the strategies employed to reach these metrics represent a substantial departure from current state-of-the-art silicon photonic solutions, all of the described avenues are fundamentally compatible with high-volume manufacturing and thus represent a realistic path for continued scaling of optical interconnects into the Pb/s regime.

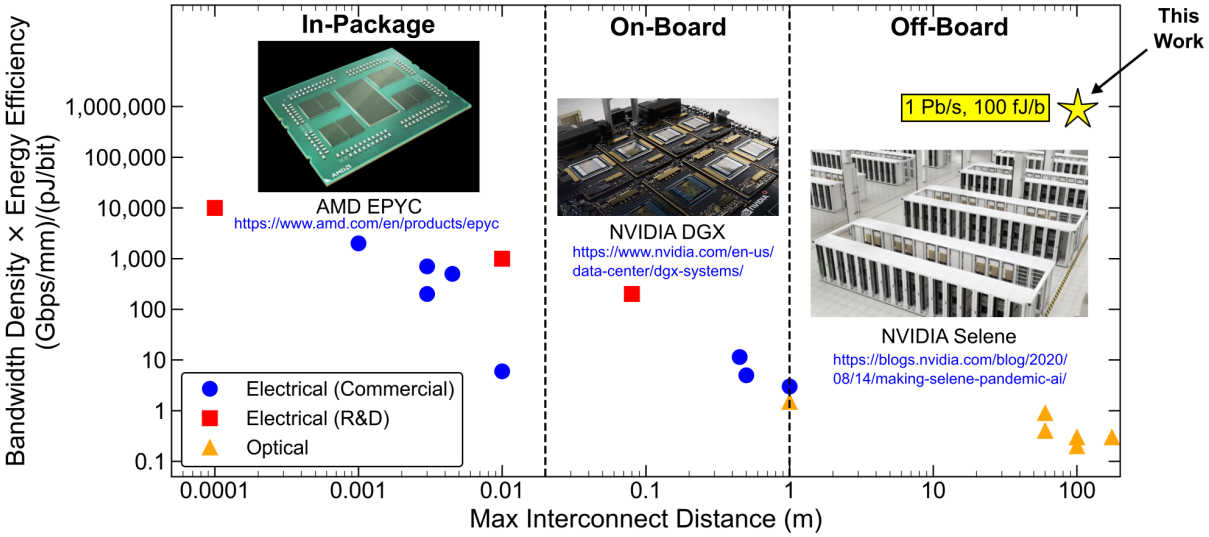

Fig. 1. Bandwidth density-energy efficiency product as a function of distance (adapted from Gordon Keeler, DARPA ERI Summit 2019). Insets highlight representative commercial systems at each length scale. The work detailed here represents a six order-of-magnitude improvement in figure of merit compared to currently available pluggable optical transceivers.

Our approach is predicated on massive parallelism in both the frequency and spatial mode domains. We leverage the large number of orthogonal, evenly-spaced frequency modes provided by chip-based Kerr frequency comb sources for highly scalable wavelength-division multiplexing (WDM) [1]. To capitalize on the broad bandwidth spanned by the comb, we recently demonstrated a novel link architecture using resonant modulators and filters which can scale to accommodate hundreds of frequency channels [2]. This architecture relies on on-chip interleavers to subdivide the comb, which we have designed and demonstrated to have ultra-broadband [3] and

fabrication-robust [4] performance. To make the process modifications necessary for realizing the required photonic system performance, we have closely collaborated with a commercial 300 mm foundry service (AIM Photonics) to tape out various dedicated wafers. Since link losses and power penalties are paramount to system performance, much of the device optimization efforts have focused on developing sub-dB chip-to-fiber coupling, highly efficient vertical junction microdisk modulators with large extinction ratio and low insertion loss, and low loss passive devices. Of additional critical importance is the energy efficiency of the constituent devices, much of which is dominated by thermal tuning to correct for fabrication variations and temperature fluctuations—in this direction, we have developed a substrate undercut process to dramatically improve the efficiency ($> 20\times$) of thermal phase shifters, a fabrication-robust design methodology to minimize phase errors in phase-sensitive devices [4], and a negative thermo-optic coefficient cladding to eliminate device temperature dependence. As an initial demonstration of a full 5 Tb/s/mm^2 transceiver module, we heterogeneously integrated a photonic die with a co-designed CMOS ASIC (fabricated in TSMC's 28 nm CMOS process node) through flip-chip bonding with copper pillars at 25 μm pitch [5]. Finally, to provide an additional axis for continued scaling, we have recently demonstrated efficient conversion from higher order spatial modes in silicon waveguides to orthogonal few-mode fiber modes for chip-to-chip mode-division multiplexing [6]. The combination of these demonstrated constituent components in a full system will enable unprecedented escape bandwidths for future-generation chip-to-chip interconnects.

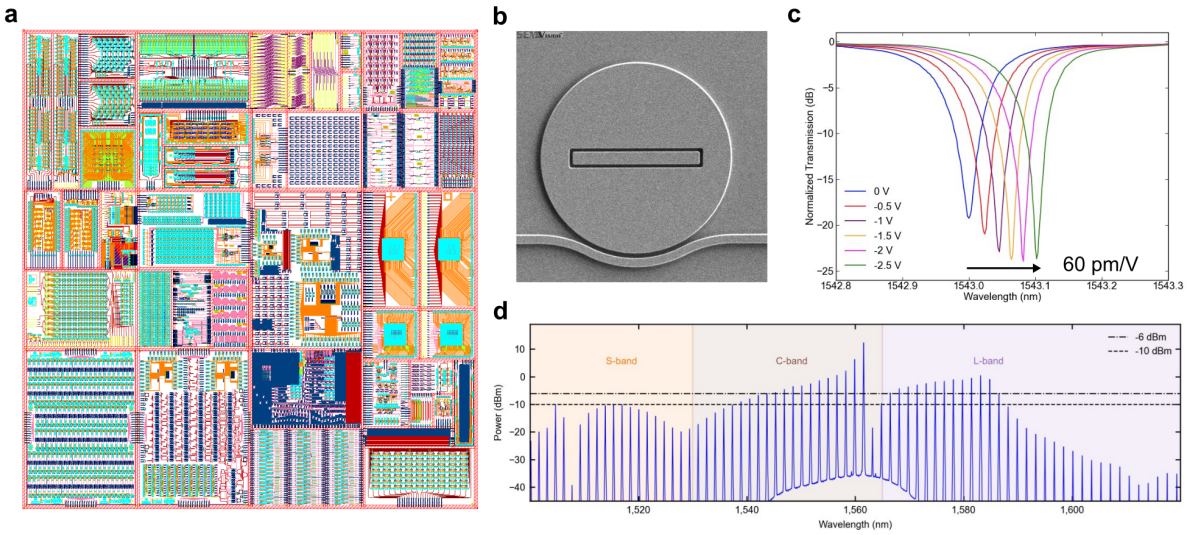

Fig. 2. **a,** Full reticle layout of dedicated wafer run. **b,** SEM image of custom vertical junction microdisk modulator. **c,** Depletion response of modulator. **d,** Normal GVD Kerr comb spectrum.

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