ETI 2019 ANNUAL WORKSHOP
NOVEMBER 5-6, 2019

Radiation Tolerant GaN Electronics

Ashok Dheenan, Shahadat Sohel, Md Wahidur Rahman, Tawfiq Musah, Siddharth Rajan

THE OHIO STATE UNIVERSITY, COLUMBUS, OHIO

THE OHIO STATE UNIVERSITY

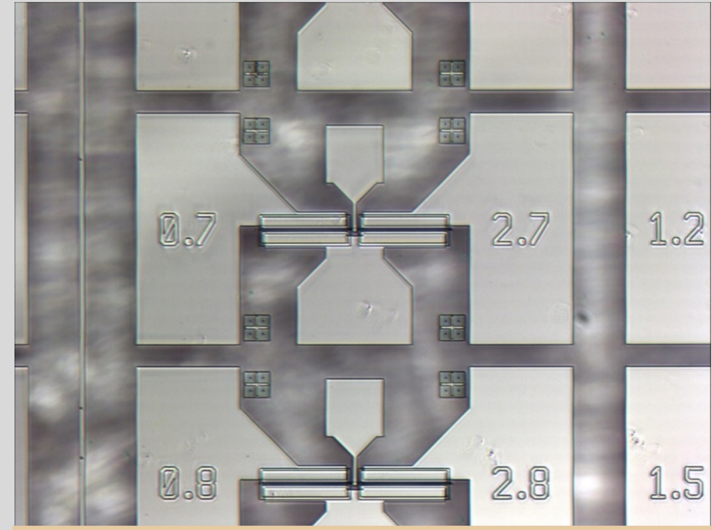
Objective: Development of radiation tolerant electronics for operation in extreme environments

Why Gallium Nitride (GaN) devices?

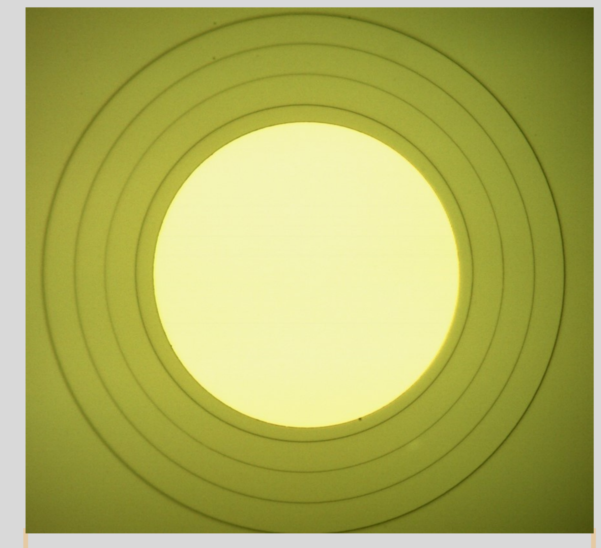
- GaN has the capability to operate in extreme environments, unlike Silicon (Si)
  - Wide-bandgap materials like GaN ($E_g = 3.2\ eV$) are more resistant than materials like Si ($E_g = 1.1\ eV$) to crystal defects caused by radiation due to the stronger bonds between atoms in the lattice

Project Outline

- Compact model robust enough to simulate device in circuit designs
- Develop process flow for digital and analog integrated circuits in The Ohio State University Nanotech West cleanroom
- Design and fabricate GaN-based ICs for sensing, communication & logic



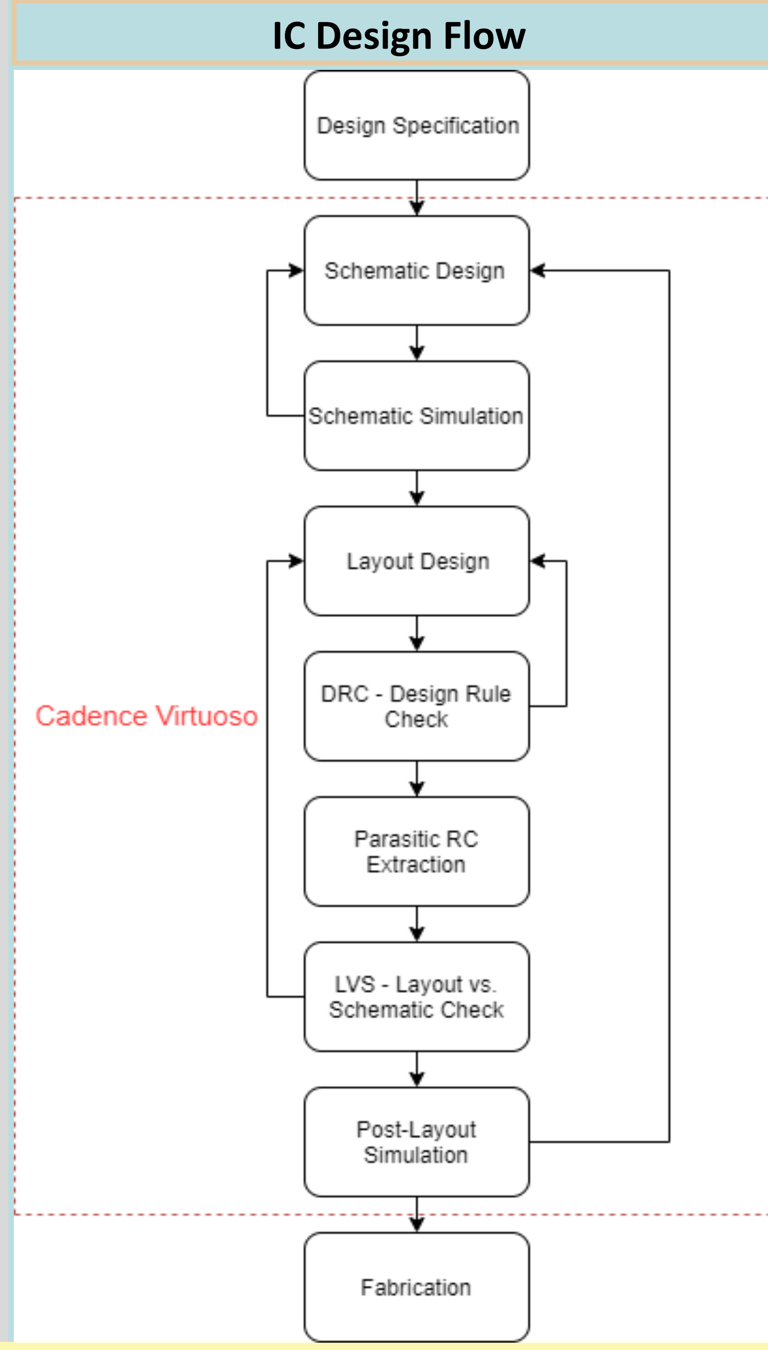
GaN HEMT Ground-Signal-Ground Die for RF Probing


GaN PiN Diode Power Device

Current Status of GaN Technology

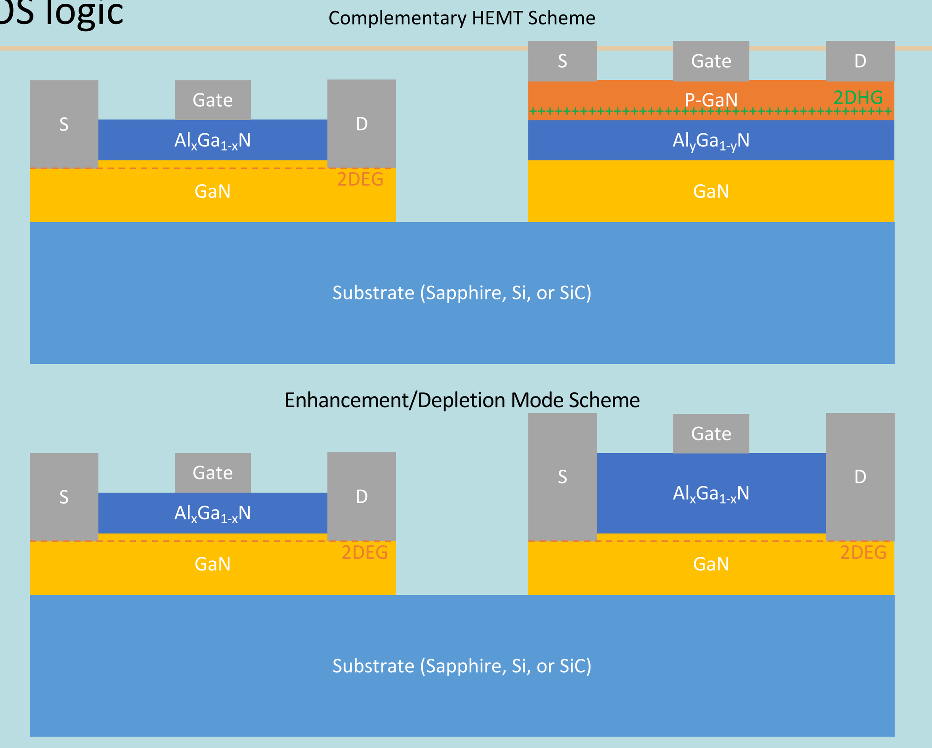
- GaN devices are widely used in power electronics & RF applications due to their ability to handle large current densities, large electric fields before breakdown and high-frequency operation
- Driving GaN RF or power devices using traditional Si CMOS logic ICs leads to inductive and capacitive losses
- Si CMOS circuits are intolerant to crystal defects caused by radiation -> results in threshold-voltage shift and unreliable operation
- Solution: develop GaN devices and circuits for digital logic and integrate on one chip with power and RF devices for best efficiency

IC Design Flow



Proposed Work

- Develop GaN logic devices and process technology in order to enable GaN digital logic IC's
- Two schemes can be employed in order to realize this goal:
  1. Enhancement/depletion-mode: A depletion-mode device serves as an active load while an enhancement-mode device serves as the driver
  2. Complementary: Use a p-channel device as the pull-up device and an n-channel device as the pull-down device; analogous to Si CMOS logic



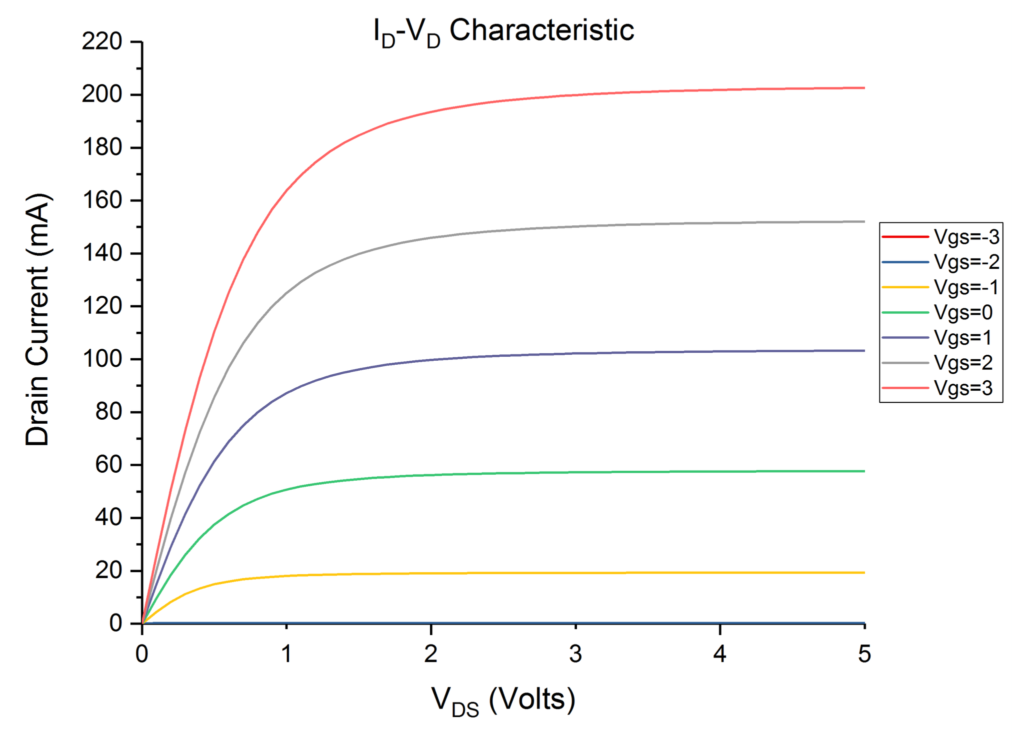
GaN HEMT Device Modeling

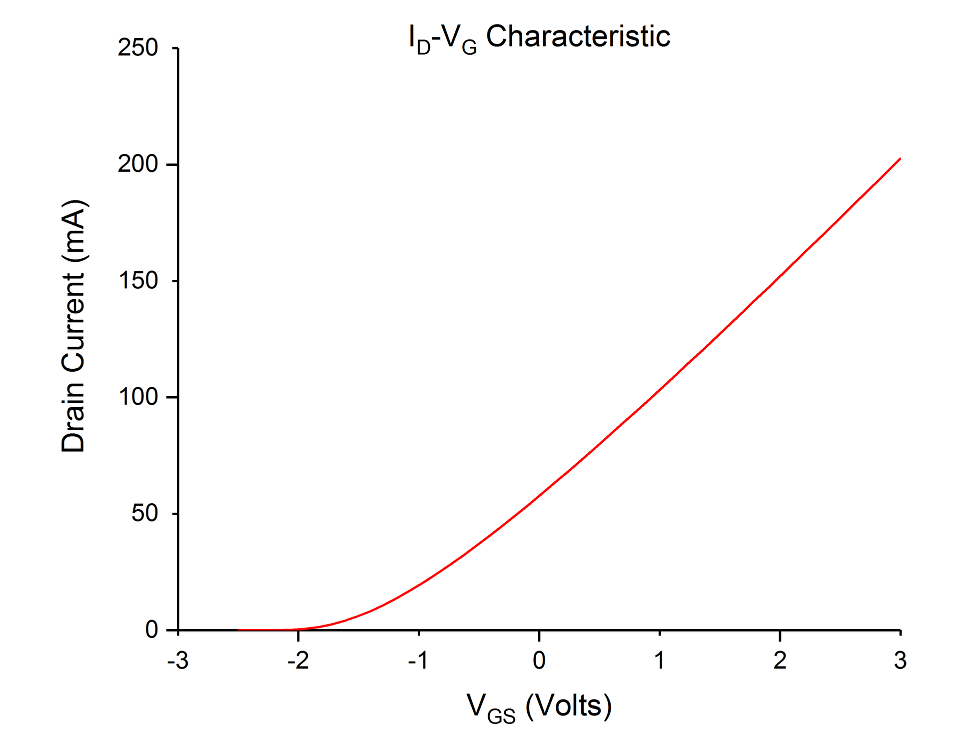
- Use ASM-HEMT 101.0.0 -> an industry-standard physics-based compact model used for power electronics and RF circuit simulation with GaN HEMTs (needs some modifications for digital & analog applications)

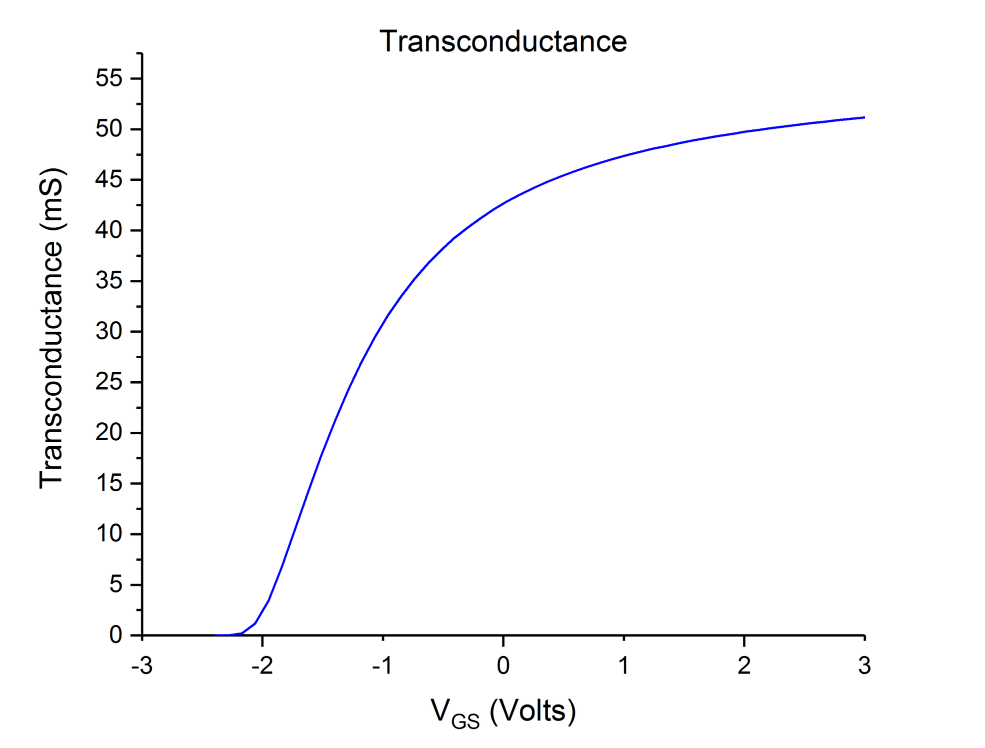
Drain Current Equation:

$$I_D = \frac{W}{L}\mu C_G\left((V_{GS} - V_{off}) - \psi_m + V_{th}\right)$$

- Modified model to automatically calculate V_{off} based on $t_{barrier}$
  - Sufficiently thin $Al_xGa_{1-x}N$ barrier layer (~5 nm) able to simulate a device with a $V_{off} > 0$ (enhancement-mode)







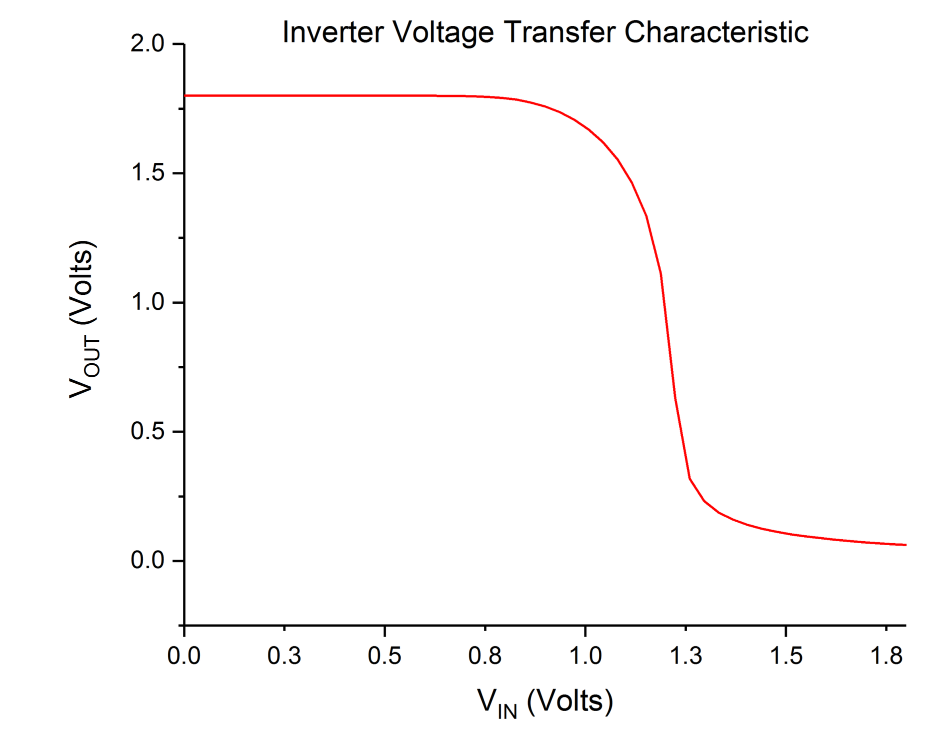
Circuit Simulation Framework

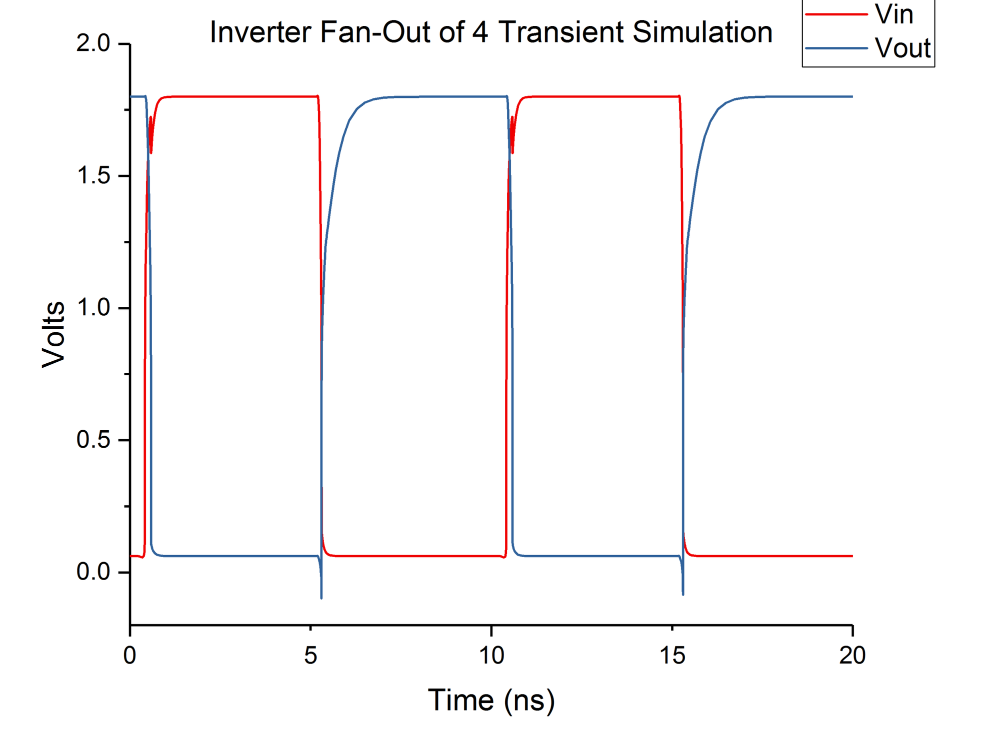
- Use Cadence Virtuoso -> CAD program for development of integrated circuits
- Simulated basic static logic gate structures using E/D mode scheme
- Extracted various performance metrics from simulated waveforms

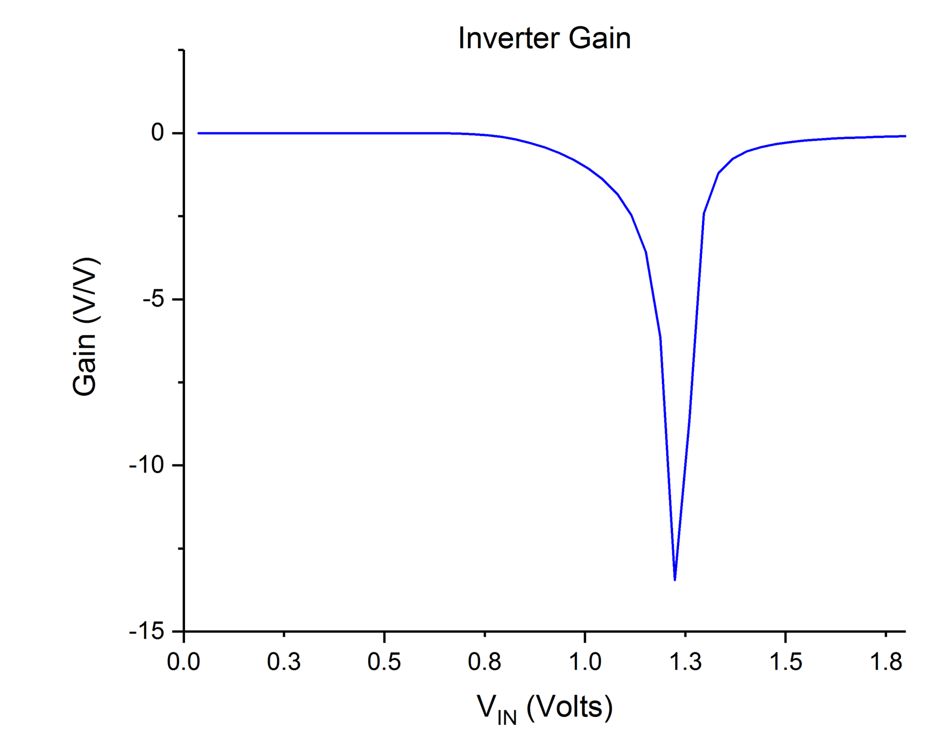
Simulation Dimensions & Voltages:

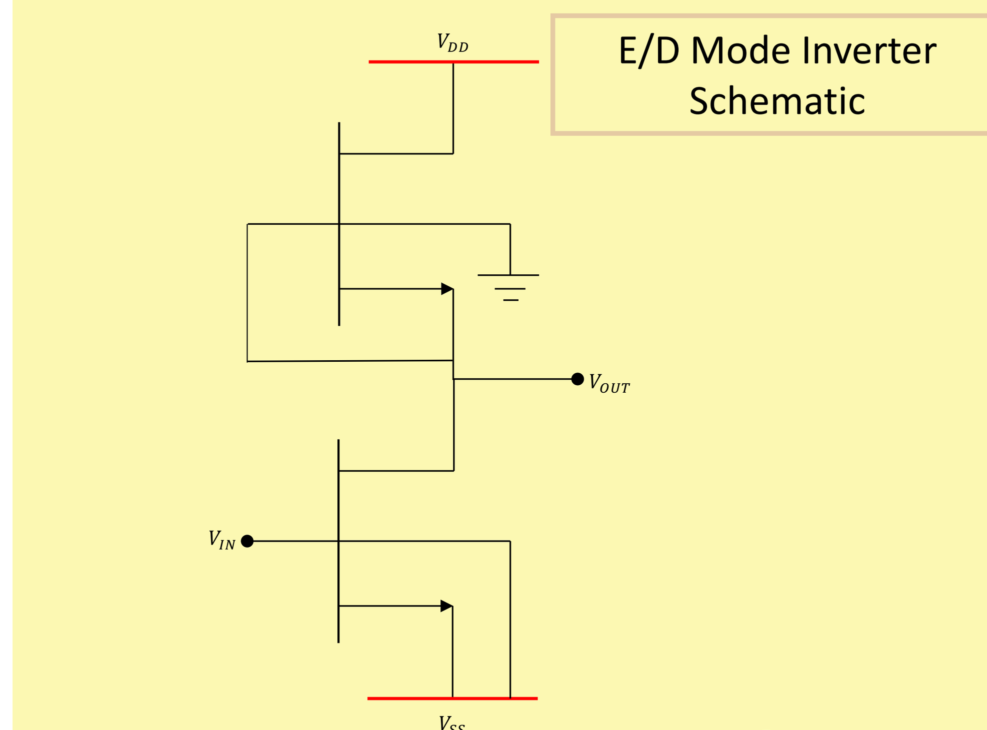
- $L_{SG} = L_{GD} = 1\ \mu m$
- $L_{Driver} = L_{Load} = 750\ nm$
- $W_{Driver} = 750\mu m = 10 * W_{Load}$
- $V_{off-Driver} = 0.9\ V$
- $V_{off-Load} = -2\ V$
- $V_{DD} = 1.8\ V$

Performance Metric	Inverter	NAND	NOR
Propagation Delay	88.3 ps	106.4 ps	88.5 ps
Fall Time (90%->10%)	90.7 ps	192.9 ps	90.5 ps
Rise Time (10%->90%)	549.6 ps	498.8 ps	550.8 ps
Noise-Margin High	450.61 mV	393.84 mV	450.60 mV
Noise-Margin Low	936.99 mV	896.97 mV	937.01 mV
Swing	1.74 V	1.67 V	1.74 V
Average Power Dissipation	50 mW	49.3 mW	50 mW









E/D Mode Inverter Schematic

National Nuclear Security Administration

Consortium for Enabling Technologies & Innovation