The Consortium for Enabling Technologies and Innovation

Virtual Summer Meeting for Young Researchers

Recent Progress on Ga_2O_3 Sensors and GaN Electronics

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The Ohio State University

8th July 2020

ETI

Thrust Area: 3

NNSA

National Nuclear Security Administration

PRESENTED BY

Wyatt Moore is an Electrical and Computer Engineering master's student at OSU. His research interests include high voltage vertical Gallium Oxide devices.

Adithya Balaji is an Electrical and Computer Engineering master's student at OSU. He is working on Gallium Nitride Integrated Circuits.

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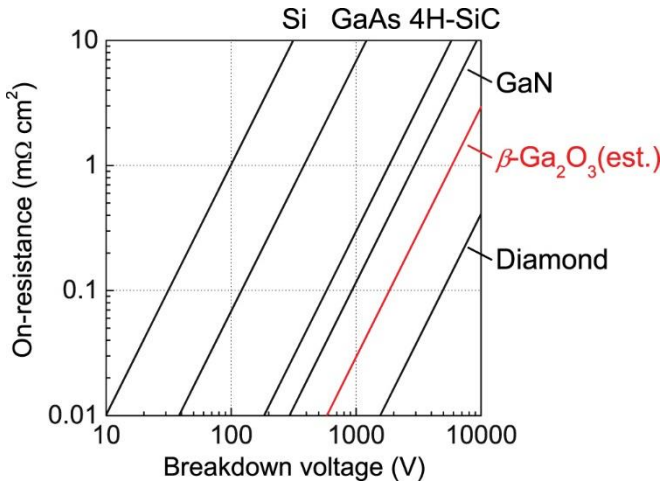
Gallium Oxide for Radiation Detectors

Novel Crystal Technology, Inc.

Edge-defined-film-fed growth

4" β–Ga_2O_3



β–Ga_2O_3 Power Devices

- High-quality bulk substrates
  - Low cost large area
- Large Bandgap
  - Reliability in high-temperature environments
  - Low intrinsic carrier concentration – **lower dark current**
- Large predicted breakdown field
  - **Low on-resistance**

Properties	Si	4H-SiC	GaN	β–Ga_2O_3
Bandgap E_g (eV)	1.1	3.3	3.4	4.8
Intrinsic Carrier Concentration (1/cm^{-3}) @Room Temperature	1.38x10^{10}	2.5x10^{-10}	9.8x10^{-12}	[a]1.48x10^{-17}
Electron Mobility μ (cm^2Vs^{-1})	1400	1000	1200	**300**
Breakdown Field E_{BR} (MVcm^{-1})	0.3	2.5	3.3	**8**
Relative Dielectric Constant ϵ_R	11.8	9.7	9.0	10
Baliga's FOM $\epsilon\mu E_{BR}^3$	1	340	870	**3444**

Masataka Higashiwaki *et al* 2016 *Semicond. Sci. Technol.* **31** 034001

[a]Vareley J, et al 2010 Applied Physics Letters 2019 vol: 115 (25) pp: 252104

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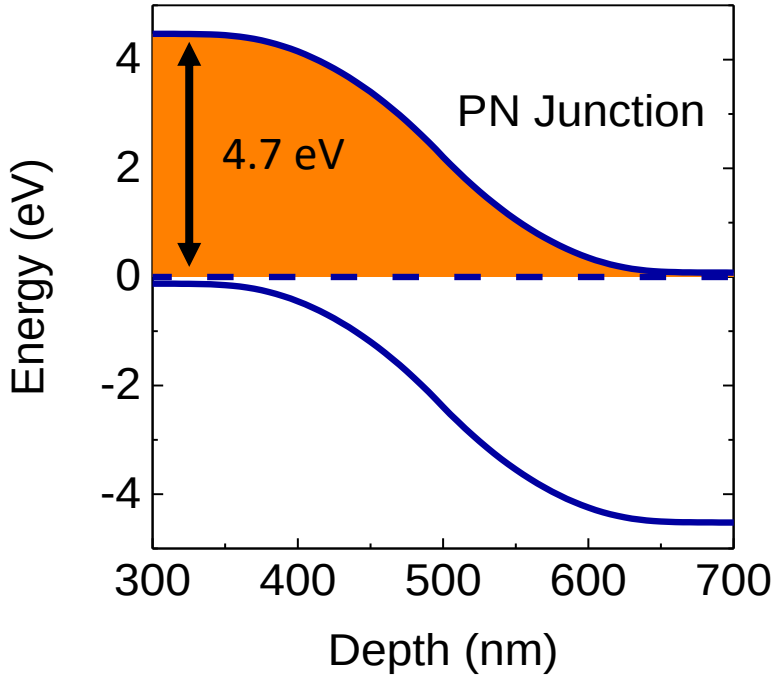
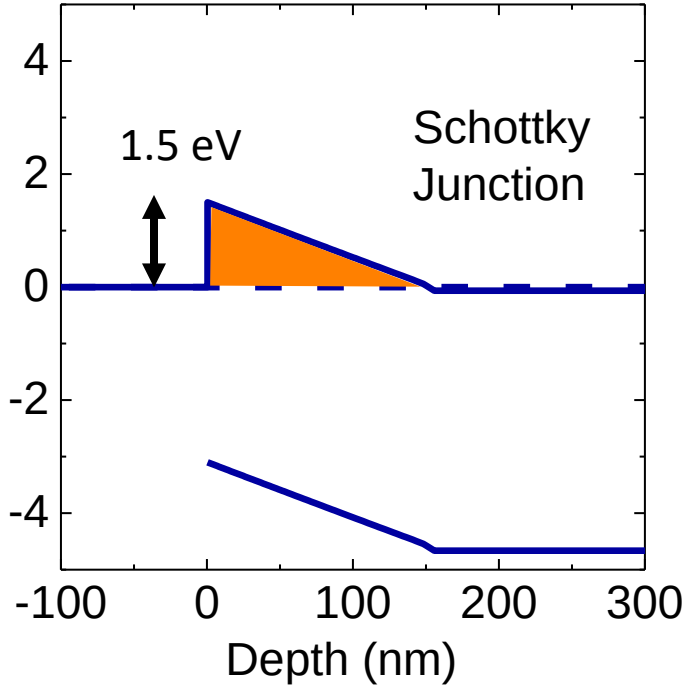
Dielectric Heterojunction (High-k) motivation





- Predicted 8MV/cm critical field assumes P-N junction to realize band-to-band tunneling
- Typical β-Ga_2O_3 Schottky Barrier diodes breakdown at a ~3MV/cm critical field.
- β-Ga_2O_3 p-type doping to realize P-N junction is challenging due to poor hole transport properties and large acceptor ionization energies.

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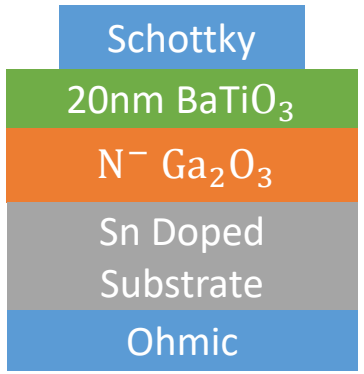
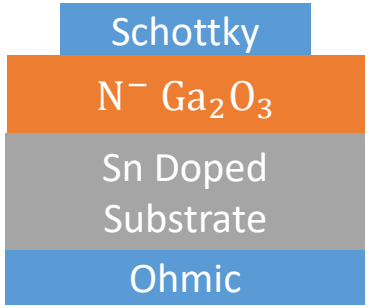
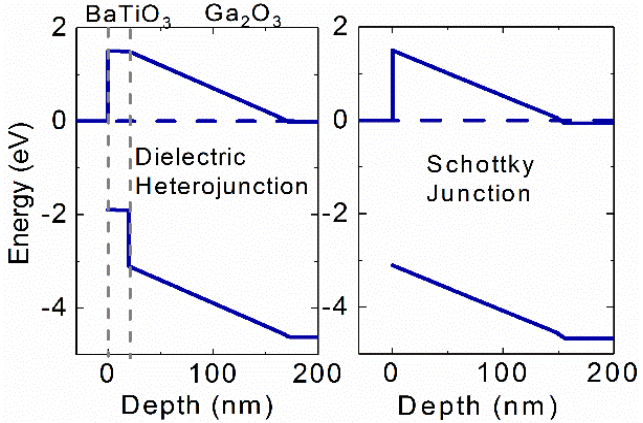
Dielectric Heterojunction Concept



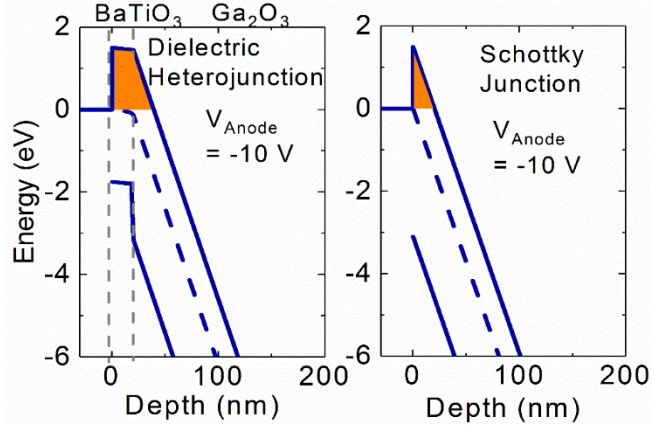
Dielectric Heterojunction



Schottky Barrier Junction



Equilibrium band Diagrams



Reverse Bias band Diagrams

- Predicted 8MV/cm critical field assumes PN junction to realize band-to-band tunneling
- Thin film $BaTiO_3$ is a high permittivity material $100 < \epsilon_R < 300$
- $BaTiO_3$ has a bandgap of 3.3eV and low CBO to Ga_2O_3 (χ=4eV vs. χ=4.1eV)
- Due to dielectric electrostatic boundary condition (1-dimension case)

$$E_{1t} = E_{2t}$$

$$\epsilon_1 E_{1n} = \epsilon_2 E_{2n} \rightarrow E_{BTO\hat{n}} = \frac{\epsilon_{Ga2O3}}{\epsilon_{BTO}} E_{Ga2O3\hat{n}} = \frac{10}{300} E_{Ga2O3\hat{n}} \rightarrow \frac{1}{30}\ \textit{reduction!}$$

- $BaTiO_3$ conduction band remains flat during reverse bias due to high relative permittivity

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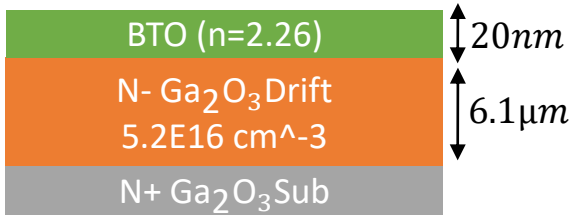
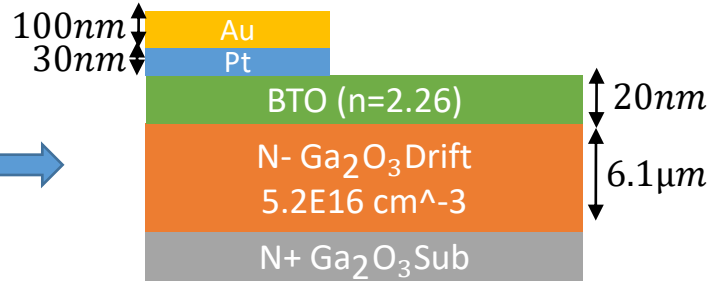
High Voltage Dielectric Heterojunction Fabrication

Novel Crystal Technology, Inc.

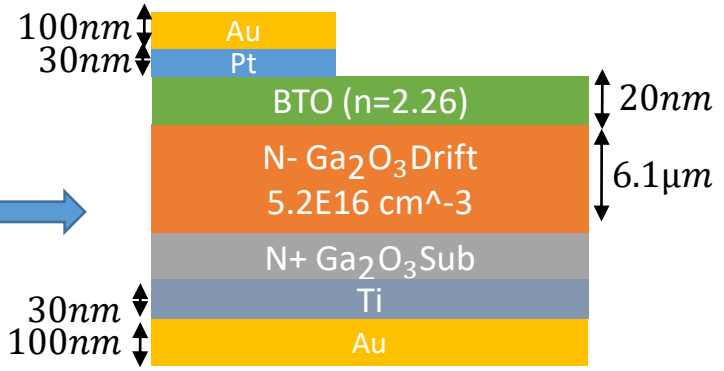
6.1µm with 5.2e16cm^{-3} doped drift layer grown by HVPE



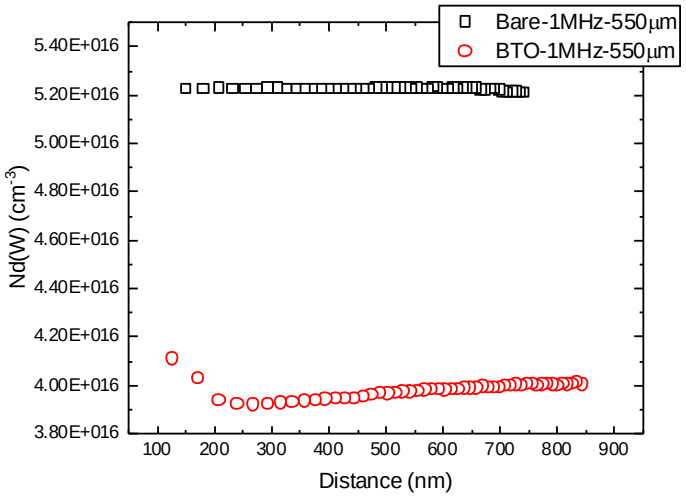
Clean substrate and deposit 20nm of $BaTiO_3$ via RF sputter



Pattern Schottky contact area and deposit 30nm/100nm Pt/Au via electron beam evaporator



Turn over and deposit ohmic contact 30nm/100nm Ti/Au via electron beam evaporator



- BTO deposited at high temperature (670 degC) with a rate of ~0.5nm/min
- 5.2x10^{16} cm^{-3} drift layer doping confirmed by capacitance-voltage measurement

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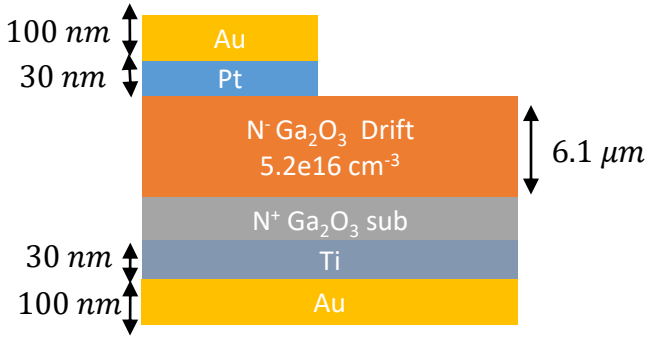
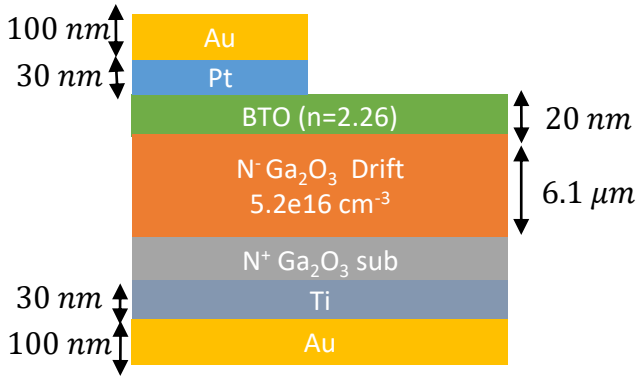
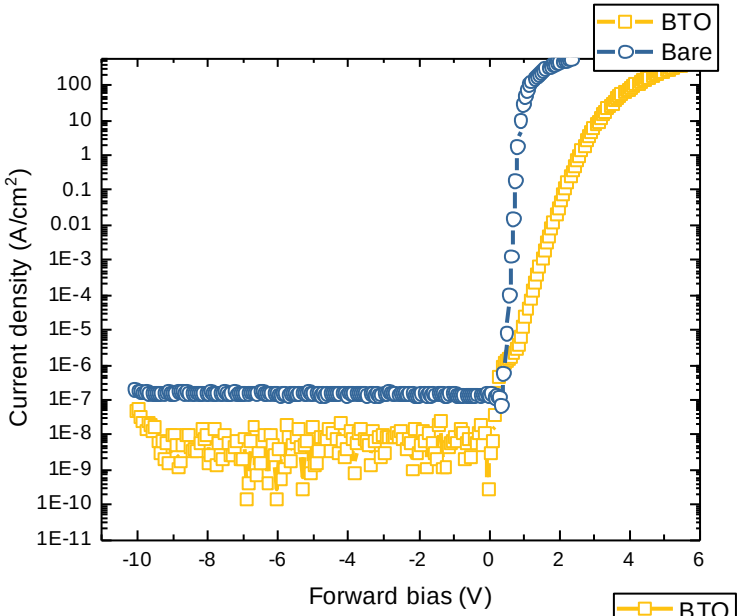
High Voltage Vertical Gallium Oxide Schottky Diodes

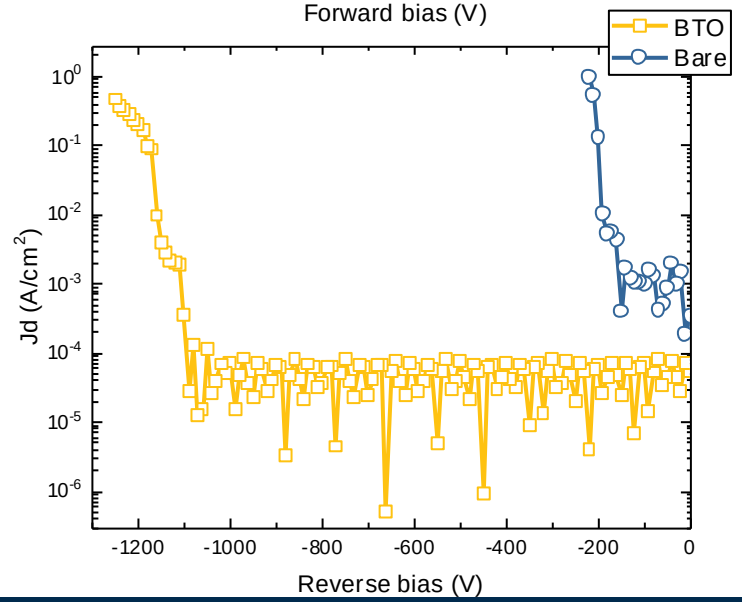


Bare Schottky



BTO Schottky





- Use of BTO enables 5X higher breakdown voltage
- Breakdown voltage **increases 5X from 220 V to 1250 V**
- Low leakage currents ~ 10 nA/cm^2, 10X improvement over Schottky diodes
- Peak field in GOX ~ 4.84 MV/cm (record value for any Gallium Oxide device)

Next steps: work with Raymond Cao (OSU) and other collaborators to investigate detector performance

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GALLIUM NITRIDE FOR RADIATION HARD ELECTRONICS

- Gallium Nitride, a wide-bandgap semiconductor, is less sensitive to ionizing radiation due to its high bond strength.
- The main objective of this work is to develop a technology to fabricate GaN digital circuits and analyze their performance in radiation environments.
- This technology could be implemented in designing radiation tolerant circuits.

RELATED GaN Research	Proton Irradiation	Gamma Irradiation	Neutron Irradiation	Electron Irradiation
HEMT	✔	✔	✔	✔
LED	✔	✔	✔	✔
Schottky Diodes	✔	✔	✔	✔
Integrated Circuits	THIS WORK			

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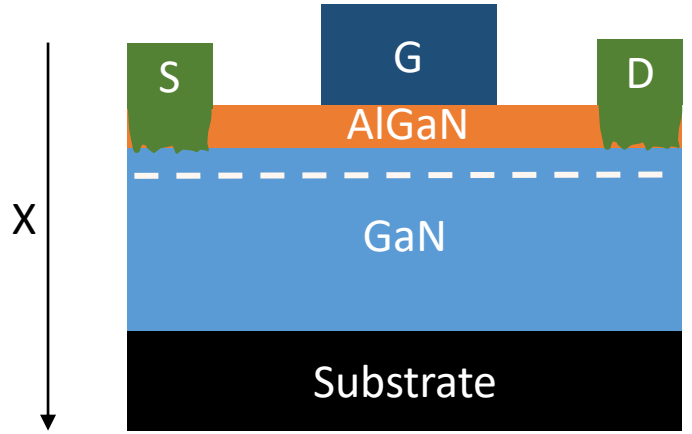
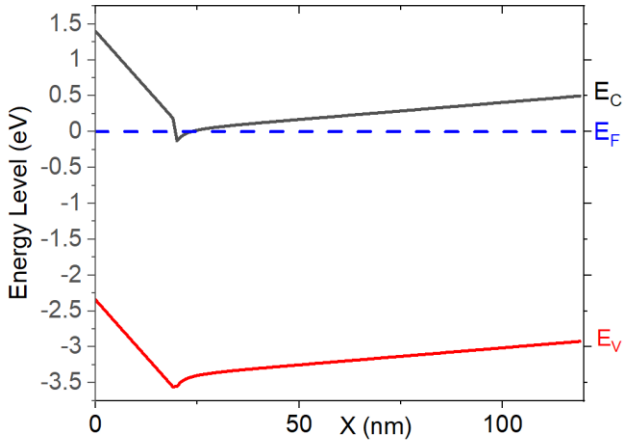
DEVICES USED IN GaN LOGIC

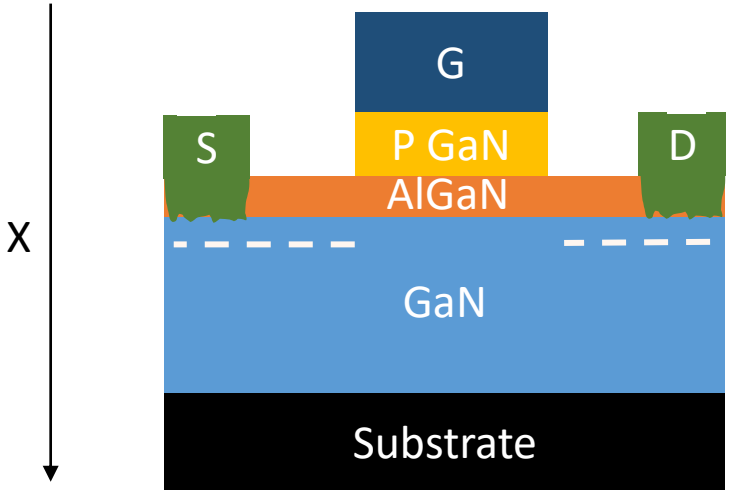
- Normally – on or **Depletion Mode GaN HEMT**: Needs a negative voltage at the gate to turn off the device.

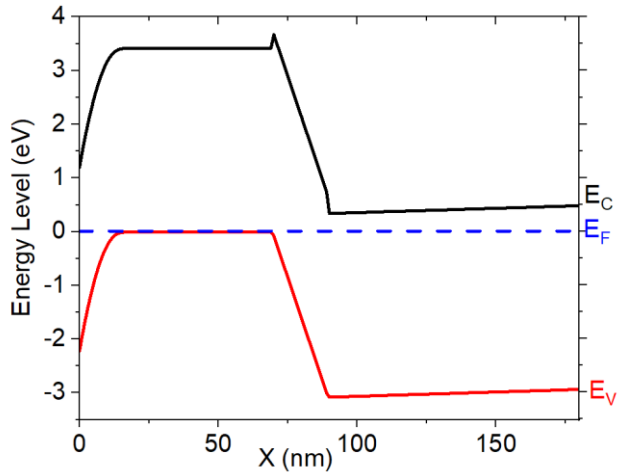




Depletion Mode HEMT: Normally ON

- Normally – off or **Enhancement Mode GaN HEMT**: Needs a positive voltage at the gate to turn on the device. The device shown here is a Gate Injection Transistor (GIT).





Gate Injection Transistor: Normally OFF

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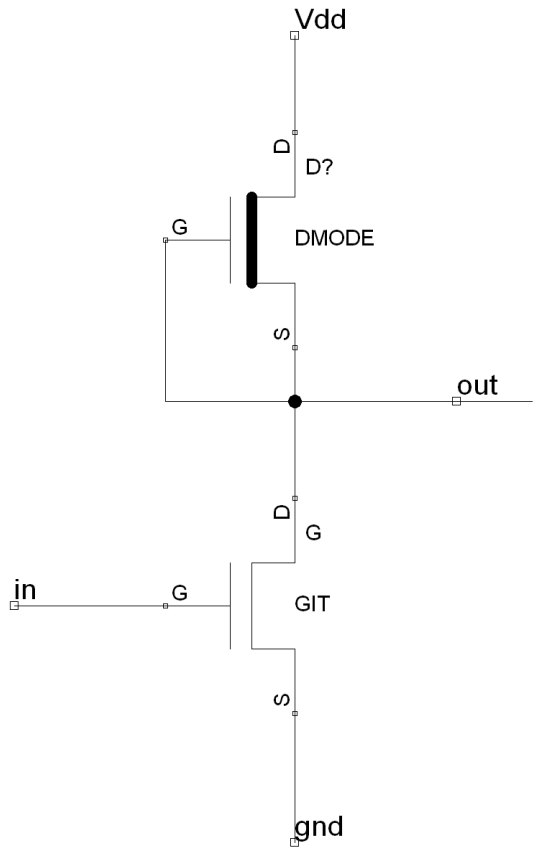
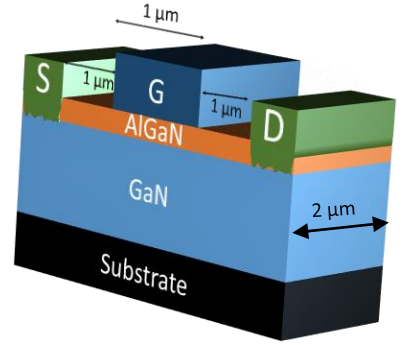
DIGITAL MONOLITHIC GaN INTEGRATED CIRCUITS

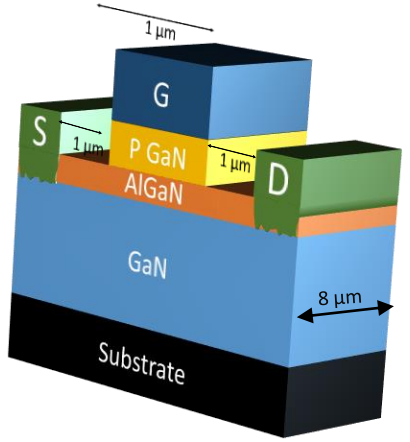
- Direct Coupled FET Logic (DCFL) enables universal gates using enhancement and depletion mode devices.
- The pull-up network is made up of a single Depletion-Mode transistor.
- The pull-down network contains the core logic implemented with Enhancement-Mode transistors.
- The D-Mode HEMT is used in the pull-up network
- Gate Injection Transistors (GIT) are used in the pull-down network.
- This logic family was chosen over CMOS due to the low hole mobility of P-Channel GaN devices.



DCFL INVERTER



D-MODE HEMT



Gate Injection Transistor

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DEVICE MODELS FOR CIRCUIT SIMULATIONS

- The device models were developed in Verilog – A. These models were used to simulate circuits in Cadence Virtuoso.

Standard HEMT:

2DEG CONCENTRATION:

$$n_s(V_g) = \frac{Q_{\pi(net)}\, d_{AlGaN} + \epsilon\left[V_G - \left(\Phi_b - \frac{\Delta E_c}{q}\right)\right]}{qD}$$

THRESHOLD VOLTAGE:

$$V_{off} = \Phi_b - \frac{\Delta E_c}{q} - \frac{Q_{\pi(net)}\, d_{AlGaN}}{\epsilon}$$

Gate Injection Transistor:

2DEG CONCENTRATION:

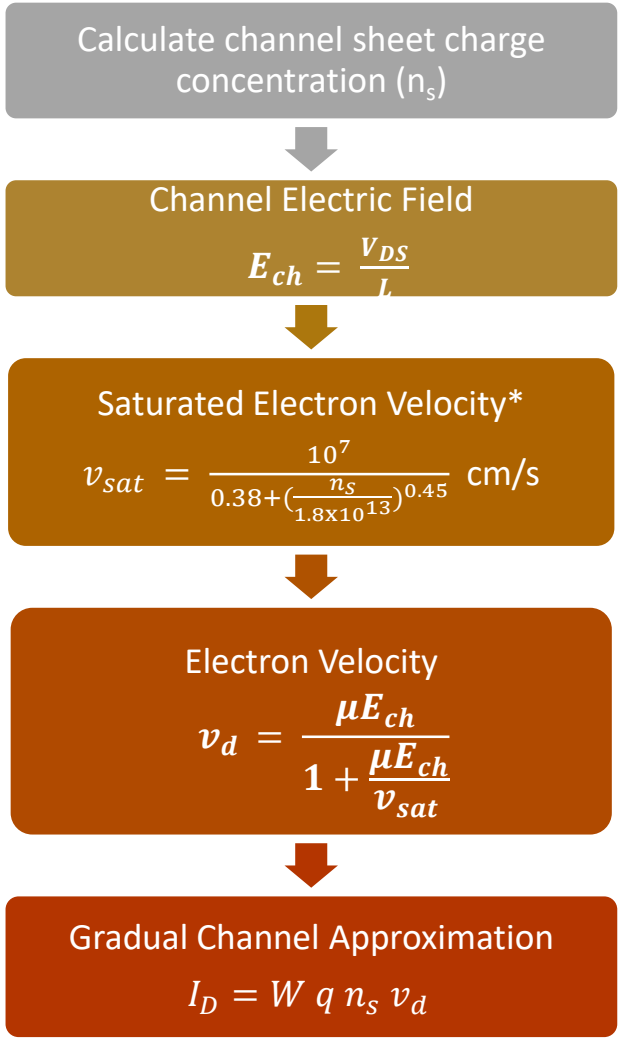
$$n_s = \sigma_p - \frac{\epsilon_s}{q d_{AlGaN}}\left(\frac{E_{gGaN}}{q} - V_G\right)$$

THRESHOLD VOLTAGE:

$$V_T = \frac{E_{g,GaN}}{q} - \frac{q\sigma_p t_A}{\epsilon_s}$$

- The simulated model device characteristics matched well with the experimental data

*Appl. Phys. Lett. 107, 153504 (2015)



Model Algorithm

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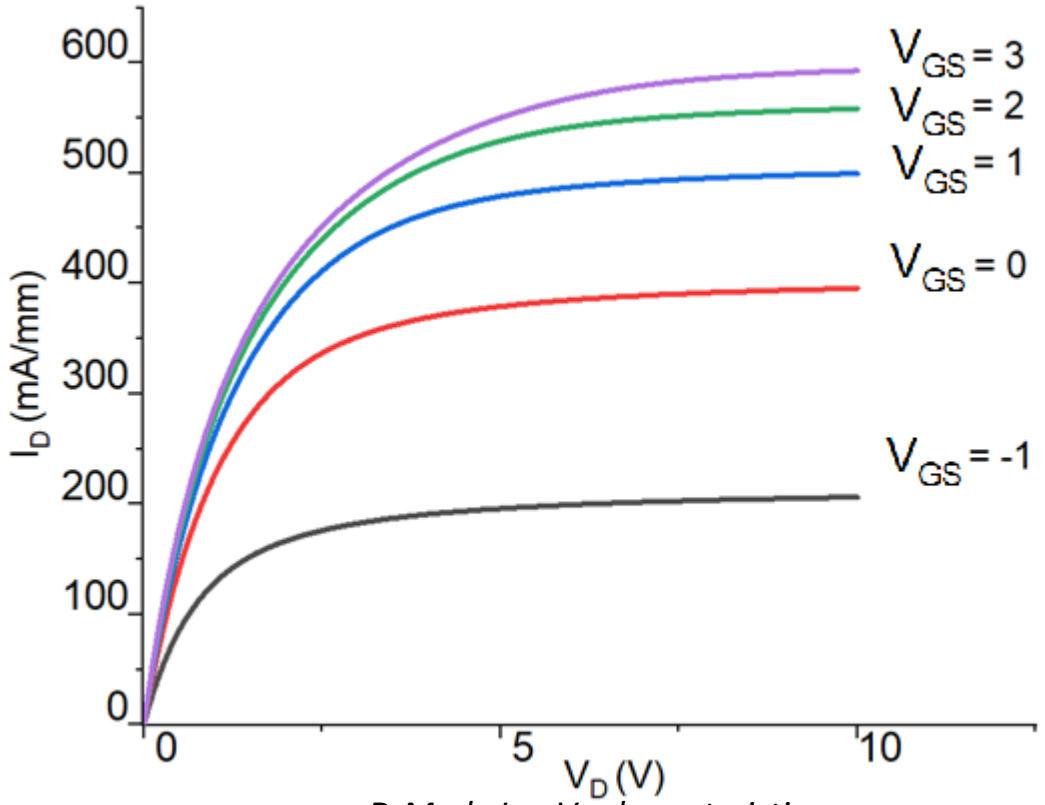
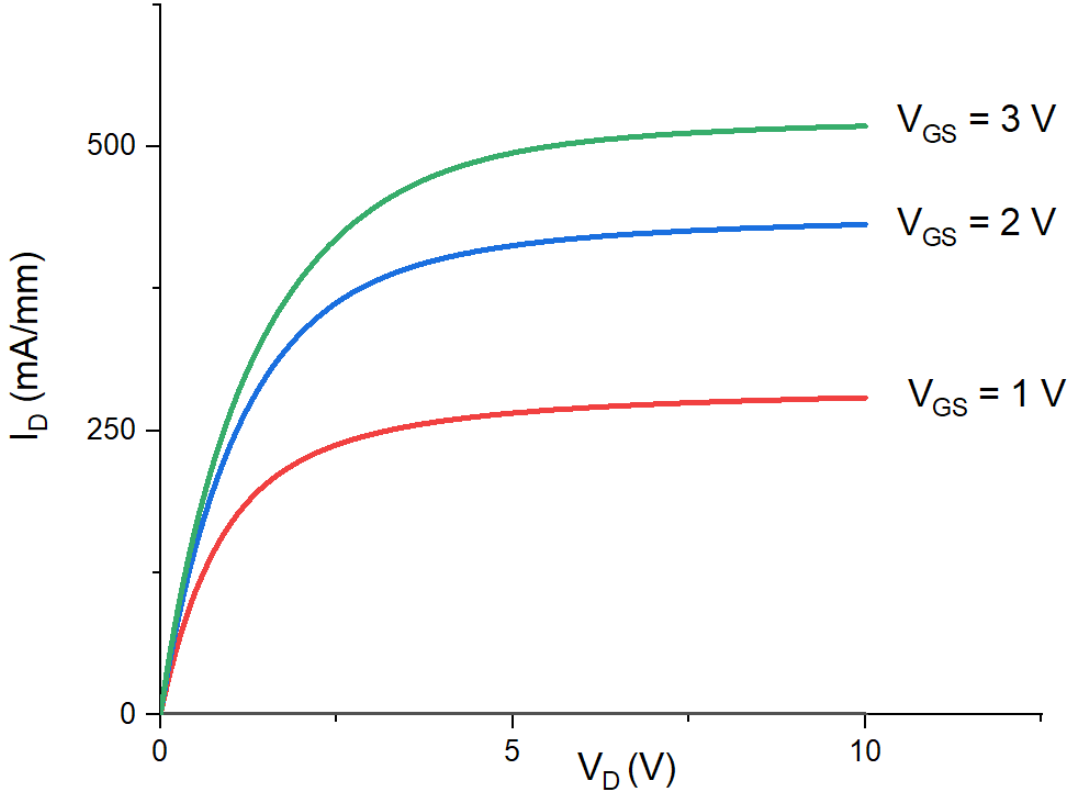
DEVICE MODELS FOR CIRCUIT SIMULATIONS

PARAMETER	VALUE
Threshold Voltage (V_T)	-1.63 V
$n_s(V_g=0)$	7.1 x 10^{12} cm^{-2}



D-Mode $I_D - V_D$ characteristics

PARAMETER	VALUE
Threshold Voltage (V_T)	0.3 V
$n_s(V_g=0)$	7.04 x 10^{12} cm^{-2}



GIT $I_D - V_D$ characteristics

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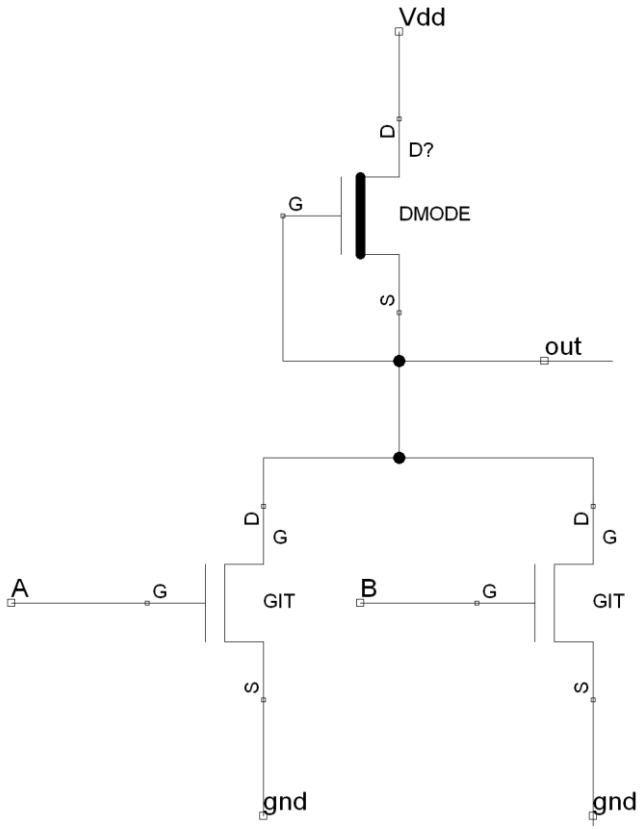
CIRCUIT SIMULATION: NOR GATE



DCFL NOR GATE CELL SCHEMATIC

- Dimensions of the devices were chosen to optimize the drive strength of the cell.
- A stronger pull-down is chosen to improve the strength of logic low.

DIMENSIONS	VALUE
Width of the D-Mode device	2 µm
Gate length of the D-Mode device	1 µm
Width of the GIT	8 µm
Gate length of the GIT	1 µm

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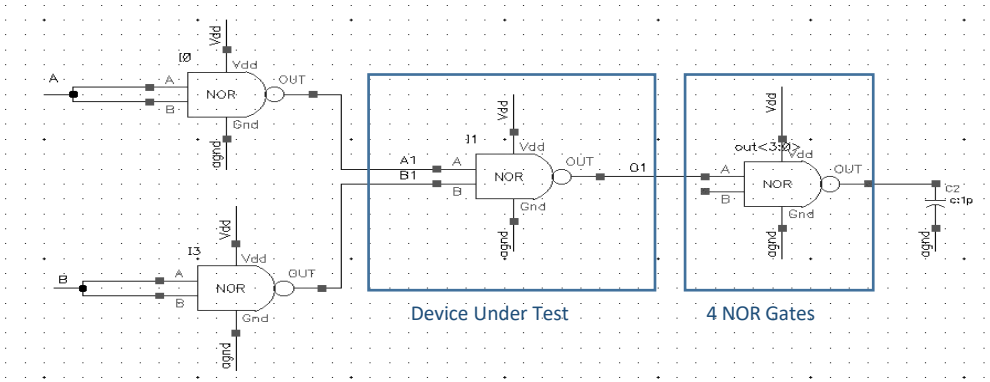
CIRCUIT SIMULATION: NOR GATE

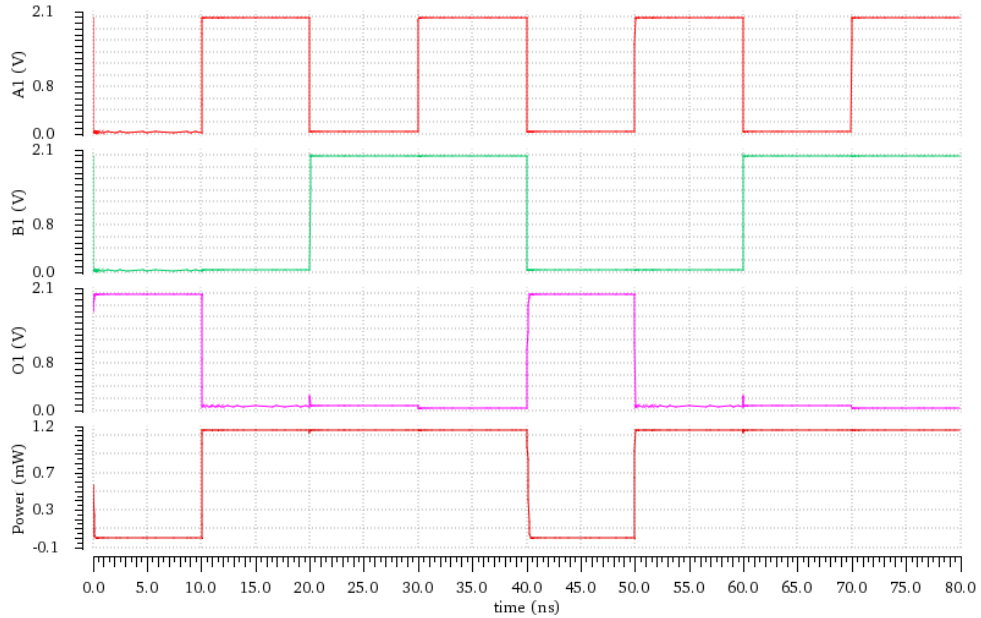
- Fan-out of 4 (FO4) delay is measured by loading the test gate by 4 other similar gates.
- Asymmetric rise and fall times are due to asymmetric drive strengths of the pull-up and pull-down devices.

METRIC	VALUE
Rise Time (T_{PLH})	251 ps
Fall Time (T_{PHL})	97 ps
FO4 Delay ($T_{PLH} + T_{PHL}$)/2	174 ps
Average Power	1.68 mW

Performance Metrics



FO4 NOR GATE TESTBENCH



NOR gate transient simulation. The NOR gate was loaded by 4 other NOR gates (FO4) for this simulation.

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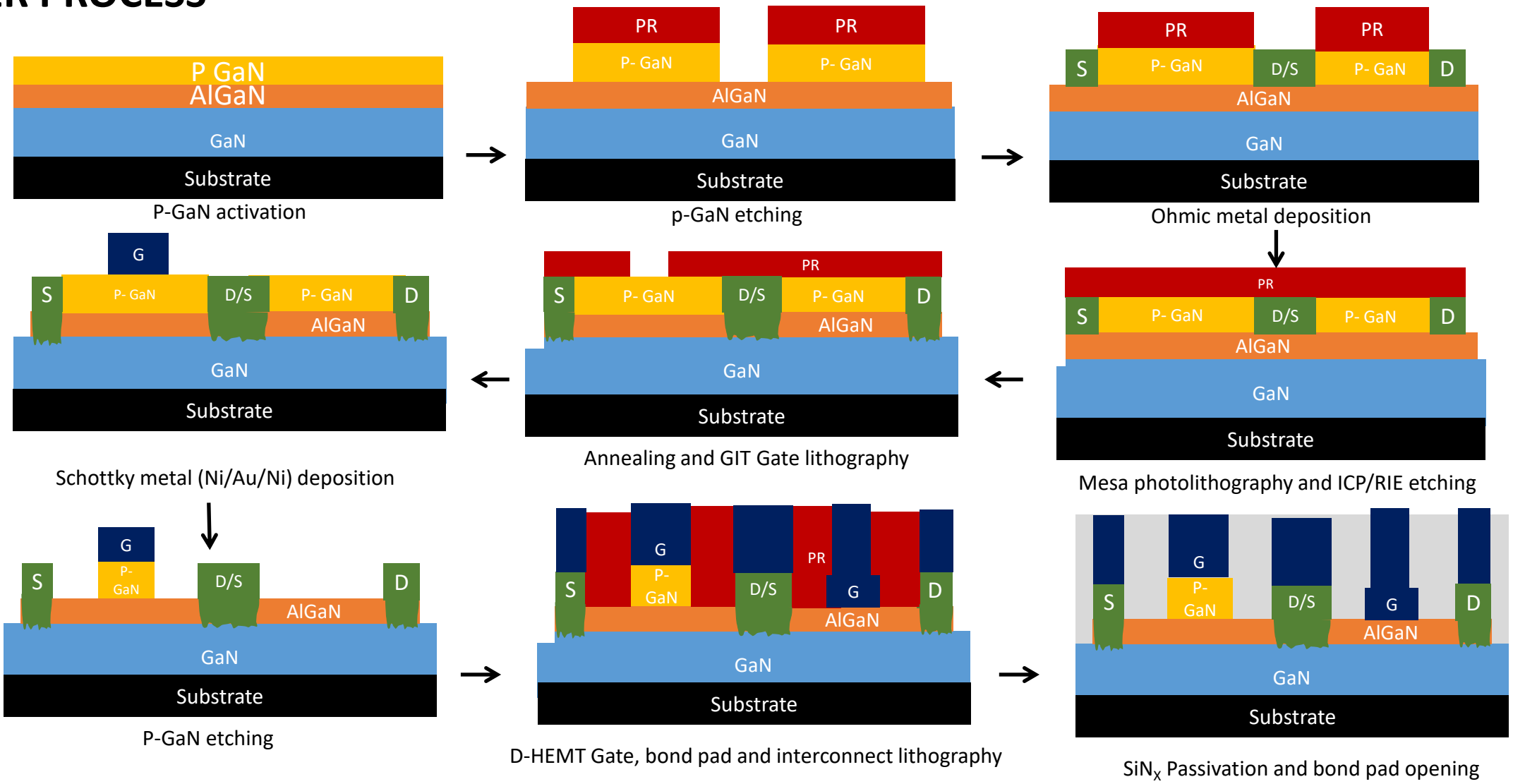
INVERTER PROCESS



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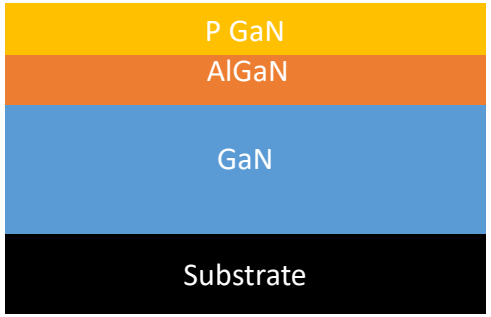
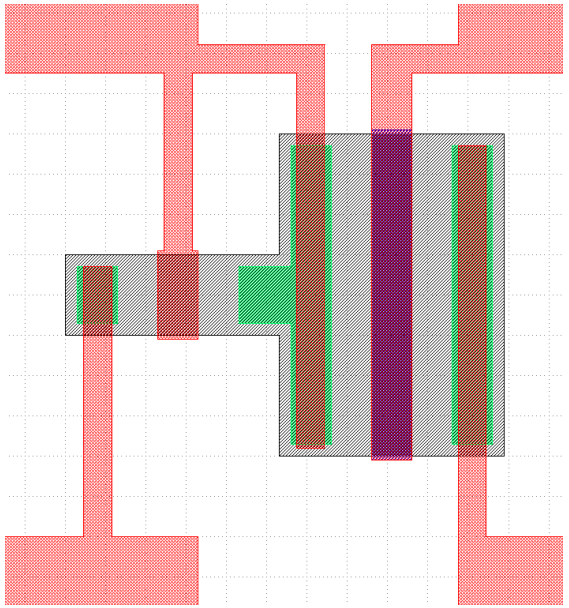
ONGOING WORK

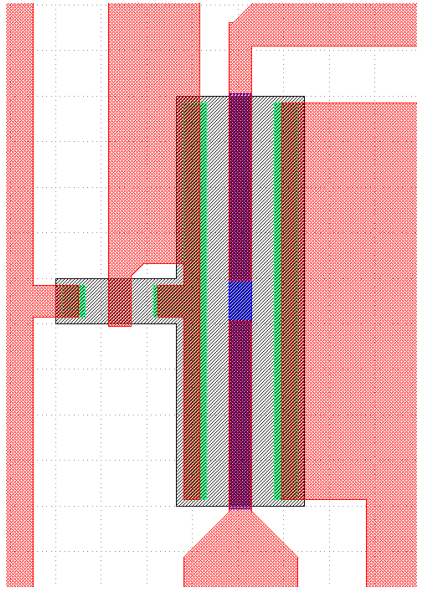
- The circuits are being laid out using this technology. The next step is to fabricate these circuits at OSU.
- Post fabrication, the samples would be subject to ionizing radiation. The performance metrics of the circuits post irradiation would be analyzed.



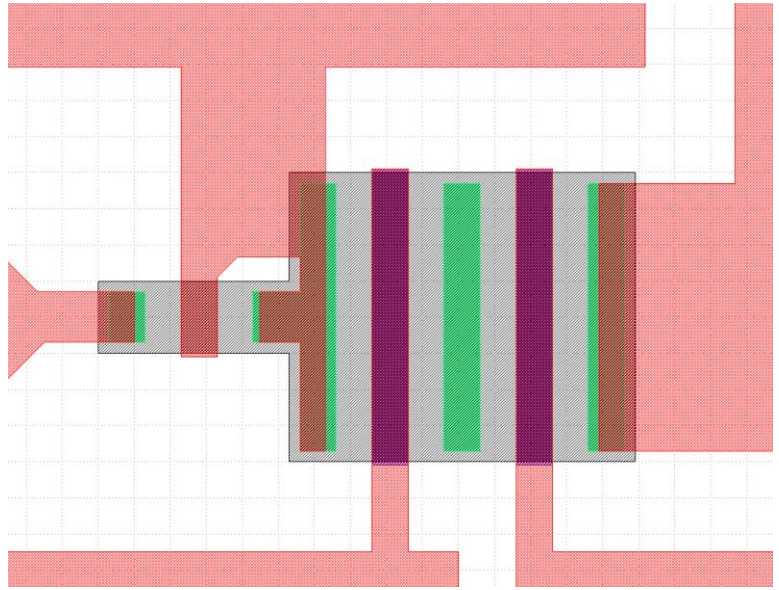
Wafer epitaxial structure



DCFL INVERTER LAYOUT



DCFL NOR GATE LAYOUT



DCFL NAND GATE LAYOUT

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