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Tradespace Analysis of Software-Defined Radio Architectures for Mid-Band 6G Communication Systems

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ABSTRACT Software-defined radios (SDRs) must balance wide frequency coverage, high instantaneous bandwidth, signal fidelity, power consumption, occupied board area, and cost. To date, a wide variety of SDRs have been implemented across baseband, intermediate frequency (IF), and direct RF sampling topologies, built with both discrete and highly-integrated RF System-on-a-Chip components. This resulted in a complex and heterogeneous landscape of SDR designs. The relative merits of different sampling topologies and of different architectures for high-performance embedded SDRs remain unclear. This paper develops a system-level architecture tradespace to evaluate whether topologies are an effective pattern for understanding this complex design space. The analysis defines a morphological matrix of candidate architecture decisions and their options, enumerates a set of valid SDR architectures, and evaluates the performance of each architecture by using a weighted multi-attribute utility metric derived from transmitter, receiver, and auxiliary sub-system performance models. Across 2,024,640 enumerated single- and multi-channel SDR transceiver architectures, the Pareto frontier reveals that recent advances in data converter and programmable logic technologies have made direct RF sampling cost-performance competitive with industry-standard IF sampling topologies. The candidate architecture decisions were also analyzed for system performance sensitivity via a main-effect analysis, allowing the sorting of SDR design decisions from most to least impactful. System performance is most sensitive to receiver architectural decisions, in particular the analog-to-digital converter, local oscillator, and preselect filter, indicating the opportunity for continued advances in these technologies to contribute to high-performance 6G SDR systems. Additionally, in contrast to single-channel systems, multi-channel RFSoC-based SDR architectures become substantially more cost-performance competitive compared to discrete component-based implementations.

INDEX TERMS Software-defined Radio, RF System Architecture, RF Transceiver, RF System-on-Chip.

I. Introduction

THE 6th generation (6G) cellular networks are expected to improve on every aspect of 5G. Currently, cumulative mobile traffic in both uplink and downlink directions exceeds 80 exabytes (80 million terabytes) per month [1]. With the advent of advanced cellular network applications, such as holographic communications and virtual/mixed reality, both throughput and overall data consumption are only expected to increase. Consequently, 6G will require to support data rates of 1 Tbps, 10 times those of 5G networks [2]. Given the scarcity of the available spectrum, the peak spectral efficiency is expected to be improved 3-10 times from current technologies [2], [3]. The user plane latency is also expected to be reduced to 100 μs compared to ultra-reliable low-latency communications offering 1 ms latency in 5G networks [4].

Achieving these goals will be difficult without considerable improvements to a set of enabling technologies that can be grouped into four broad categories: innovative network architectures, new spectrum, intelligence in the network, and new physical layer technologies [5]. In particular, software-defined radio, a digital radio whose baseband functionality is fully implemented in digital logic and software, is of particular interest as it enables reconfigurable implementation of radio functions across different frequency bands, signal bandwidths, and waveform configurations. The versatile

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technology of SDR requires a unique combination of reconfigurable complex programmable logic, advanced digital signal processing (DSP) implemented in field programmable gate arrays (FPGAs) or multi-processor (MP) systems-on-chips (SoCs), state-of-the-art high-frequency data converters, and a flexible front-end radio architecture, all of which can considerably complicate the radio hardware design. Given the vast array of possible SDR designs resulting from the combinatorial possibilities offered by modular system components, it is important to understand whether the landscape of SDRs can be grouped into a small number of recurring architectures : families of similar designs , with each family representing different cost and performance tradeoffs. To date, a wide variety of SDR designs have been implemented that span three main topologies:

- Baseband (BB) sampling, where an RF signal is mixed to complex baseband and then digitized,
- Intermediate frequency (IF) sampling, where the signal is downconverted to an intermediate frequency and digitized at IF, followed by digital downconversion, and
- Direct radio frequency (RF) sampling, where band-limited RF signals are digitized directly, often through bandpass sampling, undersampling, or Nyquist-folding techniques, with digital logic handling the frequency translation, signal channelization, and aggregation.

Across commercial implementations, BB, IF, and direct RF sampling persist as distinct topologies [6]–[10]. All three also appear in both discrete-converter implementations and in highly integrated radio frequency SoCs (RFSoCs) that co-locate high-speed data converters with programmable logic on the same semiconductor chip. However, topology alone does not determine SDR performance. Within each topology, performance also depends on a multitude of architectural decisions such as analog RF and IF filtering, placement and number of gain stages, and data-converter technology. Therefore, this paper asks whether the popular characterization of sampling topologies represents a strong organizing principle for families (architectures) of similar designs. An additional research question asks which of the many decisions in an SDR is most architectural, that is, which decisions have the greatest impact on SDR performance. These architectural decisions, in turn, should be the focus of research aimed at improving SDR performance to achieve the 6G goals. Finally, this paper examines how single-channel and multi-channel SDR architectures differ, specifically assessing whether the SDR system performance sensitivity to architectural decisions varies substantially between single-channel and multi-channel architectures. The following subsections summarize the broader grouping of 6G technology enablers that motivates this study.

A. Innovative Network Architectures

Through multi-connectivity techniques, heterogeneous integrations of different radio units and communications frameworks, concurrent use of different network interfaces, and cell-less network architecture, users will be able to connect to the network as a whole, extending network access beyond direct connectivity to the cell tower and enabling seamless mobility by minimizing handover overheads [5]. The 3D network architecture will also utilize the multi-connectivity techniques to enable extensive coverage, high-throughput, and resilient communications through the formation of an integrated three-dimensional space-air-ground network topology in which ground-based base stations are integrated with airborne and space-based network assets. Disaggregation and virtualization of the network will allow the decomposition of traditionally integrated network components, such as the hardware and software resources in medium access control and physical layers, into modular, interoperable elements that can be represented in software. This enables network slicing, whereby the physical and logical network resources are integrated into a software-defined network environment, whereby a single physical infrastructure can be subdivided into multiple virtual networks, with each slice tailored to specific network performance needs [11]. Open Radio Access Network (O-RAN) is going to offer standardized radio access hardware and software, thus providing a highly flexible network infrastructure leveraging intelligent and open multi-vendor equipment. Furthermore, the ability to use off-the-shelf components is expected to result in considerably reduced capital and operational expenditures, as well as overall network energy consumption. Within such a flexible and disaggregated network infrastructure, advanced integrated access and backhaul will enable the 6G network cells to use their extreme throughput capacity to perform backhaul functions in addition to providing network access to users. This will considerably simplify the network infrastructure but will also introduce network management and potential interference overhead.

B. New Spectrum

The new use cases of holographic communications and massive digital twins, the need for extremely high capacity in densely populated urban areas, and ultra-reliable low-latency communications will require a significant amount of new spectrum to be made available to 6G networks, and new frequency bands are being explored. The primary emerging frequency bands are the low-band, mid-band, and high-band.

The low-band, sub-1 GHz frequencies will be used in scenarios where wide-area coverage or deep indoor penetration is necessary. This band will be used to provide core mobile network connectivity everywhere while on the move, as well as enable applications such as smart agriculture and connectivity in rural areas. This frequency range is congested and contested, necessitating frequency reuse.

The mid-band frequencies, spanning 1–24 GHz, are segmented into the lower mid-band (1–7 GHz) and upper mid-band (7–24 GHz). The lower mid-band frequencies are already heavily used in 5G communication networks. While

opportunities for new spectrum are envisioned, spectrum reuse and non-exclusive use of the available spectrum are most likely scenarios. The upper mid-band, especially the 7–15 GHz frequency range, also known as the centimetric range, is a new consideration to the available spectrum, and is considered to be the main enabler of enhanced mobile broadband, the internet of senses, advanced mixed reality, and holographic communications, as well as massive digital twin technology. This frequency range, however, will also require considerable effort for global harmonization due to overlaps in the internationally allocated spectrum for already existing applications.

The high-band, sub-THz, frequencies in the 92–300 GHz range will be primarily used to achieve the peak data rates of 1 Tbps, enabled by the availability of multi-gigahertz contiguous signal bandwidths. Operating at these frequencies, however, comes with significant challenges. To overcome them, new physical layer technologies, like massive MIMO, will have to be used. Although the full use of this frequency range is not expected for the first commercial deployment of 6G systems, it is actively being considered as part of the official 6G spectrum plan. Additionally, optical or visible light communications (VLC) is emerging as a complementary technology for traditional radio frequency-based wireless communications, made attractive by low-cost hardware, low possibility for interference, high directionality, and a plethora of unlicensed spectrum.

Signal bandwidth requirements are also being identified across these candidate frequency ranges. Nokia envisions the need for 200 MHz of bandwidth per communications channel [12], whereas Huawei expects that 500 MHz to 1 GHz of bandwidth will need to be available to enable advanced use cases [13]. Ericsson, on the other hand, predicts a need from 300 MHz for wide-area communications to 10–15 GHz for high-fidelity local holographic communication in factories and hospitals [14]. It is also predicted that orthogonal frequency division multiplexing (OFDM) waveform currently in use in 5G communications will remain the waveform of choice in 6G networks, as no viable alternative has yet been proposed [15], although non-orthogonal multiple access techniques are also being evaluated [16]. Quadrature Amplitude Modulation (QAM) is also predicted to remain the baseline modulation of choice [17].

C. Intelligence in the Network

In 6G communications networks, AI and machine learning (ML) algorithms will enable real-time inferencing and adaptive intelligence to run a performance-driven network parameter optimization to meet the desired quality of service. An AI-native air interface (AI-AI) is envisioned, where the network itself could learn about and create the most optimal bespoke waveforms for a particular use case based on application-specific needs of spectral efficiency and throughput, as well as the limitations of transceiver hardware [18].

A new addition to the 6G networks will be the ability to offload the AI/ML heavy computation to the network hardware, thus leveraging the edge computing capabilities of the network itself. This will help reduce the battery drain on mobile devices as well as alleviate the need for extremely high-performance on-device computing capabilities. The combination of supervised, unsupervised, reinforcement, federated, and transfer learning will also enable AI-as-a-service (AIaaS), used for intelligent network orchestration and management, dynamic communications protocol refinement, automatic fault finding, identification and fixing, and more adaptive data transmission, resulting in the formation of cognitive networks [19].

D. New Physical Layer Technologies

Many new physical layer technologies are being researched and tested with the aim of supporting the 6G performance goals. Massive MIMO promises to increase throughput capacity, improve directivity, reduce interference, as well as improve spectral and energy efficiency by deploying multiple antennas at the base station, allowing simultaneous transmission and reception of data to and from multiple devices through spatial multiplexing and beamforming techniques [20]. Sensing and localization are expected to be achieved through advanced beam-space processing and will allow accurate mapping of the physical surroundings of the cell site, as well as tracking of users and objects to shape beamforming patterns, reduce interference, and predict handovers [5], [21]. In parallel, intelligent reflective surfaces (IRS) will be used to overcome significant propagation path loss associated with the transmission of mmWave and sub-THz signals. The integration of IRSs into the network to create a Smart Radio Environment (SRE) is expected to help guide signals to improve cell site coverage and energy efficiency through enhanced beamforming capability [22]. Complementing these propagation-control techniques, out-of-band channel estimation will enable intelligent channel estimation across multiple frequencies, including cmWave, mmWave, and sub-THz bands and varying signal bandwidths using channel data gathered at low, e.g., sub-6 GHz, frequencies [23]. Furthermore, full-duplex communications are expected to enable concurrent transmission, reception, and relay of information, requiring a high-performance design of self-interference suppression circuits and innovations in antenna and transceiver circuit design [24]. At a higher level, Cognitive Radio is expected to become the main building block of the entire 6G network infrastructure. These advanced software-defined radio (SDR) systems will be able to reconfigure themselves depending on the required system performance and use case, enabling on-the-fly changes in radio operation by switching between different frequency bands and AI-optimized waveforms occupying different signal bandwidths.

Over the years, software-defined radio technology and its applicability to wireless communications have received

considerable interest in the research community [25], [26]. With the emergence of 6G, a careful analysis of the SDR architectures could position the technology to help achieve the 6G goals.

II. Software-Defined Radio

A. History and Current State

The software-defined radio, or software radio, was introduced to the general public by Mitola in 1992 [27], although initial conceptual frameworks were developed throughout the 70s and 80s by the US Department of Defense, in projects like the Adaptive Antenna Receive System (ADARS) [28], Jam Resistant Communications (JARECO) Emulator [29], Tactical Anti-Jam Programmable Signal Processor (TAJPSP) [30], and others. These projects culminated in 1995 with the U.S. DARPA-Air Force-sponsored project SPEAKeasy [31], which demonstrated the first software-based radio terminal with programmable radio and waveform functions. It featured complete functional decomposition, with most signal processing functions assigned to digital signal processors (DSPs) implemented in FPGAs, and the inclusion of a general-purpose processor [28]. These projects led to the creation of the Joint Tactical Radio System (JTRS). Its goal was to develop a new family of software-based reconfigurable radio systems that would support multiple missions and reduce long-term operations and maintenance costs [32]. Unfortunately, JTRS failed to develop a true software-defined radio, in part due to hardware limitations and in part because both the hardware and the waveform development were contracted to the same firm, resulting in a tight coupling in the developed solution [33].

Today, SDRs are starting to gain traction in the commercial and non-military sectors, and thus, a diversity of designs has begun to emerge. The overall market size in 2024 is estimated to be $31.7 billion, and a projected 10.4% compound annual growth rate (CAGR) [34]. With this traction comes a wide variety of implementations. Whether 6G will drive consolidation to a dominant SDR architecture or whether it will be implemented in many competing SDR architectures remains to be seen.

SDRs are becoming a fundamental building block of current and future wireless communications networks, largely driven by improvements in semiconductor and very large-scale integration (VLSI) technologies, along with advances in computational methods and digital signal processing techniques that have resulted in significant improvements in data converter and programmable logic technologies. The very first SDR systems developed during phase 1 of the SpeakEASY program relied on the fastest available digital signal processor at the time, the Texas Instruments TMS320C40, running at 40 MHz, and resulting in a state-of-the-art SDR that was capable of supporting communication data rates from 75 bps to 10 Mbps [35]. In contrast, in 2025, there are multiple readily available multi-channel direct RF sampling SDR systems capable of processing up to 3 GHz instantaneous signal bandwidth and tunable RF front-end frequency ranges up to 20 GHz [36].

Current SDRs span three price ranges: low-cost hobbyist, mid-range, and high-performance. Hobbyist SDRs ($10–$50) offer limited bandwidth (low MHz), minimal frequency coverage, and require external processing. Mid-range systems ($100–$2,300) provide wider coverage ($\leq$6 GHz), greater bandwidth ($\leq$100 MHz), and may include embedded programmable logic, but require a host computer for signal processing. High-performance SDRs ($5,000–$100,000+) deliver multi-GHz bandwidth, frequency coverage up to 40 GHz, high-resolution converters (12–16 bits), and embedded programmable logic with MCUs. This paper focuses on high-performance embedded SDR architectures in SWaP-constrained platforms (e.g., vehicular, airborne, tactical radios).

B. Topological Groups of Architectures

Three primary groups of topologies have been explored for SDR, as shown in Fig. 1: baseband sampling, intermediate frequency (IF) sampling, and direct RF sampling. The topological grouping of architectures emerges from a set of valid architectures within the combinatorial space of architectural decisions for an SDR. For example, the topology of baseband and IF sampling architectures is similar, except that baseband sampling typically requires the use of an analog IQ mixer and independent digitization of the in-phase (I) and quadrature (Q) portions of the signal. In contrast, the IF sampling architecture can use a single-ended mixer and can digitize the full IF spectrum before digitally splitting it into its corresponding I and Q components.

The sampling function is performed using high-speed data converters (ADCs and DACs). Early SDR systems relied primarily on analog signal processing techniques with limited flexibility. The improvement in data converter technologies allowed signal digitization early in the processing chain (closer to the RF front end), enabling signal modulation, demodulation, filtering, and error correction to be performed fully in the digital domain. This obsoleted the need for certain discrete analog system components. Furthermore, improvements in VLSI technologies allowed the integration of multiple system components on the same semiconductor chip, resulting in MPSoC and RFSoC designs. These SoCs significantly reduce the system complexity through the optimization of the on-chip high-speed and throughput interfaces. This considerably reduces the design complexity and accelerates the development timelines. However, the tightly coupled form and function of system elements also prevents easy replacement of individual system hardware components and can impede system upgradability. Rapid technological development can cause the different components used in SDR systems to quickly become obsolete. The ability to replace individual system components while preserving the overall function of the system could help extend a design's operational lifespan.

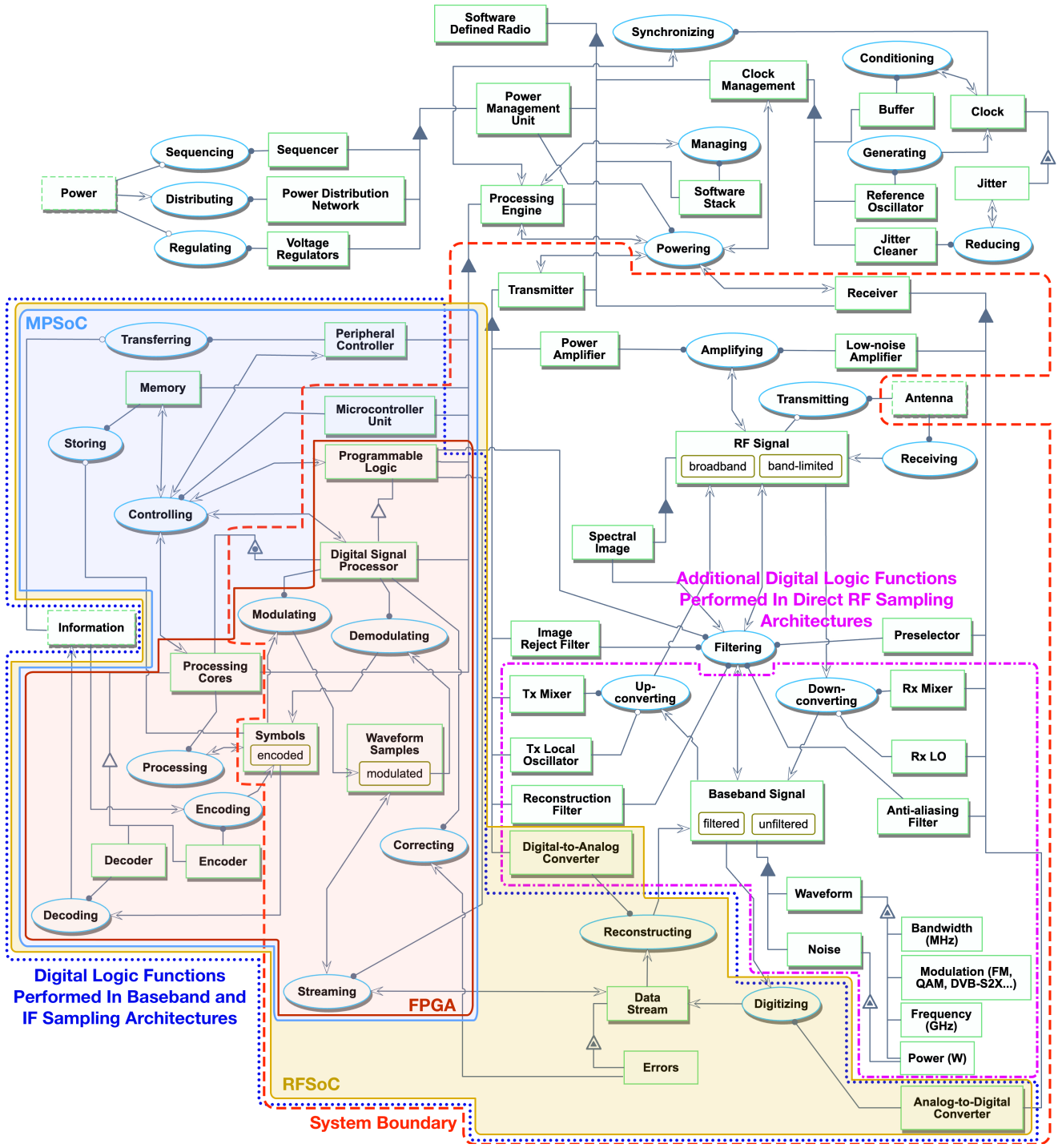


FIGURE 1. SDR system architecture and boundary used for analysis in this paper. The system element groupings show digital functions performed in the digital domain in baseband, IF sampling, and direct RF sampling topologies.

In contrast, a system design made up of individual discrete components allows for easy system upgradability, but is also highly correlated with system complexity. When interconnecting very high-speed data converters with FPGAs or MPSoCs, extremely high interface data rates need to be sustained, eliminating common, pin-inefficient options such as low-voltage differential signaling. In these situations, the designer is often forced to use high-throughput and highly complex interfaces such as a JESD204B/C, which require additional supporting synchronization circuitry and considerable design effort to maintain on-board signal integrity. This "complexity bottleneck" often manifests itself

in significantly increased engineering effort, time, cost, and risk associated with successfully designing, integrating, and verifying the interface.

It remains to be seen whether the popular topological grouping of SDR architectures is borne out as a useful pattern in the design space.

C. System Scope and Boundary

To define the scope of the analysis, we illustrate the components (form) of an SDR and the system boundary used for this analysis in an architectural diagram that traces the signal chain. The chosen diagram language is the Object Process Diagram (OPD) [37], which produces a system representation without much overhead of notation conventions and explicitly separates functions from the form of the system.

In SDRs, software defines functionality, but hardware dictates capability. That is, if the hardware cannot meet the bandwidth or carrier frequency requirements, the performance of the software architecture will be limited. Consequently, the system boundary is drawn around the transceiver (TRX) signal chain that includes both signal-related analog and digital formal elements, as shown in Fig. 1. The elements within the system boundary primarily deal with the processing, conditioning, reception, and transmission of the signal. This includes the amplifying, filtering, downconverting, demodulating, as well as processing, modulating, and upconverting functions. Some of the digital hardware, such as the peripheral controller, MCU, memory, and processing cores, are secondary, supporting elements, and are not primarily involved in signal processing. Therefore, they have been placed outside the system boundary. While the antenna is the main coupling element of the electromagnetic waves, and hence the communication signal, into the SDR, the antenna can also be treated as a standalone system with tens, hundreds, or even thousands of antenna, phase, and amplitude control elements used to enable massive MIMO, beam steering [38] and other advanced techniques to improve spectral and energy efficiency, enhance coverage, and improve the quality of service [20]. As such, the antenna is placed outside of the system boundary and is not considered in the architectural analysis.

Figure 1 also identifies three key function groups that could reside in an FPGA, MPSoC, or RFSoC, indicated in the red, blue, and yellow shaded areas, respectively. FPGAs are integrated circuits with a programmable hardware fabric that combines configurable programmable logic blocks, processing cores, DSP slices, and other elements, and can be reconfigured on demand to perform various logic functions [39]. In the context of an SDR, an FPGA is primarily used for signal processing, which includes the DSP, basic logic, filtering, channelization, and other functions. A MPSoC is a VLSI system that combines an FPGA, a microcontroller unit (MCU), peripheral controllers, and memory blocks, all in a single package [40]. MPSoCs provide compact and robust integration of different signal processing subsystems. This feature makes MPSoCs very attractive for the development and implementation of high-performance SDRs. Recent MPSoC implementations have begun incorporating high-speed ADCs and DACs into a single package, resulting in what is known as an RFSoC. An example of this is an AMD Zynq™ UltraScale+™ RFSoC series [41] and Altera® Direct RF-Series FPGAs [42]. In this analysis, RFSoCs are implementations of the standalone MPSoC and ADC/DAC combinations. That is, RFSoCs are constructed from MPSoCs, that contain FPGAs and MCUs in a single package, and available data converter options. This effectively produces a set of RFSoCs that differ on the basis of data converter options, thus allowing convenient cross-topological comparison. However, RFSoCs differ significantly in space, weight, and power (SWaP) as compared to discrete combinations of MPSoCs and data converters. The area occupied by a single RFSoC is smaller than a discrete combination of an FPGA, an MCU, a DAC, and an ADC, as a result of increased component integrality. How the functions of an SDR are assigned to these three chip types is a central question in the SDR architecture, which is analyzed in the subsequent section.

III. Architectural Decisions for SDR

Architectural decisions are the decisions that most strongly encode system performance [43]. They define the design space by framing it as a set of choices, organized in a morphological matrix. Each architecture is therefore a trace through the morphological matrix, with one option chosen for each decision. We first enumerate a set of candidate architectural decisions based on the system boundary identified Fig. 1, and then check if the previously discussed SDR topologies can be illustrated in this generalized representation. These decisions are then evaluated for their impact on the performance of an SDR, to determine which decision(s) are most architectural. The list of candidate architectural decisions in Table 1 is by no means comprehensive, as there are many other design decisions in a full implementation. However, the remainder of decisions were omitted from the list of decisions due to their hypothesized low impact on system performance.

Some architectural decisions are coupled; i.e. the choice in one architectural decision can force a specific option in another. For example, AD1 and AD2 are coupled. This means that the selection of an MPSoC as the microcontroller unit and programmable logic (AD1|O2,O5) will force the same form (an MPSoC) to be used in AD2 for digital signal processing (AD2|O2). Furthermore, coupling can also extend to specific form options within architectural decisions. For example, both a discrete MCU (O1) and an FPGA (O4) in AD1 are needed for the correct SDR functionality. In this paper, the coupling between architectural decisions and options is strictly enforced to reduce the number of SDR architectures for analysis.

TABLE 1. Morphological matrix of SDR architectural decisions, formal elements, and their specific options.

ID	Architectural Decision	Generic form	Opt. ID	Specific form
AD1	Controlling and Coordinating the Operation of System Components	Microcontroller Unit	O1	General Purpose (Discrete MCU)
			O2	MPSoC
			O3	RFSoC
		Programmable Logic	O4	FPGA
			O5	MPSoC
			O6	RFSoC
AD2	Modulating, Demodulating, Channelizing, and Filtering the Signal Data	Digital Signal Processor	O1	FPGA
			O2	MPSoC
			O3	RFSoC
AD3	Amplifying the Transmit Signal	Power Amplifier	O1	Class A
			O2	Class AB
			O3	Class B
			O6	Class E
			O7	Distributed
AD4	Filtering the Signal Image Created During the Upconversion Process	Image Reject Filter	O5	Cavity
			O6	Planar — Thin Film
AD5	Upconverting the Signal from Baseband or Intermediate Frequency to RF for Transmission	Tx Mixer	O1	Balanced
			O2	Double Balanced
			O3	Triple Balanced
			O4	Image Reject / Single Sideband
			O5	IQ
			O6	Digital
AD6	Supplying the Up/Downconversion Local Oscillator Tone	Local Oscillator	O1	PLDRO
			O2	DDS
			O3	VCO
			O4	NCO
AD7	Removing High-Frequency Transients After DAC Reconstruction	Reconstruction Filter	O1	Acoustic (SAW/BAW)
			O2	Ceramic
			O3	Lumped Element (LC)
AD8	Converting Discrete-Time Samples to Continuous Analog Signals	Digital-to-Analog Converter	O1	Interleaved
			O2	Switched-Capacitor
			O3	Current-Steering
AD9	Amplifying the Received Signal	Low-Noise Amplifier	O1	Cascode
			O2	Common-Base or Common-Gate
			O3	Distributed
			O4	Resistive Feedback
AD10	Filtering Out Unwanted Signals	Preselector	O5	Cavity
			O6	Planar
AD11	Downconverting the Signal to Baseband or Intermediate Frequency	Rx Mixer	O1	Balanced
			O2	Double Balanced
			O3	Triple Balanced
			O4	Image Reject / Single Sideband
			O5	IQ
			O6	Digital
AD12	Filtering Out Frequency Components in Higher Nyquist Zones	Anti-Aliasing Filter	O2	Acoustic (SAW/BAW)
			O3	Ceramic
			O4	Lumped Element (LC)
AD13	Sampling and Quantizing the Analog Signal	Analog-to-Digital Converter	O3	Pipelined
			O4	Time-Interleaved
			O5	Flash
			O6	Folding

A. Model Assumptions and Constants

From an SDR hardware perspective, the main parameters of interest are maximum signal channel bandwidth, frequency range, transmitter output power, and receiver sensitivity or noise floor. It is assumed that the same OFDM QAM modulated waveform, with varying modulation depths and sampling rates, will be used in 6G communications as in the 5G new radio standard [15], [17]. In this paper, the SDR architectures target the mid-band, or cmWave, spectrum, the most promising new candidate for 6G communications. Therefore, an SDR operating in this frequency range would need to aim to satisfy the requirements outlined in Table 2. The SDR architectures in the following sections will be evaluated and compared in light of this specification.

The SDR is assumed to handle the correct sequencing of the power rails, an efficient distribution of the power throughout the system, and the correct regulation of the voltage rails with supply noise and ripple sufficiently low so that it does not impact TRX performance. Power sequencing, as well as the peripheral controller, memory, and the information processing cores are not primary components involved in the

TABLE 2. Proposed SDR Specifications for Mid-Band 6G

Parameter	Value
Frequency Range	1–15.350 GHz [44]
Aggregated Signal BW	200–500 MHz per channel [12], [13], [44]
Transmitter Output Power	22–40 dBm [45], [46]
Receiver Ref. Sensitivity	−79.6 dBm for QPSK, based on the n96 band data and adjusted for 200 MHz bandwidth [47]

TABLE 3. Single-attribute utility mapping to SDR sub-systems

Utility Metric	Mapping
Error Vector Magnitude	Transmitter
Quantization Signal-to-Noise Ratio	Transmitter and Receiver
Maximum Signal Processing Bandwidth	Transmitter and Receiver
Maximum Frequency Coverage	Transmitter and Receiver
Sensitivity	Receiver
Quasi-Selectivity	Receiver
Area	Auxiliary (system)
Power Consumption	Auxiliary (system)

TRX signal chain. Thus, they are excluded from the system boundary.

The clock management unit is assumed to provide and distribute the desired stable, low-phase noise reference clock. The phase noise of the reference is expected to be better than that of all other form elements of the SDR. It is also assumed that the sampling is performed on real signals with the highest frequency within the 1st Nyquist zone. This allows a direct comparison between different options of ADCs and DACs and avoids the need to quantify jitter-related signal errors that can result from the undersampling of communications signals. It is also assumed that a correct interface, such as JESD204B/C, Interlaken, or LVDS, is used to interface data converters, programmable logic blocks, and other discrete system elements. Therefore, this work does not assess the performance of chip interconnect frameworks and protocols.

IV. Single-Channel SDR Evaluation Metrics

A. Definition of Multi-Attribute Utility

To assess the performance and contrast different SDR system architectures, a multi-attribute utility (MAU) was defined. This constitutes the core of the analysis, by establishing a direct comparison between all architectures, allowing for their visualization in a tradespace and the identification of patterns. The MAU is a weighted average linear combination of individual single attribute utilities (SAUs) and is defined as

$$U_{MA} = \frac{\mathbf{w} \cdot \mathbf{U}}{\sum_{n=i}^{m} w_i} \tag{1}$$

where $\mathbf{w}$ and $\mathbf{U}$ are the weight vector and the 1-dimensional matrix of individual i utilities, respectively.

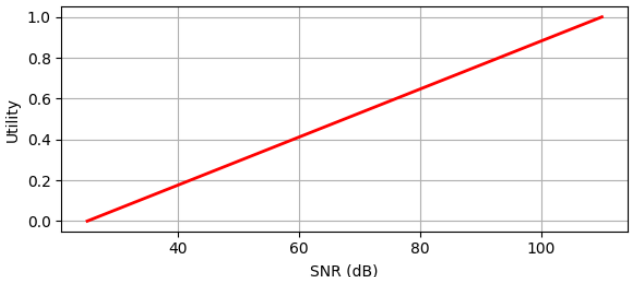


FIGURE 2. Quantization signal-to-noise ratio utility function. The minimum utility is achieved at or below 25 dB SNR, and the maximum at or above 110 dB.

As shown in Table 3, there are eight unique SAUs that are assigned to three separate SDR subsystems: receiver, transmitter, and auxiliary. Although MAU combines all single-attribute utilities into a single weighted average utility metric, the segmentation of utilities helps to identify the main system component targeted by a specific utility. In addition, some utilities are common and thus shared between the transmitter and receiver, and some are unique. All maximum and minimum utility function values are selected considering the requirements outlined in Table 2, considering a 1024-QAM OFDM signal.

B. Receiver Utilities

1) Quantization Signal-to-Noise Ratio

The first receiver utility is the quantization signal-to-noise ratio of the ADC, which can be defined as

$$\text{SNR (dB)} = 6.02N + 1.76 + 10\log_{10}\frac{F_s}{2B} \tag{2}$$

where N is the ADC bit depth in bits, F_s is the sampling frequency in Hz, and B is the signal bandwidth in Hz [48]. For this linearly increasing utility, the higher the SNR, the better, as shown in Fig. 2, with the maximum achieved at 110 dB and the minimum at 25 dB. The significance of this utility lies in its ability to minimize the overall noise of the receiver, thus minimizing the bit-error rate of the entire SDR system.

2) Sensitivity

Receiver sensitivity can be defined as

$$\text{Sens. (dBm)} = -174 + 10\log_{10}(B) + F + (C/N)_{Req}\,, \tag{3}$$

where F is the noise figure of the system in dB and $(C/N)_{Req}$ is the minimum required carrier-to-noise ratio in dB.

It is assumed that QAM with varying modulation orders will remain the dominant modulation scheme in 6G [49]. As the exact waveform parameters are not yet known, a 1024-QAM Wi-Fi 6 waveform with parameters summarized in Table 4, is used in this analysis. In (3), the signal bandwidth is assumed to be known and is set to 500 MHz. The required carrier-to-noise ratio is dictated by the modulation scheme

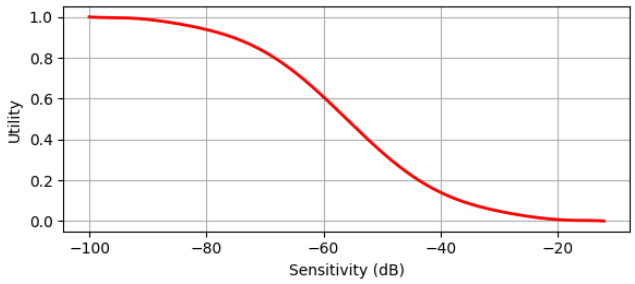


FIGURE 3. Receiver sensitivity utility achieving its maximum at or below -100 dB and minimum at or above -12 dB.

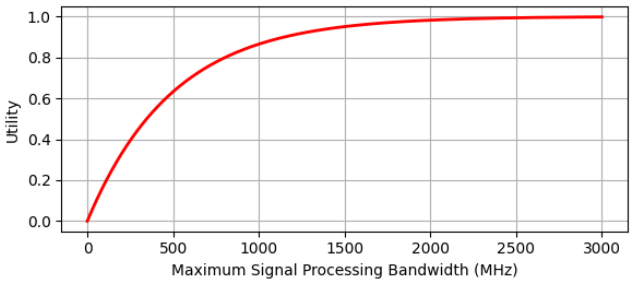


FIGURE 4. Maximum signal processing and generation bandwidth utility function. The maximum is achieved at and above 3000 MHz, and no utility is derived at 0 MHz.

and the target error performance. The receiver sensitivity is measured at 95% of throughput [47], which corresponds to a block error rate (BLER) $\leq$ 10%. To obtain a conservative energy per bit to noise ratio (E_b/N_0), we decouple from the 3GPP BLER criterion and adopt an uncoded simplified model with a transport block size of 1 bit. Under this assumption, a 95% throughput target corresponds to BER of 5%, which for 1024-QAM over an additive white Gaussian noise Rayleigh fading channel is achieved at 16.5 dB [50]. The relationship between (E_b/N_o) and carrier-to-noise is defined as

$$\frac{C}{N} = \frac{E_b}{N_o} + 10\log_{10}(\frac{R_b}{B}), \tag{4}$$

where R_b is the channel bit rate, which can be computed as

$$R_b = \frac{N_{bps} \cdot \frac{B}{SCS} \cdot R_c}{T_{GID} + T_{SD}}, \tag{5}$$

with N_{bps} corresponding to the number of bits per symbol, SCS is the OFDM subcarrier spacing, R_c is the coding rate, and T_{GID} and T_{SD} are the guard interval and symbol duration, respectively. Substituting parameters from Table 4 into (4 – 5) yields a theoretical data rate of 3.53 Gbps and a required carrier-to-noise ratio of 25 dB.

The total noise figure (F) of the cascaded system elements can be computed as

$$F\ (\text{dB}) = 10\log_{10}\left(F_1 + \sum_{i=2}^{M} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j}\right) \tag{6}$$

Where F_1 and F_i are the noise factors of the first and i-th system elements, and G_j is the available gain of the j-th system element. For linear passive devices, including mixers, the noise figure is equal to their insertion or conversion loss.

TABLE 4. 1024-QAM OFDM signal bit rate parameter assumptions

Parameter	Description	Value
N_{bps}	Number of bits per symbol	10
SCS	Subcarrier spacing	78.125 kHz
T_{GID}	Symbol guard interval	0.8 μs
T_{SD}	Symbol duration	12.8 μs
R_c	Coding rate	3/4

The ADC noise figure at room temperature is computed as

$$F_{\text{ADC}}(\text{dB}) = 10\log_{10}\left(\frac{V_{p-p}^2}{4\,Z_{\text{In}}\,F_s}\right) + 30 + 174 - \text{SNR} \tag{7}$$

where V_{p-p} is the full-scale voltage swing and Z_{In} is the input impedance of the ADC [51]. The defined sensitivity utility function is shown in Fig. 3.

3) Maximum Signal Processing Bandwidth

Although the assumed base-case signal bandwidth is 500 MHz, the receiver should also be evaluated for the maximum possible signal processing bandwidth. This is important for SDR systems, as the signal modulation scheme and the corresponding occupied bandwidth can be changed programmatically. The maximum processing bandwidth of real signals is governed by the Nyquist theorem and is equal to half of the sampling rate. In this utility, the higher the processing bandwidth, the better as shown in Fig. 4 with the maximum utility achieved at 3 GHz.

4) Maximum Frequency Coverage

The maximum receiver frequency coverage utility is normalized to the target mid-band SDR frequency of 15.350 GHz. The utility is defined as

$$MFC(f) = \frac{f_{tuning}}{15.35} = \frac{f_{Tun_{IF}} + \sum_{n=1}^{m} f_{Tun_{LO_i}}}{15.35} \tag{8}$$

where f_{tuning} is the maximum tuning frequency range in GHz computed as a linear sum of all frequency tunable local oscillators in the system ($\sum_{n=1}^{m} f_{Tun_{LO_i}}$) and the maximum frequency of the IF processing stage ($f_{Tun_{IF}}$), which is equal to the Maximum Signal Processing Bandwidth. For a direct conversion receiver, the value f_{tuning} is the same as the maximum signal processing bandwidth. The graphical representation of the utility is shown in Fig. 5, where the utility exhibits a linear increase with increasing frequency coverage.

5) Quasi-Selectivity Utility

Receiver selectivity is a critical parameter in communications receivers and is difficult to calculate analytically. It is usually

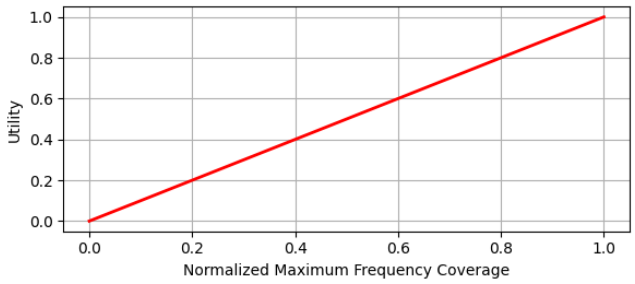


FIGURE 5. **Maximum frequency coverage utility function. The maximum is achieved for the full frequency coverage of 15.35 GHz, and the minimum for 0 GHz.**

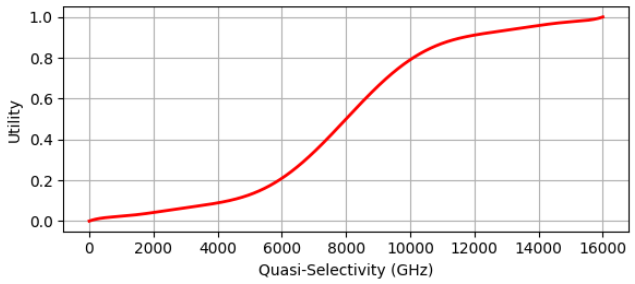


FIGURE 6. **Quasi-selectivity utility achieving the maximum at 16000 and minimum at 0.**

measured directly and is predominantly governed by filter selection. For tradespace analysis, a quasi-selectivity utility is defined as

$$QS = \frac{\sum_{n=1}^{m} Q_n \cdot f_{span_n}}{15.35} \tag{9}$$

where Q_n is a typical Q factor of the n-th filter in the receiver chain, f_{span_n} is the typical usable frequency span of a particular filter type in GHz [52], and m is the total number of filters in the receiver chain. The graphical representation of this utility function is shown in Fig. 6.

C. Transmitter Utilities

1) Error Vector Magnitude

One of the most popular metrics for assessing the combined impact of system-level impairments on signal quality is the error vector magnitude (EVM) defined as

$$EVM^2 = EVM_N^2 + EVM_{PN}^2 + EVM_{Lin}^2 \, . \tag{10}$$

and its utility function is plotted in Fig. 7. In (10), EVM_N^2 is the error vector magnitude contribution due to the additive white Gaussian noise, defined as

$$EVM_N = NSD + 10\log_{10}(B) + PAPR + P_{BO} + 3 \, , \tag{11}$$

where NSD is the noise spectral density of the DAC in dB, $PAPR$ is the peak-to-average power ratio of the signal in dB, and P_{BO} is the signal power backoff from the full-scale range of the DAC [53]. In this analysis, it is assumed that the full range of the DAC is utilized, therefore $P_{BO} = 0$ dB, and that a 1024-QAM OFDM signal exhibits $PAPR$ of 11 dB.

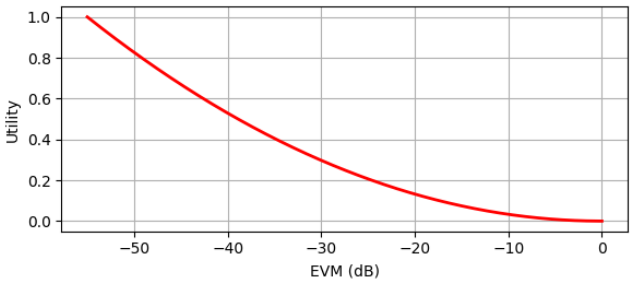


FIGURE 7. **Graphical representation of the EVM utility function showing that the maximum is achieved at or below -55 dB and minimum at 0 dB.**

The EVM_{PN} is the error vector magnitude contribution arising from the phase noise in the signal chain. To compute the total transmitter phase noise ($\mathcal{L}_{\mathrm{TX}}$) and hence its EVM contribution, a linear superposition of the phase noise of each frequency-generating component in the RF chain needs to be computed as

$$\mathcal{L}_{\mathrm{TX}} = 10\log_{10}(l_{\mathrm{IF}}^2 + \sum_{n=1}^{m} l_{\mathrm{LO_n}}^2) \tag{12}$$

where $l_{\mathrm{LO_n}}$ is the integrated phase noise contribution of each local oscillator used in the system in dBc/Hz, and l_{IF} is the linear representation of the signal phase noise generated by the system DAC, defined as

$$\mathcal{L}_{\mathrm{IF}} = \mathcal{L}_{\mathrm{CLK}} + 20\log_{10}\left(\frac{f_{\mathrm{IF}}}{f_{\mathrm{CLK}}}\right) \, , \tag{13}$$

where $\mathcal{L}_{\mathrm{CLK}}$ is the phase noise of the DAC clock signal in dBc/Hz, f_{IF} is the DAC-generated signal frequency in Hz, and f_{CLK} is the DAC clock frequency. The total transmitter EVM due to phase noise can then be computed as

$$EVM_{PN} = 10\log_{10}\left(10^{\frac{\mathcal{L}_{\mathrm{IF}}}{10}} + \sum_{n=1}^{m} 10^{\frac{\mathcal{L}_{\mathrm{LO_n}}}{10}}\right) + 3 \tag{14}$$

The last EVM component in (10) is related to system (non)-linearity and can be defined as

$$EVM_{Lin} = 2P_{RMS} - 2OIP_3 + 3 \, , \tag{15}$$

where P_{RMS} is the root-mean-square value of the signal power, OIP_3 is the 3rd order intercept point of the system, which, for a cascaded system, is computed as

$$OIP_3 = \left(\sum_{k=1}^{n} \frac{1}{OIP_{3,k}\prod_{j=k+1}^{n} G_j}\right)^{-1} \tag{16}$$

where G_n and $OIP_{3,n}$ are the gain and the OIP_3 of the n-th cascaded system elements, respectively [54].

2) Quantization Signal-to-Noise Ratio

This transmitter utility mimics that of the receiver utility and is defined as

$$\mathrm{SNR\ (dB)} = 6.02N + 1.76 + 10\log_{10}\frac{F_s}{2B} \, . \tag{17}$$

It models the in-band, quantization-limited SNR of an N-bit DAC. Quantization noise is assumed to be white across the 1st Nyquist zone. This linearly increasing utility achieves maximum at 110 dB and the minimum at 25 dB, as shown in Fig. 2. Minimizing the QSNR of the DAC, helps to improve the transmitter EVM.

3) Maximum Signal Generation Bandwidth

This utility quantifies the maximum contiguous transmit bandwidth the DAC can synthesize while still meeting linearity and spectral mask requirements. In an SDR, this is particularly important for channel aggregation, wideband modulation, and reconfiguration without hardware changes. A real-output DAC can only generate unique signal content up to the limit of the 1st Nyquist zone, which extends to half of the sampling rate. This utility increases with increasing bandwidth and reaches maximum at 3 GHz as shown in Fig. 4.

4) Maximum Frequency Coverage

The maximum transmitter frequency-coverage utility is obtained by normalizing the highest RF output frequency the transmitter can generate to the target frequency of 15.35 GHz. The highest transmitter RF output frequency is determined by the available LO tuning range together with the maximum IF or baseband output frequency supported by the transmit chain. For a direct RF sampling transmitter, frequency coverage is determined by the maximum DAC signal generation bandwidth. The utility increases linearly with the normalized transmit frequency coverage as shown in Fig. 5.

D. Auxiliary Utilities

1) Area

Area utility is computed by adding up the area occupied by individual system components and is defined as

$$A_{\text{Total}} = \sum_{n=1}^{m} A_n \ , \tag{18}$$

where A is the area of the n-th system element in millimeters squared (mm^2). The graphical representation of this utility function is illustrated in Fig. 8, and the maximum value is achieved when the occupied area is minimized.

2) Power Consumption

The power consumption of the system is defined as

$$P_{DC_{Total}} = \sum_{n=1}^{m} P_{DC_n} \tag{19}$$

where P_{DC_n} is the DC power consumption of the n-th system element in W. In this calculation, special attention is paid to the power amplifier in the transmit chain as

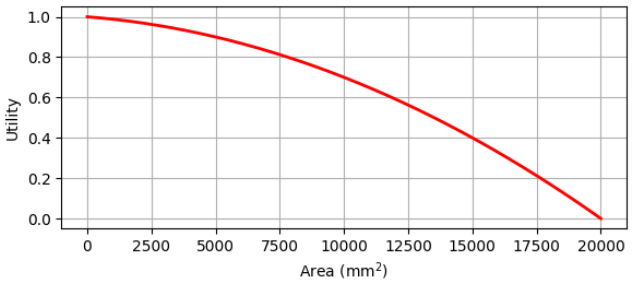


FIGURE 8. Area utility illustrating the decrease in the utility value as the area occupied by system components increases.

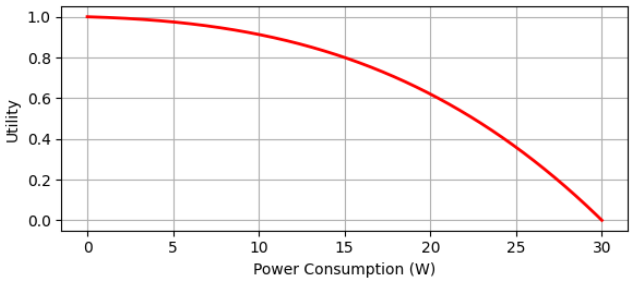


FIGURE 9. Power consumption utility function with the maximum achieved at 0 W of power consumption, and the minimum at or above 30 W.

different levels of power-added efficiency (PAE) are achieved based on the class of power amplifier operation. PAE can be computed as

$$\text{PAE}(\%) = \frac{P_{\text{Out}} - P_{\text{In}}}{P_{\text{DC}}} \cdot 100\% \tag{20}$$

where P_{Out} and P_{In} are the signal output and input powers, respectively. The graphical representation of the power consumption utility function is shown in Fig. 9.

3) Cost

The system bill-of-materials (BOM) cost is computed for a given architecture by adding up the costs of the selected options for each architectural decision as

$$C_{System} = \sum_{n=1}^{m} C_n \ , \tag{21}$$

where C_n is the cost of the n-th system element. The market cost for each system architectural decision option was determined by collecting the average cost from the principal component suppliers.

E. Utility Weights

The weights assigned to each utility are assigned by their relative importance within transmitter, receiver, and auxiliary sub-systems according to expected impact on communications link quality, usable frequency range, and mobile deployment feasibility of the target SDRs for mid-band 6G communications. These weights are assigned on a 5-point scale, where 5 denotes the highest importance, 4 high

TABLE 5. Weights and Mapping of Single-Attribute Utilities

Metric	Transmitter	Receiver	Auxiliary
Error Vector Magnitude	5	-	-
Quantization Signal-to-Noise Ratio	2	3	-
Max. Signal Processing Bandwidth	2	2	-
Max. Frequency Coverage	3	3	-
Sensitivity	-	5	-
Quasi-Selectivity	-	4	-
Area	-	-	1
Power Consumption	-	-	3
Total System MAU Contribution	36.4 %	51.5 %	12.1 %

importance, 3 moderate importance, 2 low importance, and 1 the lowest importance, and are listed in Table 5. The assigned utility weights are not meant to be universally optimal for all SDR systems. Rather, they are intended to provide a consistent comparative basis for valid mid-band 6G-capable SDR architectures and serve to define a baseline reference scenario. A different application might warrant a change in weighting, which would result in potentially different ranking of the generated system architectures.

The maximum weights were assigned to the EVM and the Sensitivity utilities in the transmitter and receiver subsystems, respectively. For the receiver, selectivity is also of significant importance, therefore the quasi-selectivity utility weight is set to 4. The maximum frequency coverage utility is assigned a weight of 3, as, depending on the system application, a useful SDR can still be manufactured even with reduced frequency coverage instead of spanning the full 15 GHz range. Similarly, quantization noise is also an important utility, but it is more important in the radio receiver; therefore, the weights are assigned as 3 and 2, respectively. The reduction in receiver noise allows for wider dynamic range and better system sensitivity, thus allowing the reception of lower-power signals with reduced bit error rates.

In the auxiliary group, the area and power consumption utilities are assigned the weights of 1 and 3, respectively. Power consumption is very important in any mobile system that relies on the power supplied by the onboard batteries. The increase in power consumption leads to an increased power dissipation. This, in turn, leads to the requirement for efficient heat extraction, thus necessitating heatsinking solutions, which in turn increase the weight and size of the radio unit. The area constraint, however, is primarily important for handsets and man-packs, where space comes at a premium. The transmitter, receiver, and auxiliary subsystem contributions of 36.4%, 51.5%, and 12.1%, respectively, to the total system MAU shown in Table 5 are obtained by summing the individual utility weights within each subsystem and normalizing them by the sum of all individual utility weights.

V. Single-Channel SDR Tradespace Analysis

A. Tradespace Definition

In order examine which decisions are most impactful on the performance of an SDR, we construct a tradespace by evaluating each of the traces through the morphological matrix, and plotting them on cost vs. MAU axes. Tradespace analysis is a method to visualize the combinatorial complexity of many interacting decisions [43]. It can also identify clustering in the design space, and can be used to determine whether any architectural decision choices are clearly dominated by others.

The tradespace analysis incorporated all architectural decisions within the system boundary, as detailed in Table 1. To create the tradespace, quantitative parameters for each architectural decision were collected and detailed in [55]. This analysis explored three groups of topological SDR architectures: baseband, IF, and direct RF sampling. Each of the identified topological groups of architectures has the same emergent functions set (enabling software-defined radios), albeit with varying degrees of performance. First, we examine the three primary clusters to understand what decision(s) create discontinuities in performance. Second, we evaluate subsystem-centric architectures to understand how they create tradeoffs at the system level. Third, we conduct a main-effects analysis to prioritize which architectural decisions have the strongest influence on the performance of an SDR.

The combination of all architectural decisions and their options yielded 2,024,640 unique SRD architectures. The generated tradespace is shown in Fig. 10. The architecture that minimizes the vector distance to the utopia point ($U = (c_u, u_u) = (0, 1)$) on the tradespace is designated as a

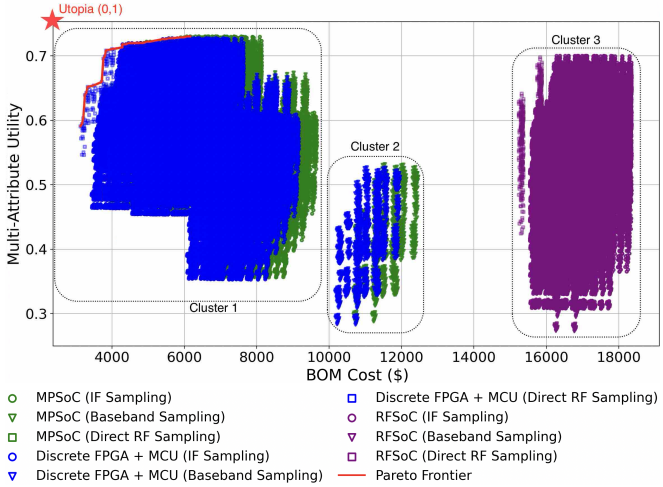


FIGURE 10. The architectural tradespace showing 2,024,640 different SDR architectures across three different topologies: baseband sampling, IF sampling, and direct RF sampling. Pareto frontier and utopia point are also identified on the plot.

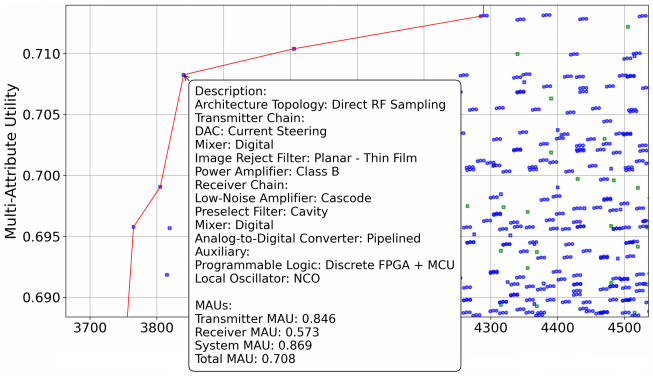


FIGURE 11. Baseline SDR architecture on the Pareto frontier minimizing the distance to the utopia point.

baseline architecture ($\mathbf{A_{Base}}^*$), and is identified as

$$\mathbf{A_{Base}}^* = \underset{(c_i,u_i)\in P}{\arg\min} \left[\sqrt{(c_i - c_u)^2 + (u_i - u_u)^2}\right] \tag{22}$$

where $P \subseteq A$ denotes the Pareto frontier, identified in a red line on the tradespace, which consists of the non-dominated architectures within the full set of generated SDR architectures $A = (c_1, u_1), (c_2, u_2), \ldots, (c_n, u_n)$ and defined as

$$P = \big\{(c,u) \in A \;\big|\; \nexists\,(c',u') \in A \text{ with } (c',u') \neq (c,u) \text{ and } c' \leq c \text{ and } u' \geq u\big\}\,. \tag{23}$$

The baseline architecture, as shown in Fig. 11, achieves the MAU of 0.708 using the direct RF sampling topology. This is a surprising result, as the IF sampling architecture has been the most popular radio architecture for decades [56] and direct RF sampling is a relatively new topology enabling high-performance software-defined radios. This is an indication of significant technological advances made in data converter and programmable logic technologies.

There are three distinct architectural clusters in Fig. 10, which are primarily differentiated by the data converter architectural decision. The architectures in the leftmost cluster (Cluster 1) offer a good trade-off between the system performance and the system BOM cost. Within this cluster, multiple topologies are present, with the direct RF and IF sampling architectures consistently achieving greater performance compared to those employing the baseband sampling topology. Although direct RF sampling results in lower overall system cost, the MAU envelope of the IF sampling topology is higher overall. This increase in utility can be explained by the improved selectivity of the system due to the increased number of filters and an added frequency tuning stage in the system, which expands the frequency coverage. However, this performance gain with IF sampling comes at an increased system cost, occupied board area, and power consumption due to the additional components.

Cluster 2 contains architectures exhibiting significantly lower MAU (maximum of 0.532), as well as increased system cost. The architectures in this cluster are comprised only of baseband sampling architectures, and all incorporate flash ADCs. Flash ADCs have a considerably lower bit depth compared to other analog-to-digital converters, resulting in low receiver sensitivity, quantization signal-to-noise ratio, and other single-attribute utilities. Furthermore, baseband sampling requires one anti-aliasing filter and ADC for each I and Q signal path, thus increasing the overall number of components in the receiver chain compared to other architectures. This leads to an increase in the occupied board area, power dissipation, and system cost, making this set of architectures unattractive for use in SDRs.

Cluster 3 is associated with the selection of RFSoC as an architectural decision. This cluster of architectures exhibits both high variability of the system utility and an overall high cost. RFSoCs generally include a higher number of data converters (2, 4 or even 8 ADC and DAC pairs) within a single package. This considerably increases the overall system cost and power consumption, but preserves the same board area as the MPSoC and a smaller area than discrete FPGA and MCU implementations. The analysis of single-channel SDR systems shows that RFSoC-based SDR implementations are less competitive in terms of cost. However, in multi-channel SDR systems, as shown in Section VI, the RFSoCs are highly competitive on both cost and MAU metrics.

Another way to analyze the tradespace is to assess the transmitter, receiver, and auxiliary subsystem utilities individually, to find the architectures that maximize performance of each subsystem in turn, but at the cost of sub-optimizing the system performance. To accomplish this, the computed multi-attribute utilities for each subsystem are normalized to the sum of the weights associated solely with the utilities mapped to those specific subsystems. For example, the multi-attribute utility corresponding to the transmitter portion of the SDR is computed using (1) by considering only the single-attribute utilities in the transmitter column of Table 5. The same rationale is applied to the computation of receiver-centric and auxiliary-centric analyses. One transmitter-centric architecture was selected on the Pareto frontier according to (22), which scored an MAU of 0.846. When the tradespace is constructed using only the transmitter utilities, all of transmitter-centric architectures on the Pareto frontier employ a direct RF sampling topology, further illustrating the power of the use of modern RF data converters in software-defined radios. In contrast, the Pareto-efficient receiver-centric architectures (when scored only against the receiver utiliy) are all comprised of IF sampling topologies, implying that high-performance SDR receivers employing analog down-conversion benefit from multi-stage filtering, extended frequency tuning, and the ability to leverage very high bit-depth ADCs that are not available at high sampling rates [55]. Overall, receiver-centric architectures tend to exhibit systematically lower MAUs compared to the transmitter-centric architectures. A receiver-centric architecture on the Pareto frontier obtained using (22) results in the

TABLE 6. Transmitter-, receiver-, auxiliary-centric, and baseline SDR architectures, their decisions, and multi-attribute utilities.

Parameters	Transmitter-Centric	Receiver-Centric	Auxiliary-Centric	Baseline Architecture
Topology	Direct RF Sampling	IF Sampling	Direct RF Sampling	Direct RF Sampling
Digital-to-Analog Converter	Current Steering	Switched-Capacitor	Current Steering	Current Steering
Reconstruction filter	–	Lumped Element (LC)	–	–
Tx Mixer	Digital	Balanced	Digital	Digital
Image Reject Filter	Planar - Thin Film	Planar - Thin Film	Planar - Thin Film	Planar - Thin Film
Power Amplifier	Class B	Class B	Class E	Class B
Low-Noise Amplifier	Common-Base or Gate	Cascode	Common-Base Gate	Cascode
Preselect Filter	Planar - Thin Film	Cavity	Planar - Thin Film	Cavity
Rx Mixer	Digital	Balanced	Digital	Digital
Anti-Aliasing Filter	–	Acoustic	–	–
Analog-To-Digital Converter	Pipelined	Pipelined	Pipelined	Pipelined
Programmable Logic	Discrete MCU + FPGA	Discrete MCU + FPGA	Discrete MCU + FPGA	Discrete MCU + FPGA
Local Oscillator	NCO	VCO	NCO	NCO
Transmitter MAU	0.846	0.404	0.572	0.846
Receiver MAU	0.439	0.606	0.439	0.573
Auxiliary MAU	0.874	0.908	0.929	0.870
Total SDR Architecture MAU	0.639	0.570	0.547	0.708

receiver MAU of 0.608. Finally, analyzing auxiliary-centric architectures reveals that the auxiliary utility is maximized with the direct RF sampling topology, as with the transmitter-centric group. The auxiliary-centric utilities tend to be systematically high compared to the transmitter and receiver, which indicates that efficient combinations of low-cost, low-surface-area and low-power architectural decision options are simultaneously achievable. The baseline auxiliary-centric architecture achieves a system MAU of 0.929. The performance summary of the transmitter-, receiver-, and auxiliary-centric subsystem architectures and the list of their individual architectural decisions are shown in Table 6.

B. Tensions in the Design Space

As can be seen in Table 6, the transmitter-centric SDR architecture results in a significantly underperforming receiver choices (MAU of 0.439), while the auxiliary-centric group produces performance close to a baseline SDR architecture. Interestingly, the transmitter architectural decisions of the transmitter-centric architecture are identical to those of the transmitter in the baseline SDR architecture, suggesting that for this SDR architecture on the Pareto frontier, trade-offs primarily exist between the receiver and the auxiliary group of architectural decisions.

The receiver-centric architecture achieves a MAU of 0.608, but does so by reducing the transmitter MAU by over 50%. Furthermore, the receiver-centric architecture calls for a complete topological change compared to the transmitter, moving from direct RF sampling to IF sampling. This creates a tension between the system topologies as well as the transmitter and receiver architectural decisions, suggesting that the system could have greater overall utility with a mixed-topology TRX chain.

Finally, the auxiliary-centric SDR architecture is severely suboptimal in MAU for both the transmitter and receiver. This highlights an important trade-off between the space and power metrics and the performance of the TRX chain itself. Furthermore, the composition of the receiver in the auxiliary-centric architecture is the same as that found in the transmitter-centric architecture. The primary differences are observed in the transmitter chain, namely in the DAC and the power amplifier architectural decisions. The MAU of the auxiliary subsystem is maximized by minimizing power consumption and board area. Since Class E power amplifiers are the most efficient in the architectural decision options considered, this option is expected to have a significant effect on the auxiliary utility. However, since Class E power amplifiers have the lowest OIP_3 out of all power amplifier options, resulting in reduced EVM performance, thus penalizing this architectural decision option in the transmitter chain [55].

C. Prioritizing Architectural Decisions for a Single-Channel SDR System

When architecting systems it is important to understand which decisions have the strongest influence on performance, as these decisions merit more careful analysis. This can be analyzed by performing the main effect analysis [57] on the tradespace results in Fig. 10. System performance is most sensitive to the architectural decision of the analog-to-digital converter with the main effect of 0.0604, as seen in Fig. 12. This result is expected because the performance of the ADC is the main driver behind most receiver utilities. This also indirectly highlights the need for ADC technology improve-

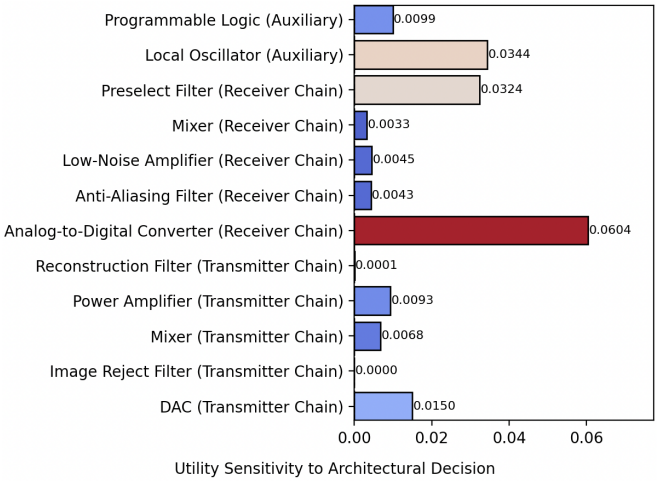


FIGURE 12. Main effect-based sensitivity analysis of a single-channel SDR system multi-attribute utility to individual architectural decisions.

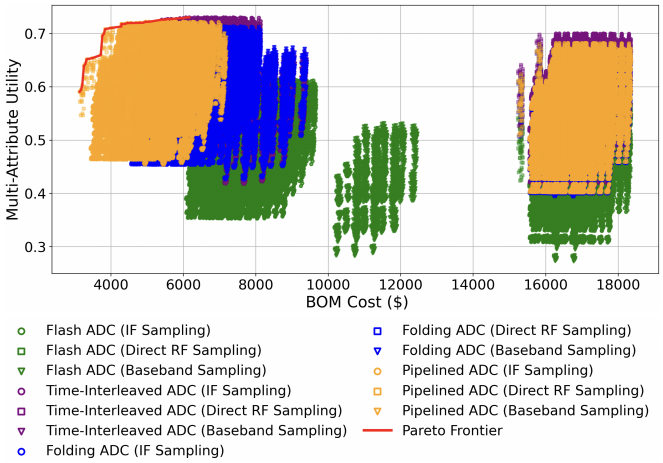


FIGURE 13. Tradespace showing distribution of SDR system architectures across all three topologies, colored by the ADC architectural decision option.

ment to enhance the performance of software-defined radio architectures if the goals of 6G are to be achieved. This statement is also backed up by current market trends, where available off-the-shelf ADCs tend to have lower sampling rates and overall lower bit depth compared to DACs in the same category. The price differential is also substantial between the two types of data converters [55]. What is surprising, however, is that the SDR architectures appear to be 75% less sensitive to the selection of digital-to-analog converters compared to ADCs. Although the sampling rate and bit depth are indeed higher, the DAC performance is driving the performance of the physical waveform generation, transforming the digital bit stream into an analog waveform. Therefore, it is expected to have a significant impact on overall system performance. However, it appears that (based on the utility weights evaluated) DACs are very capable devices to produce clean, low-EVM waveforms, which maximize those utilities.

The sensitivity to the local oscillator and preselect filter is also an interesting result. The primary function of the local oscillator is to provide a fixed or tunable tone that can be modulated by the baseband waveform in the upconversion path (transmitter), or alternatively, it is used to remove the carrier or downconvert the communications signal to intermediate frequency in the downconversion (receiver) path. It appears that the SDR system is highly sensitive to the local oscillator options, which are primarily driving the utilities through the tunable range and phase noise figures of merit. The preselect filter, on the other hand, appears to have a significant effect on the receiver chain due to its cascaded effect on the SDR selectivity and noise figure, impacting the quasi-selectivity and sensitivity utilities, respectively. Furthermore, as can be observed from Fig. 12, some architectural decisions result in a negligible or no effect on performance, notably the choice of the reconstruction and image rejection filters. Filtering in the transmitter chain, unlike the receiver, lacks an explicitly defined selectivity utility in this analysis. This utility would be necessary to include if the model were targeting a specific regulatory framework for compliance of power radiated in adjacent communication channels. Given the high sensitivity of the performance to the ADC architectural decision, the tradespace in Fig. 10 was plotted again in Fig. 13 with the ADC options highlighted individually. As can be observed, the inclusion of a flash ADC option consistently leads to a lower overall performance of the generated system architectures. In contrast, architectures including the pipelined and time-interleaved ADC options maximize the system's multi-attribute utility and lead to the formation of the Pareto-frontier. This result can be tied back to the low bit-depth of the flash ADCs, which results in high quantization noise and low sensitivity, albeit at a very high sampling rate. Importantly, this analysis indicated that the ADC architectural decision, together with the choice of topology, is the primary ddriverfor tradespace clustering.

VI. Modeling Multi-Channel SDR Systems

Modern SDR systems are commonly used in coherent multi-antenna MIMO and beamforming applications to improve coverage, capacity, and interference management [58], [59]. This section expands upon the single-channel SDR analysis to systems with multiple, coherent TRX channels, describes the changes in single-attribute utilities that are impacted by the addition of additional channels, and explores the tradespace of multi-channel architectures. For this analysis, a single-user, single-layer (rank 1) beamforming application is selected, as the required layer-to-port mapping and precoding strongly impact the utilities outlined in Section IV.

A. Multi-Channel Model Assumptions and Constants

1) Phase Coherence

One of the most critical elements in a multi-channel SDR system in a beamforming application is the phase coherence

between individual TRX channels. In this model, all channels are assumed to be fully phase coherent. This is modeled as a single fanned-out reference clock. In IF and BB sampling architectures, a single distributed phase-locked local oscillator drives the system components, thus minimizing phase coherence errors.

Full system calibration is assumed to remove systematic phase offsets, including signal-routing errors due to differences in transmission-line length and dispersion between channels. In addition, all data-converter interfaces are assumed to support calibration. For example, with JESD204B/C, appropriate use of SYSREF can establish deterministic latency, enabling inter-channel alignment to be corrected in the digital back end, although no specific architectural decision for the converter interfaces is imposed.

The remaining phase and timing errors are modeled as independent, zero-mean Gaussian processes. The system model assumes uncorrelated 90 fs clock jitter, t_{UCJ}, and a residual 10 ps RMS inter-channel timing mismatch between the data converters and programmable logic, denoted Δt. Both t_{UCJ} and Δt are chosen as representative, practically achievable values with modern jitter-cleaner chips [60], [61], ensuring PCB trace length-matching, interface timing deskew, synchronization, and absolute timing calibration. In the model, these timing parameters are used to compute the impact of residual errors on the expected improvement in system sensitivity and EVM.

2) Device Scaling

To enable appropriate per-channel scaling of FPGA, MPSoC, and RFSoC resources, and accurately evaluate device package area and power consumption utilities, as well as system bill of materials cost, a DSP slice-centric device scaling rule is used. This scaling rule is informed by published FPGA implementations of OFDM transceivers, using reported DSP-slice utilization [62], [63], and assumes 700 usable DSP slices per SDR channel. Assuming 70% effective DSP utilization due to placement, routing congestion, and resource fragmentation, this corresponds to 1000 nominal DSP slices per channel. Therefore, 4- and 8-channel SDR systems are assumed to require 4000 and 8000 nominal DSP slices, respectively. This rule also implicitly assumes that the processing system is not limiting the performance of the SDR system. While the exact need for DSP slices and logic elements in programmable logic chips is difficult to estimate without knowing the exact implementation of all SDR functional blocks, 700 usable DSP slices is a reasonable assumption for a moderate SDR workload and serves well as a first-order device sizing rule. The device feasibility can also be constrained by a multitude of secondary emergent system-level constraints like memory and I/O bandwidth requirements, timing closure, and others that are not included in this system model.

3) Beamforming

Given that the selected multi-channel SDR use case is beamforming, the model enforces a fixed main-lobe effective isotropic radiated power (EIRP) target equal to the single-channel case. Although the antenna sub-system is outside of the modeled SDR system boundary, keeping EIRP fixed allows a consistent basis for scaling the required PA output power in each TRX chain, which impacts both the system power consumption and the EVM utilities. The system channels are modeled as exact replicas of each other, i.e. a single-channel architecture is defined and then replicated exactly for other channels, without mixing the architectures or specific forms of each architectural decision. This enforces equal per-channel gain, matching the equal-amplitude excitation assumption used for coherent beamforming.

VII. Multi-Channel Evaluation Metrics

A. Receiver Sensitivity in multi-channel SDR

A significant advantage of employing a multichannel SDR system for beamforming is its ability to improve the receiver sensitivity when coherently combining the same signal across all channels. This can be achieved by using maximal-ratio combining, in which each receiver channel is weighted proportionally to its complex channel estimate before summation [64]. In an ideal case, the sensitivity gain will be proportional to the number of system channels (N_{ch})

$$\Delta\text{Sens.} = 10\log_{10}(N_{ch})\ . \tag{24}$$

One of the practical challenges in realizing the expected multi-channel sensitivity gain is achieving and maintaining phase coherence across all channels. While the SDR model is assumed to use a single, fanned-out system reference clock, a single, shared, phase-locked LO source distributed among all SDR channels, as well as phase calibration to remove static inter-channel offsets, the residual phase errors arising from the FPGA and data converter interface alignment errors, timing skew, residual differential phase noise, and channel-estimation errors due to AWGN, will still impact the signal combining efficiency, and thus the sensitivity improvement. Therefore, in this system model, the sensitivity improvement is modeled using [65] as

$$\Delta\text{Sens.} = 10\log_{10}(\eta N_{ch})\ , \tag{25}$$

where η is the coherence factor defined as

$$\eta = \frac{1-e^{-\sigma_\phi^2}}{N_{ch}} + e^{-\sigma_\phi^2}\ , \tag{26}$$

and σ_ϕ^2 is the variance of the inter-channel normally distributed residual phase errors in rad^2 associated with clocking, LO distribution, signal routing, etc. The root-mean-square phase errors are modeled as

$$\sigma_\phi = \pi f_s \sqrt{\Delta t^2 + t_{\mathrm{UCJ}}^2} \tag{27}$$

where f_s is the maximum converter sampling frequency (worst case scenario), and Δt and t_{UCJ} are defined in the model assumptions section.

B. Error Vector Magnitude

Similar to the receiver sensitivity utility, multiple channels can also improve the effective in-beam transmitter EVM if the impairment terms, like phase-noise and jitter contributions, AWGN, and DAC noise, are uncorrelated across channels. The expected EVM improvement then is

$$\Delta EVM = -10\log_{10}(1 - e^{-\sigma_\phi^2} + N_{ch}e^{-\sigma_\phi^2}) \,, \tag{28}$$

where σ_ϕ is defined in (27) and the system EVM resulting from AWGN and phase noise in dB can be computed as

$$EVM_{N/PN,\mathrm{dB}} = 10\log_{10}\big(EVM^2_{PN_{Corr.}} + \big(EVM^2_N + EVM^2_{PN_{Uncorr.}}\big)10^{\Delta EVM/10}\big) \,, \tag{29}$$

where $EVM^2_{PN_{Corr.}}$ and $EVM^2_{PN_{Uncorr.}}$ are the correlated and uncorrelated phase-noise-related EVM mean-square contributions, respectively. The correlated and uncorrelated phase noise between the SDR channels is partitioned as

$$\mathcal{L}_{Total} = \alpha\mathcal{L}_{Corr.} + (1-\alpha)\mathcal{L}_{Uncorr.} \,. \tag{30}$$

It is assumed that 90% of the overall phase noise will be correlated (represented by α) due to the common fanned out reference clock and local oscillator signals, and thus is not subject to improvement due to additional channels, while the remaining $1-\alpha$ portion is subject to improvement.

Furthermore, for a fixed total effective isotropic radiated power (EIRP), the increase in the number of coherent system channels (N_{ch}), in an ideal case, will reduce the output power requirement of individual transmitter PAs $\propto 1/N^2$ [66], assuming that each SDR TRX channel drives a dedicated antenna element through its own PA. The PA output power reduction is computed as

$$P_{\mathrm{out_{Nth\ PA}}} = P_{\mathrm{out,ref}} - 20\log_{10}(N_{ch}) - 10\log_{10}(\eta) \,, \tag{31}$$

where $P_{\mathrm{out,ref}}$ is the required PA output power in a single-channel SDR system. This reduced output power requirement will allow the system to operate in a more linear P_{in}–P_{out} region of the power amplifiers, thus reducing the non-linearity contribution to EVM, as defined in (15).

C. Power Consumption

The power consumption of each transceiver channel in the system scales linearly with the number of channels, as they are exact replicas of each other. However, appropriate scaling needs to be applied to the shared system components, i.e. the local oscillators and programmable logic with a processing system.

In IF and baseband sampling system topologies, the local oscillator is assumed to be driven from a single source and distributed among the channels to ensure phase coherence. The LO fanout, however, reduces the LO power available for each mixer in the system. Therefore, for each specific form of AD6, the LO output power, and thus the DC power consumption, scales with the number of system channels and mixers per channel as

$$P_{\mathrm{DC_{LO}}} = P_{\mathrm{DC_{LO,base}}} + P_{\mathrm{LO_{ref}}}N_{\mathrm{mixers}}, \tag{32}$$

where $P_{\mathrm{DC_{LO,base}}}$ is the DC power required to bias and enable the oscillator, $P_{\mathrm{LO_{ref}}}$ is the required LO output drive power per mixer in W, and N_{mixers} is the number of mixers in the system. In this model, the local oscillator and its distribution network are assumed to be ideal, with a unity conversion slope between the incremental LO output power and incremental LO DC power.

The power consumption ($P_{DC_{\mathrm{digital}}}$) of the digital system blocks including the programmable logic and processing system can be estimated as

$$P_{DC_{\mathrm{digital}}} = P_{\mathrm{base}} + N_{ch}\Big(P_{\mathrm{c2c}}(L,r) + P_{\mathrm{DSP}}(N_{\mathrm{DSP}},f) + P_{\mathrm{fabric}}(W,f)\Big) \tag{33}$$

where P_{base} is the baseline power consumption of the programmable logic and, for MPSoC or RFSoC, processing system components including clocking infrastructure and other always-on resources, P_{c2c} is the power consumption of a per-channel high-speed chip-to-chip interface, L is the number of interface lanes (could be N LVDS pairs or JESD lanes), r is the interface data rate, P_{DSP} is the power consumed by the DSP slices, N_{DSP} is the number of DSP slices used, f is PL operating frequency, P_{fabric} is the power consumed by the PL fabric, and W is the aggregate internal datapath width processed in the PL blocks. To parameterise the incremental per-channel power consumption scaling for the $P_{DC_{\mathrm{digital}}}$, the AMD Power Design Manager (PDM) [67] was used assuming a 250 MHz PL clock, 700 effective DSP slices per channel and 70% effective utilization of available on-chip resources due to routing and timing closure constraints.

The per-PA output power requirement drops as outlined in (31). Therefore, the total PA DC power consumption across all channels decreases $\propto 1/N_{ch}$, with the PA efficiency in backoff approximated by a linear function of backed-off PA output power,

$$\eta_{\mathrm{PA}}(P_{\mathrm{out}}) = a\,P_{\mathrm{out}} + b \,. \tag{34}$$

The backed-off PA DC power is then computed from (20) using the delivered RF power in back-off and the backed-off efficiency ($\eta_{\mathrm{PA_{BO}}}$) as

$$P_{\mathrm{DC_{Nth\ PA}}} = \frac{P_{\mathrm{BO_{out}}} - P_{\mathrm{BO_{in}}}}{\eta_{\mathrm{PA_{BO}}}} \,, \tag{35}$$

and the total PA DC power across all channels is computed as

$$P_{\mathrm{DC}} = N_{ch}\,P_{\mathrm{DC_{Nth\ PA}}}. \tag{36}$$

D. Area

The physical area occupied by all non-shared specific form options of each architectural decision in the system increases linearly with the number of components. The system is assumed to only have a single local oscillator source, so its area is only considered once. To estimate the package area of FPGA, MPSoC, and RFSoC devices as a function of channel count, a DSP-slice-based scaling rule is used.

Each channel is assumed to require 700 effective DSP slices. Furthermore, only 70% of the total device DSP resources are assumed to be usable due to placement, routing, and fragmentation limitations. The resulting package channel capacity is computed as

$$C_{\text{pkg}} = \left\lfloor \frac{0.7 \cdot \text{DSP}}{700} \right\rfloor . \tag{37}$$

Using the total number of DSP slices listed for commercially available Altera and Xilinx FPGA, MPSoC, and RFSoC devices, the C_{pkg} was mapped to the published chip package area for each architectural decision option to establish an area-to-capacity relationship, which was then used to compute the area utility.

E. Cost

The same first-order, DSP-centric resource scaling approach is used to map the commercially available FPGA, MPSoC, and RFSoC device cost as a function of effective DSP resources, yielding a cost-sizing rule used in the system model. However, for RFSoC-based SDRs, an additional constraint is the number of available integrated data converters, as the baseband system configuration requires two ADCs and two DACs per SDR channel for individual sampling of I and Q data streams. Also, similar to the area utility, the LO cost is only considered once.

F. Throughput Estimation in Multi-Channel SDR

Often, interfaces between system components, memory bandwidth, programmable-logic fabric throughput, and compute overheads limit the total data throughput of the system. To model this potential system limitation, a throughput utility for multi-channel SDR systems is defined as

$$TPU = \min(\max\left(\frac{TP_{\text{cap}}}{TP_{\text{payload}}} - 1, 0\right), 1) , \tag{38}$$

where TP_{payload} is the required payload throughput defined as

$$TP_{\text{payload}} = 2B(1+\beta)(N_{\text{bd}} + N_{\text{pad}})N_{ch} \tag{39}$$

where B is the signal bandwidth, N_{bd} is the nominal converter bit depth, N_{pad} is the number of padding bits to achieve the desired internal datapath width, and β is the oversampling factor. The system throughput capacity TP_{cap} could be modeled using a reduced-order, Gables-like roofline model [68], as

$$TP_{\text{cap}} = \min\left(\frac{R_{\text{CI}}}{\alpha_{\text{CI}}}, \frac{R_{\text{Fabric}}}{\alpha_{\text{Fabric}}}, \frac{R_{\text{Mem}}}{\alpha_{\text{Mem}}}, \frac{C_{\text{Ops}}}{k_{\text{Ops/bit}}}\right) \tag{40}$$

where R_{CI}, R_{Fabric}, and R_{Mem} are the raw data converter interface rates, programmable logic fabric streaming bandwidth, and raw off-chip external memory bandwidth limit, respectively. The computation limit is expressed by taking the ratio of total system compute capacity in operations per second (C_{Ops}) and dividing it by the number of algorithmic operations required per input bit $k_{\text{Ops/bit}}$. The α terms in (40) represent the overhead factors, all ≥ 1. E.g. α_{CI} represents the converter interface overhead factor associated with data encoding, forward error correction, and framing.

Therefore *TPU* could be used to filter out the throughput-infeasible architectures with $TP_{\text{cap}} \leq TP_{\text{payload}}$ and grade relative performance of all remaining valid architectures through the system MAU. However, all terms in (40) represent emergent system properties that depend on the exact SDR software architecture and implementation of corresponding DSP and data processing algorithms in the programmable logic and the processing system. Similarly, depending on the software architecture, memory bandwidth can become a significant bottleneck if a significant amount of data is written to and read from the external memory components. Without a specific software architecture, R_{Fabric}, R_{Mem}, and the overhead factors α cannot be credibly parameterized across the tradespace. Therefore, as the software architecture is outside of the modeled system boundary, the SDR TRX system model reported in this paper does not implement the *TPU*-based filter, and assumes that all generated TRX architectures are valid.

VIII. Multi-Channel SDR Tradespace Analysis

With the SAU modifications outlined above, two new tradespaces were generated representing 4- and 8-channel SDR architectures, as shown in Fig. 14. The analysis shows that for multi-channel SDRs, the base architectures identified in the generated tradespaces have changed from direct RF sampling, as in a single-channel case, to IF sampling topologies. Additionally, the Pareto frontier in both 4- and 8-channel cases includes RFSoC-based SDR architectures, whereas, for the single-channel case, the Pareto-optimal set of good architectures did not contain RFSoC. More interestingly, the multi-channel RFSoC-based architectures also yield the highest system utility. This utility increase is attributed to an aggressive on-chip integration of programmable logic, processing system as well as data converters, which yields considerable gains in overall system power consumption and occupied component area. While this utility gain is observable in both 4- and 8-channel SDR architectural tradespaces, it is most pronounced in the 8-channel tradespace.

The significant cost disparity observed between single-channel RFSoC- and non-RFSoC-based architectures, which bifurcated the single-channel tradespace in two large clusters in Fig. 10, is not present in the tradespaces of the multi-channel systems. Further, the cost premium for RFSoC-based systems decreases (as a fraction of the total system cost) as the number of SDR channels increases. All three clusters representing discrete FPGA and MCU, MPSoC, and RFSoC architectural decision options overlap in the multi-channel SDR system tradespaces with varying degrees of overall system utility. The most cost-efficient system architectures remain the ones using discrete FPGA and MCU options for AD1 and AD2, with MPSoC-based SDR architectures showing comparable, albeit slightly higher BOM cost. The

most cost-inefficient system architectures appear to be driven not by specific form options of AD1 and AD2, but rather by the flash ADC option of AD13 coupled with the baseband sampling system topology. Since baseband sampling requires independent sampling of the I and Q waveforms, the high cost of a flash ADC option considerably affects the overall system cost and leads to clustering.

To see whether the relative importance of system architectural decisions differs from the single-channel case, the main-effect-based sensitivity analysis was performed on an 8-channel system tradespace.

The overall architectural decision hierarchy appears to be stable between single- and multi-channel systems, with the ADC, LO, and preselect filter decisions being the most sensitive. In the SDR RX chain, the mean MAU sensitivity is dominated by the ADC, whose sensitivity increases by 15.9%, while preselect-filter sensitivity decreases by 16.4%. In the transmitter chain, the 8-channel system becomes less sensitive to the PA architectural decision, with sensitivity

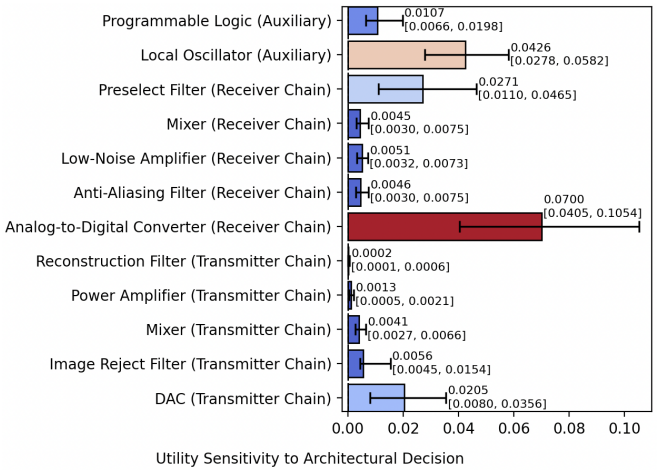
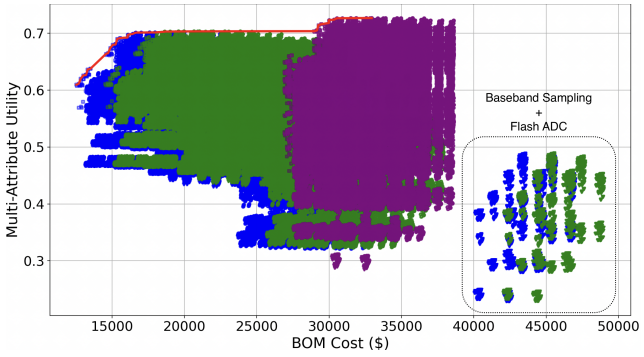
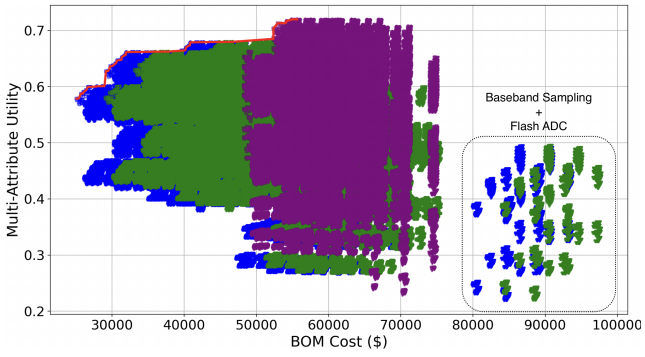


FIGURE 15. Prioritized architectural decisions for an 8-channel SDR system from main effects sensitivity analysis. The error bars show the range of the main-effect results across the full factorial combination of utility weights when each weight was perturbed by ±1 from their nominal values considered in Table 5.



(a)



(b)

FIGURE 14. The architectural tradespaces showing 2,024,640 different SDR architectures across three different topologies: baseband sampling, IF sampling, and direct RF sampling, in (a) 4-channel configuration, and (b) 8-channel configuration.

dropping by 86%, which is expected given the beamforming-related model assumptions, which allow the PAs to be driven in backoff, resulting in power consumption and linearity improvements. Interestingly, the sensitivity to the DAC architectural decision increased by 36.7%, making it comparable in importance to the preselect filter. This is largely attributable to the drop in sensitivity to the PA architectural decision, as the PA stops being the dominant component, which makes the system more sensitive to other components in the TX chain. Similarly, the sensitivity to the TX image-reject filter becomes non-negligible in the multi-channel case. Lastly, the mean sensitivity to the common system components, such as the local oscillator and programmable logic, has also increased by 23.8% and 8.1%, respectively.

To assess the sensitivity of the decision ranking to the utility weights shown in Table 5, each weight was perturbed by ±1 (a 20% to 100% change). A full factorial weight analysis resulted in 52,488 unique tradespaces, with the main effect of each decision recorded each time. This sensitivity is shown in Fig. 15, identifying the nominal sensitivity value in the text label, and the minimum and maximum values as error bars. The range of the weight-perturbed main-effect analysis results reveals some interesting observations. The top 3 nominal main-effect analysis ADs (ADCs, LOs, and preselect filters) also show the strongest sensitivity to the utility weights. The ADC remains one of the critical ADs to focus on when designing a 6G-capable SDR. Additionally, programmable logic and DAC ADs might become more prominent under modified utility weights. Conversely, the remaining considered TRX chain components show low sensitivity to the choice of weights. This analysis highlights that even with utility weight perturbations, the system is most sensitive to the ADC, local oscillator, and preselect filter ADs, with the DAC AD following closely for an 8-channel architectural tradespace. Overall, the multi-channel

results indicate a stronger relative emphasis on architectural decisions that affect system-level performance in aggregate, while the influence of some per-channel TX decisions, most notably the PA, decreases.

IX. Model Limitations

The SDR TRX architectures analyzed in this work target the 6G mid-band frequency range specified in Table 2, and do not cover the entire FR3 (7.125–24.25 GHz) band. For direct RF sampling architectures, the primary limiting factor is the limited availability of high-sampling-rate, clock jitter-tolerant data converters that offer a sufficient effective number of bits and, as a result, signal-to-noise ratio at the desired frequency range and signal bandwidth. New products are starting to appear on the market, offering sampling rates up to 64 GSps for both ADCs and DACs, albeit at a low nominal bit depth of 8–10 bits, considerably affecting the system sensitivity and dynamic range [69], [70].

Future work should examine the full FR3 frequency band. This could be accomplished by integrating a core SDR system as a back end with a fully frequency-agile frequency translation front end. This would allow the extension of the SDR frequency range well into the FR3 band and above. While architecting a frequency translation front end, particular emphasis should be placed on the harmonic and non-harmonic spurs, which can create in-band and out-of-band (OOB) interferers, thus degrading EVM and signal-to-interference-and-noise ratio (SINR). Out-of-band harmonic spurious tones can violate spectral masks and the permitted OOB emission limits. Additionally, LO leakage may result in carrier feed-through, LO-related spurious, and potential DC offsets via self-mixing. Importantly, there will be additional requirements imposed on the programmable logic, which must handle system calibration and compensation for frequency translation system imperfections, such as thermal instability, soft compression, group delay and gain variations in the passband, among others. This could increase resource requirements, such as DSP slices and programmable logic blocks, and potentially make digital correction and calibration a limiting factor in the overall system architecture. While two potential frequency translation architectures are already implicitly represented by topology in this analysis, namely direct conversion/zero-IF in baseband sampling, and single conversion in IF sampling, a full coverage of the FR3 band would likely require a double- or multi-stage conversion architecture. Therefore, it is recommended to model the frequency translation front end as an entirely separate system.

Similarly, the set of modeled SDR TRX utilities defined in this work is by no means comprehensive and could be expanded to more finely model low-level TRX effects, such as sampling spurs, performance over temperature, and performance variation over frequency. For more detailed system performance evaluation, compact electrothermal or nonlinear behavioral device models could be used for each specific option in the architectural decisions. Furthermore, the current SDR TRX model only allows coupled architectures for TX and RX chains. While this reduces the combinatorial complexity, it could also eliminate plausible mixed TRX architectures with a higher multi-attribute utility value.

Finally, this model does not explicitly capture implementation risk and complexity, given that chip-to-chip interfaces, memory, and DSP implementation were outside the system boundary. These factors affect the converter interface throughput, buffering, memory bandwidth, and timing closure limitations. The MAU-driven tradespace evaluation framework presented in this paper provides a systematic method for comparing, ranking, and assessing the sensitivity of competing modern SDR transceiver architectures.

X. Conclusions

This analysis examined the impact of major design decisions in 6G-capable single- and multi-channel software-defined radio architectures spanning baseband, IF, and direct RF sampling topologies. The performance of each architecture was evaluated using a weighted composite of utility functions forming a multi-attribute utility and visualized on a tradespace, enabling identification of the Pareto frontier and the architectures that provide the highest performance for a given BOM cost. The use of sampling topology as an organizing pattern for the wide variety of designs on the market was validated. This paper's primary contribution is an analytical method to evaluate the merits of this topology-based decomposition of the design landscape. One of the principal findings is that, for single-channel SDR systems, the knee-in-the-curve (base) architecture used the direct RF sampling topology, whereas for multi-channel systems the tradespace analysis identified the IF sampling architectures. This suggests that direct RF sampling is becoming increasingly competitive with IF sampling, particularly as data-converter capabilities continue to improve, and supports a broader shift towards highly integrated digital SDR architectures. The overall highest system utility in a single-channel case was still obtained with IF sampling architectures, albeit at a higher system cost.

The multi-channel analysis of 4- and 8-channel SDR architectures identified RFSoC-based architectures on the Pareto frontier and yielded the highest overall system utility, with this advantage becoming most pronounced in the 8-channel case. This indicates that aggressive on-chip integration becomes increasingly advantageous as channel count increases, shifting the preferred architectures away from those favored in the single-channel case. The tradespace analysis also enabled a main-effect-based prioritization of the SDR architectural decisions. The analysis highlighted that performance is most sensitive to the selection of the analog-to-digital converter, with the overall hierarchy of architectural sensitivities remaining stable between single-channel and multi-channel systems. In the multi-channel case, however, greater relative importance was placed on

shared system components, while the influence of some per-channel decisions, most notably the power amplifier in the transmitter chain, decreased. These results indicate that continued advances in data-converter technology are likely to remain a key enabler for improved 6G-capable SDR performance, while increasing channel count further strengthens the architectural advantages of highly integrated RFSoC-based SDR implementations.

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