CURRICULUM VITA
VIJAYKRISHNAN NARAYANAN

Education:

1998 Ph.D., Department of Computer Science and Engineering, University of South Florida, Tampa
1993 B.E., Department of Computer Science and Engineering, SVCE, University of Madras, India (First Rank in University of Madras)

Experience:

2023- Associate Dean of Innovation, College of Engineering, The Pennsylvania State University
2021- Director, Center for Artificial Intelligence Foundations and Engineered Systems. The Pennsylvania State University
2020- Interim Director of Limited Submission, Office of Senior Vice President of Research, The Pennsylvania State University
2018- Robert Noll Chair Professor, Computer Science and Engineering and Electrical Engineering, Penn State
2015-2018 Distinguished Professor, Computer Science and Engineering and Electrical Engineering, Penn State
2007-2014 Professor, Computer Science and Engineering and Electrical Engineering, Penn State
2003-2007 Associate Professor, Computer Science and Engineering, Penn State
1998-2003 Assistant Professor of Computer Science and Engineering, Penn State
1993-1998 Graduate Assistant, University of South Florida

Honors and Awards:

2024 AAAS Fellow, elected for contributions to the field of computer architecture and design automation, particularly for power-aware systems and emerging technologies
2023 Commendation in Joint Press Release by United States and India released by the White House for the India-U.S. Defense Acceleration Ecosystem (INDUS-X) team. Narayanan serves as the lead U.S. coordinator for Academic Collaborations for Defense Startups.
2023 Editors Pick Paper, Biomedical Optics Express Journal.
2022 Micro Hall of Fame, ACM/IEEE International Symposium on Microarchitecture
2022 ACM SIGDA Distinguished Service Award
2021 IEEE Computer Society TCVLSI Distinguished Research Award
2021 Best paper award in the architecture track, IEEE NAS 2021.
2021 Best paper nomination, Design and Test in Europe Conference.
2021 Fellow, National Academy of Inventors
2021 IEEE Computer Society Edward J. McCluskey Technical Achievement Award
2020 Northeastern Association of Graduate Schools Geoffrey Marshall Mentoring Award
2020 Best paper nomination, Design and Test in Europe Conference
2019 Nanoarch Best Student Paper
2018 IEEE CEDA Distinguished Speaker
2018 IEEE CEDA Oustanding Service Award
2017 IEEE Transactions on Multi-Scale Computing Systems Best Paper Award.
2017 Invited Lecturer, Global Initiative of Academic Network, Ministry of Human Resource Development, Government of India.

2017	IEEE/ACM ASPDAC Best Paper Award
2016	Invited demonstration (only one selected nationally by Computing Research Association) at The 22nd Annual Coalition for National Science Funding (CNSF) Exhibition & Reception on Capitol Hill
2016	Invited Technology Speaker, China (Beijing) International Technology Transfer Convention 2016 hosted by China Ministry of Science and Technology and Beijing Municipal People's Government
2016	Big Ten Network Television Network coverage on "Visual Cortex on Silicon" Project
2016	IEEE Micro's Top Picks.
2015	Most significant paper award for influencing theory and practice in the area of Field Programmable Logic and Applications among those published over the last 25 years
2015	ACM Fellow, elected for contributions to Power-Aware Design
2015	Invited Panelist at US Senate and House Caucus Briefing
2015	IEEE HPCA Best Paper Award
2014	Best paper nomination DAC Designer Track
2014	Invited Participant at US White House Brain Conference
2014	Association of Computing Machinery Fellow, elected for contributions to Power-Aware Design
2014	Featured on cover story of NSF news for work on computing using oscillators.
2012	Penn State Engineering Alumni Society (PSES) Premier Research Award
2012	ASPDAC 10-year Retrospective Most Influential Paper Award
2012	Best paper nomination, CODES/ISSS 2012
2011	IEEE Fellow, elected for contributions to Power-Aware Design
2010	Certificate of Appreciation for promoting excellence in scientific research, National Security Agency/University of Maryland Laboratory of Physical Sciences.
2010	Outstanding Alumni Award**,** Sri Venkateswara College of Engineering, India
2009	The NSF CRI Project (PI: Narayanan) on soft errors was featured as a selected investment by National Science Foundation and described as "One of a Kind Test Facility to Reduce Chip Errors," page 39. http://www.nsf.gov/news/nsf09013/nsf_09013_selected.pdf).
2009	NSF HoDoo Project (PI: Narayanan) was selected by NSF Computing and Communications Foundations program cluster as one of the featured projects on the NSF Web site.
2006	PSES Outstanding Research Award
2006	Best paper nomination ISQED Conference
2006	ICA DSN Best Paper Award
2003	Best paper nomination DATE Conference
2002	Penn State CSE Outstanding Faculty Teaching Award
2002	IEEE Circuits and Systems Society VLSI Transactions Best Paper Award
2001	NSF CAREER Award
2000	The ACM SIGDA Outstanding New Faculty Award

Research Contributions Summary

Narayanan's research has focused on computer architecture (power-aware systems, application specific systems, on-chip networks, design using emerging technologies and reliable design) and design automation (design tools, models and automation frameworks). He has published more than 500 papers, with an H-index of 86 and 28324 citations (December 2023). His work has gained recognition in multiple research communities spanning design automation, computer architecture, FPGA, VLSI circuits and devices through best paper awards/nominations, most influential papers, invited keynotes and panel discussions. He has served as an investigator on research grants administered by U.S. Federal agencies (including the National Science Foundation, DARPA, Dept. of Energy, Army, Office of Naval Research, NSA), Semiconductor Research Corporation, and industry. He serves as an associate director for a DoE center on 3D electronics, and a thrust leader for the DARPA/SRC JUMP 2.0 Center for the Center for Processing with Intelligent Storage and

Memory. He served as a thrust leader for DARPA/SRC JUMP Center for Brain-Inspired Computing and STARNET Center for Low Energy Systems Technology. His work has been featured in Big Ten Television Network, and in technical media. He has presented more than 200 invited/keynote talks to audiences around the world, has mentored 10 Postdocs, 54 Ph.D. students, 72 masters' students, 15 undergrad honors theses, and involved K-12 teachers and students in research experience projects. He has been actively engaging under-represented students in research through the summer research opportunities program for many years. He has offered in-depth technical tutorials at many conferences and demos from his group have been featured in science exhibits for K-12 students and the public. He has been involved with technology transition projects with the Navy, Intel Corporation, Videomining and Siliconscapes. Many of his former students are recognized leaders in industry (such as Intel, TSMC, Qualcomm, IBM, Oracle), founders of tech companies (md Portal, DigiComCore, SiliconScapes) and tenured faculty in premier academic institutions (such as IIT Madras, India; KAIST, Korea; Univ. of Cyprus; NCKU, Taiwan;). His research has resulted in the design of new VLSI/FPGA CAD tools and optimizations for power and reliability, the creation of new experimental platforms and system architectures.

Articles published in refereed journals (142).

1. A Kumar, S Abrams, A Kumar, V Narayanan, STAR: Efficient SpatioTemporal Modeling for Action Recognition. Circuits, Systems, and Signal Processing 42 (2), 705-723. 2023.
2. Z Li, B Li, K. W Eliceiri, V. Narayanan. Computationally efficient adaptive decompression for whole slide image processing. Biomedical Optics Express 14 (2), 667-686 2023.
3. A Mallick, Z Zhao, MK Bashar, S Alam, MM Islam, Y Xiao, Y Xu, A Aziz, V. Narayanan. CMOS-compatible Ising machines built using bistable latches coupled through ferroelectric transistor arrays. Scientific reports 13 (1), 2023.
4. I Okafor, AK Ramanathan, NR Challapalle, Z Li, V Narayanan. Fusing In-Storage and Near-Storage Acceleration of Convolutional Neural Networks. ACM Journal on Emerging Technologies in Computing Systems 2023.
5. A Hanchate, P S Dave, A Tiwari, D Sagapuram, A Verma, SRT Kumara, et. al. A Graphical Representation of Sensor Mapping for Machine Tool Fault Monitoring and Prognostics for Smart Manufacturing. Smart and Sustainable Manufacturing Systems 7 (1), 82-110. 2023.
6. Wenjun Tang, Mingyen Lee, Juejian Wu, Yixin Xu, Yao Yu, Yongpan Liu, Kai Ni, Yu Wang, Huazhong Yang, Vijaykrishnan Narayanan, Xueqing Li. FeFET-Based Logic-in-Memory Supporting SA-Free Write-Back and Fully Dynamic Access With Reduced Bitline Charging Activity and Recycled Bitline Charge. IEEE Trans. Circuits and Systems. I. 70(6): 2398-2411 (2023)
7. Yiming Chen, Yushen Fu, Mingyen Lee, Sumitha George, Yongpan Liu, Vijaykrishnan Narayanan, Huazhong Yang, Xueqing Li. FAST: A Fully-Concurrent Access SRAM Topology for High Row-Wise Parallelism Applications Based on Dynamic Shift Operations. IEEE Trans. Circuits Syst. II Express Briefs 70(4): 1605-1609 (2023) Yu, T., Xu, Y., Deng, S., Zhao, Z., Jao, N., Kim, Y. S., Duenkel, S., Beyer, S., Ni, K., George, S., & Narayanan, V. (2022). Hardware functional obfuscation with ferroelectric active interconnects. Nature Communications, 13(1). DOI: 10.1038/s41467-022-29795-3

8. Jiang, Z., Zhao, Z., Deng, S., Xiao, Y., Xu, Y., Mulaosmanovic, H., Duenkel, S., Beyer, S., Meninger, S., Mohamed, M., Joshi, R., Gong, X., Kurinec, S., Narayanan, V., & Ni, K. (2022). On the Feasibility of 1T Ferroelectric FET Memory Array. IEEE Transactions on Electron Devices, 69(12), 6722-6730. DOI: 10.1109/TED.2022.3216819, ISBN/ISSN: 00189383
9. Ma, X., Zhong, H., Xiu, N., Chen, Y., Yin, G., Narayanan, V. , Liu, Y., Ni, K., Yang, H., & Li, X. (2022). CapCAM: A Multilevel Capacitive Content Addressable Memory for High-Accuracy and High-Scalability Search and Compute Applications. IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 30(11), 1770-1782. DOI: 10.1109/TVLSI.2022.3198492, ISBN/ISSN: 10638210
10. Lu, H., He, T., Wang, S., Liu, C., Mahdavi, M., Narayanan, V. , Chan, K. S., & Pasteris, S. (2022). Communication-Efficient k-Means for Edge-Based Machine Learning. IEEE Transactions on Parallel and Distributed Systems, 33(10), 2509-2523. DOI: 10.1109/TPDS.2022.3144595, ISBN/ISSN: 10459219
11. Lee, S., Aldas, N. D., Lee, C., Rosson, M. B., Carroll, J. M., & Narayanan, V. (2022). AIGuide: Augmented Reality Hand Guidance in a Visual Prosthetic. ACM Transactions on Accessible Computing, 15(2). DOI: 10.1145/3508501, ISBN/ISSN: 19367228
12. Shen, T., Mishra, C. S., Sampson, J., Kandemir, M. T., & Narayanan, V. (2022). An Efficient Edge-Cloud Partitioning of Random Forests for Distributed Sensor Networks. IEEE Embedded Systems Letters. DOI: 10.1109/LES.2022.3207968, ISBN/ISSN: 19430663
13. Chen, Y., Fu, Y., Lee, M., George, S., Liu, Y., Narayanan, V. , Yang, H., & Li, X. (2022). FAST: A Fully-Concurrent Access SRAM Topology for High Row-wise Parallelism Applications Based on Dynamic Shift Operations. IEEE Transactions on Circuits and Systems II: Express Briefs. DOI: 10.1109/TCSII.2022.3231589, ISBN/ISSN: 15497747
14. N. Jao, A. K. Ramanathan, J. Sampson and V. Narayanan, "Sparse Vector-Matrix Multiplication Acceleration in Diode-Selected Crossbars," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 29, no. 12, pp. 2186-2196, Dec. 2021, doi: 10.1109/TVLSI.2021.3114186.
15. Hongtao Zhong, Shengjie Cao, Li Jiang, Xia An, Vijaykrishnan Narayanan, Yongpan Liu, Huazhong Yang, Xueqing Li, "DyTAN: Dynamic Ternary Content Addressable Memory Using Nanoelectromechanical Relays," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 29, no. 11, pp. 1981-1993, Nov. 2021, doi: 10.1109/TVLSI.2021.3115622.
16. Keni Qiu, Nicholas Jao, Kunyu Zhou, Yongpan Liu, Jack Sampson, Mahmut Taylan Kandemir, Vijaykrishnan Narayanan. MaxTracker: Continuously Tracking the Maximum Computation Progress for Energy Harvesting ReRAM-based CNN Accelerators. ACM Trans. Embed. Comput. Syst. 20(5s): 78:1-78:23. (2021).
17. Skyler Anderson, Nagadastagiri Challapalle, John Sampson, Vijaykrishnan Narayanan. Adaptive Neural Network Architectures for Power Aware Inference. IEEE Design and Test 37(2): 66-75 (2020)
18. Hanlin Lu, Ming-Ju Li, Ting He, Shiqiang Wang, Vijaykrishnan Narayanan, Kevin S. Chan. Robust Coreset Construction for Distributed Machine Learning. IEEE J. Sel. Areas Commun. 38(10): 2400-2417 (2020)

19. S. R. Swamy Saranam Chongala, Sumitha George, Hariram Thirucherai Govindarajan, Jagadish Kotra, Madhu Mutyam, John Sampson, Mahmut T. Kandemir, Vijaykrishnan Narayanan. Optimization of Intercache Traffic Entanglement in Tagless Caches With Tiling Opportunities. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 39(11): 3881-3892 (2020)
20. Hongtao Zhong, Mingyang Gu, Yu Wang, Yongpan Liu, Vijaykrishnan Narayanan, Huazhong Yang, Xueqing Li. One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. IEEE Trans. Circuits Syst. 67-II (12): 3402-3406 (2020)
21. Nagadastagiri Challapalle, Sahithi Rampalli, Nicholas Jao, Akshay Krishna Ramanathan, John Sampson, Vijaykrishnan Narayanan. FARM: A Flexible Accelerator for Recurrent and Memory Augmented Neural Networks. J. Signal Process. Syst. 92(11): 1247-1261 (2020
22. Z Shen, S Srinivasa, A Aziz, S Datta, V Narayanan, SK Gupta. SRAMs and DRAMs With Separate Read–Write Ports Augmented by Phase Transition Materials. IEEE Transactions on Electron Devices 66 (2), 929-937 (2019)
23. Xueqing Li, Juejian Wu, Kai Ni, Sumitha George, Kaisheng Ma, John Sampson, Sumeet Kumar Gupta, Yongpan Liu, Huazhong Yang, Suman Datta, Vijaykrishnan Narayanan. Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. IEEE Design & Test 36(3): 39-45 (2019)
24. Arijit Raychowdhury, Abhinav Parihar, Gus Henry Smith, Vijaykrishnan Narayanan, György Csaba, Matthew Jerry, Wolfgang Porod, Suman Datta. Computing With Networks of Oscillatory Dynamical Systems. Proceedings of the IEEE 107(1): 73-89 (2019)
25. Srivatsa Rangachar Srinivasa, Akshay Krishna Ramanathan, Xueqing Li, Wei-Hao Chen, Sumeet Kumar Gupta, Meng-Fan Chang, Swaroop Ghosh, Jack Sampson, Vijaykrishnan Narayanan. ROBIN: Monolithic-3D SRAM for Enhanced Robustness with In-Memory Computation Support. IEEE Trans. on Circuits and Systems 66-I(7): 2533-2545 (2019)
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27. Xueqing Li, Sumitha George, Kaisheng Ma, Kai Ni, Ahmedullah Aziz, Sumeet Gupta, John Sampson, Meng-Fan Chang, Yongpan Liu, Huazhong Yang, Suman Datta, and Vijaykrishnan Narayanan. Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, accepted.
28. Sumitha George, Xueqing Li, Minli Julie Liao, Kaisheng Ma, Srivatsa Srinivasa, Karthik Mohan, Ahmedullah Aziz, John Sampson, Sumeet Kumar Gupta, and Vijaykrishnan Narayanan. Symmetric 2-D-Memory Access to Multidimensional Data. IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 2018, doi: 10.1109/TVLSI.2018.2801302.
29. Neel Gala, Sarada Krithivasan, Wei-Yu Tsai, Xueqing Li, Vijaykrishnan Narayanan, V. Kamakoti: An Accuracy Tunable Non-Boolean Co-Processor Using Coupled Nano-Oscillators. JETC 14(1): 1:1-1:28 (2018)

30. Srivatsa Rangachar Srinivasa, Xueqing Li, Meng-Fan Chang, John Sampson, Sumeet Kumar Gupta, Vijaykrishnan Narayanan: Compact 3-D-SRAM Memory With Concurrent Row and Column Data Access Capability Using Sequential Monolithic 3-D Integration. IEEE Trans. VLSI Syst. 26(4): 671-683 (2018)
31. Xueqing Li; John Sampson; Asif Khan; Kaisheng Ma; Sumitha George; Ahmedullah Aziz; Sumeet Kumar Gupta; Sayeef Salahuddin; Meng-Fan Chang; Suman Datta; Vijaykrishnan Narayanan. Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET. IEEE Transactions on Electron Devices 2017, 64(8): 3452 – 3458
32. Shreya Gupta; Mark Steiner; Ahmedullah Aziz; Vijaykrishnan Narayanan; Suman Datta; Sumeet Kumar Gupta. Device-Circuit Analysis of Ferroelectric FETs for Low-Power Logic. IEEE Transactions on Electron Devices. 2017, 64(8): 3092 - 3100
33. Xueqing Li; Kaisheng Ma; Sumitha George; Win-San Khwa; John Sampson; Sumeet Gupta; Yongpan Liu; Meng-Fan Chang; Suman Datta; Vijaykrishnan Narayanan. Design of Nonvolatile SRAM with Ferroelectric FETs for Energy-Efficient Backup and Restore. IEEE Transactions on Electron Devices. 2017. 64(7): 3037 – 3040
34. Xueqing Li; Sumitha George; Kaisheng Ma; Wei-Yu Tsai; Ahmedullah Aziz; John Sampson; Sumeet Kumar Gupta; Meng-Fan Chang; Yongpan Liu; Suman Datta; Vijaykrishnan Narayanan. Advancing Nonvolatile Computing With Nonvolatile NCFET Latches and Flip-Flops. IEEE Transactions on Circuits and Systems I: Regular Papers. 2017, 13 pages.
35. Peter A. Zientara, Sooyeon Lee, Gus H. Smith, Rorry Brenner, Laurent Itti, Mary Beth Rosson, John M. Carroll, Kevin M. Irick, Vijaykrishnan Narayanan. Third Eye: A Shopping Assistant for the Visually Impaired. IEEE Computer 50(2): 16-24 (2017)
36. Yun-Jui Li, Ching-Yi Huang, Chia-Cheng Wu, Yung-Chih Chen, Chun-Yao Wang, Suman Datta, Vijaykrishnan Narayanan. Dynamic Diagnosis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Trans. VLSI Syst. 25(4): 1477-1489 (2017)
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38. Tsai, W.-Y., Barch, D., Cassidy, A., Debole, M., Andreopoulos, A., Jackson, B., Flickner, M., Arthur, J., Modha, D., Sampson, J., & Narayanan, V. (2016). Always-on Speech Recognition using TrueNorth, a Reconfigurable, Neurosynaptic Processor. IEEE Transactions on Computers (99). (First Author co-supervised)
39. Ho, C.-H., Chen, Y.-C., Wang, C.-Y., Huang, C.-Y., Datta, S., & Narayanan, V. (2016). Area-Aware Decomposition for Single-Electron Transistor Arrays. ACM Transactions on Design Automation of Electronic Systems (TODAES), 21(4), 70.
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41. Srinivasa, S., Aziz, A., Shukla, N., Li, X., Sampson, J., Datta, S., Kulkarni, J. P., Narayanan, V. , & Gupta, S. (2016). Correlated Material Enhanced SRAMs With Robust Low Power Operation. IEEE Transactions on Electron Devices, 63(12), 4744–4752. (First Author co-supervised)
42. Huang, C.-Y., Li, Y.-J., Liu, C.-W., Wang, C.-Y., Chen, Y.-C., Datta, S., & Narayanan, V. (2016). Diagnosis and Synthesis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 24(6), 2321–2334.
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44. Kim, M. S., Li, X., Liu, H., Sampson, J., Datta, S., & Narayanan, V. (2016). Exploration of low-power high-SFDR current-steering D/A converter design using steep-slope heterojunction Tunnel FETs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 24(6), 2299–2309. (First author supervised)
45. Sun, Y., Yuan, Z., Liu, Y., Li, X., Wang, Y., Wei, Q., Wang, Y., Narayanan, V. , & Yang, H. (2016). Maximum Energy Efficiency Tracking Circuits for Converter-less Energy Harvesting Sensor Nodes. IEEE Transactions on Circuits and Systems II: Express Briefs. (Fourth author supervised)
46. Ma, K., Li, X., Swaminathan, K., Zheng, Y., Li, S., Liu, Y., Xie, Y., Sampson, J., & Narayanan, V. (2016). Nonvolatile Processor Architectures: Efficient, Reliable Progress with Unstable Power. IEEE Micro, 36(3), 72–83. (First Author co-supervised, second author supervised)
47. Sustersic, J., Wyble, B., Advani, S., & Narayanan, V. (2016). Towards a unified multiresolution vision model for autonomous ground robots. Robotics and Autonomous Systems, 75, 221–232. http://dx.doi.org/10.1016/j.robot.2015.09.031. (Third author supervised)
48. Kaisheng Ma, Xueqing Li, Shuangchen Li, Yongpan Liu, John (Jack) Morgan Sampson, Yuan Xie, Vijaykrishnan Narayanan: Nonvolatile Processor Architecture Exploration for Energy-Harvesting Applications. IEEE Micro 35(5): 32-40 (2015) (First Author co-supervised, second author supervised)
49. Chian-Wei Liu, Chang-En Chiang, Ching-Yi Huang, Yung-Chih Chen, Chun-Yao Wang, Suman Datta, Vijaykrishnan Narayanan: Synthesis for Width Minimization in the Single-Electron Transistor Array. IEEE Trans. VLSI Syst. 23(12): 2862-2875 (2015)
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51. Y. Cho, N. Chandramoorthy, K.M. Irick, V. Narayanan, "Accelerating Multiresolution Gabor Feature Extraction for Real Time Vision Applications," in Journal of Signal Processing Systems Volume 76, Issue 2, Aug. 2014 (First three authors supervised)
52. Moon Seok Kim, Huichu Liu, Xueqing Li, Suman Datta, Vijaykrishnan Narayanan, "A Steep-Slope Tunnel FET Based SAR Analog-to-Digital Converter," IEEE Transactions on Electron and Devices, 6 pages. (First author supervised and second author co-supervised)
53. N. Shukla, A. Parihar, E. Freeman, H. Paik, G. Stone, V. Narayanan, H. Wen, Z. Cai, V. Gopalan, R. Engel-Herbert, D. G. Schlom, A. Raychowdhury, and S. Datta "Synchronized charge oscillations in correlated electron systems", Scientific Reports 4:4964, May 14, 2014.

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219. Eachempati*, S., A. Nieuwoudt, A. Gayasen, Y. Massoud, N. Vijaykrishnan. April 2007. Assessing Carbon Nanotube Bundle Interconnect for Future FPGA Architectures. Proceedings of the Design, Automation and Test in Europe (DATE'07). pp. 307-312. Nice, France. (First author supervised)

220. Krishnan*, R., R. Ramanarayanan*, S. Srinivasan*, N. Vijaykrishnan, Y. Xie, M. J. Irwin. March 2007. Variation Impact on SER of Combinational Circuits. Proceedings of the International Society for Quality Electronic Design (ISQED 2007). pp. 911-916. San Jose, CA. (First and third author supervised and second author co-supervised by candidate)
221. Mupid*, A., M. Mutyam*, N. Vijaykrishnan, Y. Xie, M. J. Irwin. March 2007. Variation Analysis of CAM Cells. Proceedings of the Eighth International Symposium on Quality Electronic Design (ISQED 2007). pp. 333-338. San Jose, CA. (First two authors supervised by candidate)
222. Mondal, M., A. Ricketts*, S. Kirolos, T. Ragheb, G. Link, N. Vijaykrishnan, Y. Massoud. March 2007. Mitigating Thermal Effects on Clock Skew with Dynamically Adaptive Drivers. Proceedings of the International Society for Quality Electronic Design (ISQED 2007). pp. 67-72. San Jose, CA. (Second author supervised)
223. Ramakrishnan*, R S. Srinivasan*, N. Vijaykrishnan, Y. Xie. January 2007. Impact of NBTI on FPGAs. Proceedings of the International Conference on VLSI Design. pp. 717-722. Bangalore, India. (First and second authors supervised by candidate) (141 papers accepted out of 444 submissions) (32% acceptance rate)
224. Vaidyanathan, B., W. Hung, F. Wang, Y. Xie, N. Vijaykrishnan, M. J. Irwin. January 2007. Architecting Microprocessor Components in 3D Design Space. Proceedings of the Twentieth International Conference on VLSI Design. pp. 103-108. Bangalore, India. (141 papers accepted out of 444 submissions) (32% acceptance rate)
225. Nicopoulos*, C. A., D. Park, J. Kim, N. Vijaykrishnan, C. R. Das. December 2006. ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers. Proceedings of the International Symposium on Microarchitecture (MICRO 06). pp. 333-346. Orlando, FL. (First author supervised by candidate) (42 papers accepted out of 174 submissions) (24% acceptance rate)
226. Vaidyanathan, B., Y. Xie, N. Vijaykrishnan, R. Luo. December 2006. Leakage Optimized DECAP Design for FPGAs. Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2006). pp. 960-963. Singapore.
227. Sundararajan*, P. A. Gayasen*, N. Vijaykrishnan, T. Tuan. November 2006. Thermal Characterization and Optimization in Platform FPGAs. Proceedings International Conference on Computer Aided Design (ICCAD-2006). pp. 443-447. San Jose, CA. (First author supervised and second author co-supervised by candidate) (130 papers accepted out of 537 submissions) (24% acceptance rate)
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229. Chen, G, L. Xue, J. Kim*, K. Sobti, L. Deng, X. Sun, N. Pitsianis, C. Chakrabarti, M. Kandemir, N. Vijaykrishnan. September 2006. Using Geometric Tiling for Reducing Power Consumption in Structured Matrix Operations. Proceedings of the IEEE International System on Chip Conference (SOCC 2006). pp. 113-114. Austin, TX. (Third author supervised by candidate)
230. Srinivasan*, S., R. Ramadoss*, N. Vijaykrishnan. September 2006. Process Variation Aware Parallelization Strategies for MPSoCs. Proceedings of the IEEE International System on Chip Conference (SOCC 2006). pp. 179-184. Austin, TX. (First and second author supervised by candidate)
231. Park, D., C. Nicopoulos*, J. Kim, N. Vijaykrishnan, C. R. Das. September 2006. A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects. Proceedings of the First International Conference on Nano-Networks (Nano-Net 2006). CDROM proceedings. 6 pages. Lausanne, Switzerland. (Second author supervised by candidate)

232. Srinivasan*, S., M. Prasanth*, S. Karthik, Y. Xie, N. Vijaykrishnan. July 2006. FLAW: FPGA Lifetime Awareness. Proceedings of the Forty-Third Design Automation Conference (DAC 2006). pp. 630-635. San Francisco, CA. (First two authors supervised by candidate) (accepted 209 out of 865 submissions) (24% acceptance rate)
233. Park, D., C. A. Nicopoulos*, J. Kim, N. Vijaykrishnan, C. R. Das. June 2006. Exploring Fault-Tolerant Network-on-Chip Architectures. Proceedings of the International Conference on Dependable Systems and Networks – DCCS Track (DSN-2006). pp. 93-102. Philadelphia, PA. (Second author supervised by candidate) (34 papers accepted out of 187 submissions) (19% acceptance rate)
234. Li, F., C. Nicopoulos*, T. Richardson, Y. Xie, N. Vijaykrishnan, M. Kandemir. June 2006. Design and Management of 3D Chip Multiprocessors using Network-in-memory. Proceedings of the Thirty-Third Annual International Symposium on Computer Architecture (ISCA 2006). pp. 130-141. Boston, MA. (Second author supervised by candidate) (31 papers accepted out of 234 submissions) (13% acceptance rate)
235. Kim, J., C. A. Nicopoulos*, D. Park, N. Vijaykrishnan, C. R. Das. June 2006. A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Proceedings of the Thirty-Third Annual International Symposium on Computer Architecture (ISCA 2006). pp. 4-15. Boston, MA. (Second author supervised by candidate) (31 papers accepted out of 234 submissions) (13% acceptance rate)
236. Mutyam*, M., F. Li, N. Vijaykrishnan, M. Kandemir, M.J. Irwin. June 2006. Compiler Directed Thermal Management for VLIW Functional Units. Proceedings of the ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES 2006). pp. 163-172. Ottawa, Canada. (First author supervised by candidate) (21 accepted out of 83 submissions) (25% acceptance rate)
237. Gayasen*, A., N. Vijaykrishnan, M. Kandemir, A. Rahman. April 2006. Switch Box Architectures for Three-Dimensional FPGAs. Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM). 2 pages. Napa Valley, CA. (First author co-supervised by candidate)
238. Ramanarayanan*, R., Krishnan*, N. Vijaykrishnan, Y. Xie, M. J. Irwin. April 2006. Temperature and Voltage Scaling Effects on Electrical Masking. Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE 2006). 4 pages. Urbana, IL. (First author co-supervised and second author supervised by candidate)
239. Vaidyanathan, B., Y. Xie, N. Vijaykrishnan, H. Zheng. April 2006. Soft Error Analysis and Optimizations of C-elements in Asynchronous Circuits. Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE 2006). 4 pages. Urbana, IL.
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241. Link*, G., N. Vijaykrishnan. March 2006. Thermal Trends in Emerging Technologies. Proceedings of the Seventh International Symposium on Quality Electronic Design (ISQED 2006). pp. 625-632. San Jose, CA. (First author supervised by candidate) (93 regular papers accepted out of 256 submissions) (36% acceptance rate) (Nominated for Best Paper Award)
242. Hung, W.-L., G. Link*, Y. Xie, N. Vijaykrishnan, M. J. Irwin. March 2006. Interconnect and Thermal-aware Floor planning for 3D Microprocessors. Proceedings of the Seventh International Symposium on Quality Electronic Design (ISQED 2006). pp. 98-104. San Jose, CA. (Second author supervised by candidate) (93 regular papers accepted out of 256 submissions) (36% acceptance rate)

243. Wang, F., Y. Xie, N. Vijaykrishnan, M. J. Irwin. March 2006. On-chip Bus Thermal Analysis and Optimization. Proceedings of the Design, Automation and Test in Europe Conference (DATE 2006). pp. 850-855. Munich, Germany. (233 papers accepted out of 834 submissions) (28% acceptance rate)
244. Ricketts*, A. J., K. Irick*, N. Vijaykrishnan, M. J. Irwin. March 2006. Priority Scheduling in Digital Microfluidics-Based Biochips. Proceedings of the Design, Automation and Test in Europe Conference (DATE 2006). pp. 329-334. Munich, Germany. (First two authors supervised by candidate) (233 papers accepted out of 834 submissions) (28% acceptance rate)
245. Kim, J., C. A. Nicopoulos*, D. Park, N. Vijaykrishnan, C. R. Das. March 2006. Performance Enhancement through Early Release and Buffer Optimization in Network-on-Chip Router Architectures. Special Workshop on Future Interconnects and Networks on Chip, in conjunction with the Design, Automation and Test in Europe (DATE 06). Proceedings on CD-ROM. Munich, Germany. (Poster) (Second author supervised by candidate)
246. Theocharides*, T., N. Vijaykrishnan, M. J. Irwin. March 2006. A Parallel Architecture for Hardware Face Detection. Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI 2006). pp. 452-454. Karlsruhe, Germany. (First author co-supervised by candidate) (Poster) (92 papers accepted out of 151 submissions)
247. Srinivasan*, S., N. Vijaykrishnan. March 2006. Variation Aware Placement Scheme for FPGAs. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2006). pp. 422-424. Karlsruhe, Germany. (First author supervised by candidate) (Poster) (92 papers accepted out of 151 submissions)
248. Mutyam*, M., M. Eze, N. Vijaykrishnan, Y. Xie. March 2006. Delay and Energy Efficient Data Transmission for On-Chip Buses. Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI 2006). pp. 355-360. Karlsruhe, Germany. (First author supervised by candidate) (64 full papers accepted out of 151 submissions)
249. Yang*, S., W. Wolf, N. Vijaykrishnan, Y. Xie. March 2006. Reliability-aware SOC Voltage Islands Partition and Floorplan. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2006). pp. 341-347. Karlsruhe, Germany. (First author supervised by candidate) (64 full papers accepted out of 151 submissions)
250. Chen, G., G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. January 2006. Object Duplication for Improving Reliability. Proceedings of the Eleventh Asia and South Pacific Design Automation Conference (ASP-DAC 2006). pp. 140-145. Yokohama City, Japan. (135 out of 432 papers were accepted)
251. Richardson*, T., C. Nicopolus*, N. Vijaykrishnan, D. Park, Y. Xie C. R. Das. January 2006. A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks. Proceedings of IEEE International Conference on VLSI Design. pp. 657-664. Bangalore, India. (First author co-supervised and second author supervised) (88 regular papers accepted out of 328 submissions) (27% acceptance rate)
252. Ramanarayanan*, R., J. S. Kim*, N. Vijaykrishnan, Y. Xie, M. J. Irwin. January 2006. SEAT-LA: A Soft Error Analysis tool for Combinational Logic. Proceedings of Nineteenth International Conference on VLSI Design. pp. 499-502. Bangalore, India. (First author co-supervised and second author supervised) (88 regular papers accepted out of 328 submissions) (27% acceptance rate)
253. Kim, J., D. Park, C. Nicopoulus, N. Vijaykrishnan, C. R. Das. October 2005. Design and Analysis of an NoC Architecture from Performance, Reliability and Energy Perspective. Proceedings of the First Symposium on Architectures for Networking and Communication Systems (ANCS 2005). pp. 173-182. Princeton, NJ. (Third author supervised by candidate) (23 accepted out of 100 submissions) (23% acceptance rate)

254. Pirretti, M. , N. Vijaykrishnan, M. Kandemir, R. Brooks. October 2005. Realistic Models for Sensor Networks Using Key Predistribution Schemes. Proceedings of the Innovations and Commercial Applications of Distributed Sensor Networks Symposium (ICA DSN). Proceedings on CD-ROM. Bethedsa, MD. (First author supervised)
255. Pirretti, M., S. Zhu, N. Vijaykrishnan, P. McDaniel, M. Kandemir, R. Brooks. October 2005. The Sleep Deprivation Attack in Sensor Networks: Analysis and Methods of Defense. Proceedings of the Innovations and Commercial Applications of Distributed Sensor Networks Symposium (ICA DSN). Proceedings on CD-ROM. Bethedsa, MD. (First author supervised) (Selected as best paper)
256. Hung, W., G. Link, Y. Xie, N. Vijaykrishnan, N. Dhanwada J. Conner. October 2005. Temperature-Aware Voltage Islands Architecting in System-on-Chip Design. Proceedings of the IEEE International Conference on Computer Design (ICCD 2005). pp. 689-696. San Jose, CA. (Second author supervised by candidate) (101 papers accepted out of 313 submissions) (32% acceptance rate)
257. Tsai, Y., Y. Xie, N. Vijaykrishnan, M. J. Irwin. October 2005. Three-dimensional cache design using 3DCacti. Proceedings of the IEEE International Conference on Computer Design (ICCD 2005). pp. 519-524. San Jose, CA. (First author supervised by candidate) (101 papers accepted out of 313 submissions) (32% acceptance rate)
258. Dhanwada, N., I. Lin, N. Vijaykrishnan. September 2005. A Power Estimation Methodology for SystemC Transaction Level Models. Proceedings of the International Conference on Hardware/Software Codesign and Synthesis (CODES + ISSS 2005). pp. 142-147. New York, NY. (Second author co-supervised by candidate) (50 papers accepted out of 200 submissions) (25% acceptance rate)
259. Srinivasan, S., F. Angiolini, M. Ruggiero, N. Vijaykrishnan, L. Benini. September 2005. Simultaneous Memory and Bus Partitioning for SoC Architectures. Proceedings of the IEEE International SoC Conference (SOCC 2005). pp. 125-128. Washington, D.C. (First author supervised by candidate)
260. Swankowski, E., N. Vijaykrishnan. September 2005. Dynamic High-Performance Multi-Mode Architectures for AES Encryption. Proceedings of the Annual Military and Aerospace Applications of Programmable Devices and Technologies Conference (MAPLD'05). (CD ROM Proceedings). Washington, D.C.
261. Veezhinathan, K., Sk. Noor Mahammad, V. Muralidaran, N. Vijaykrishnan and V. Chandrasekar. September 2005. Reduced Triple Modular Redundancy for Tolerating SEUs in SRAM-based FPGA. Proceedings of the Annual Military and Aerospace Applications of Programmable Devices and Technologies Conference (MAPLD'05). (CD ROM Proceedings). Washington, D.C.
262. Gayasen, A., N. Vijaykrishnan, M. J. Irwin. June 2005. Exploring Technology Alternatives for Nano-Scale FPGA Interconnects. Proceedings of the Forty-Second Design Automation Conference (DAC'05). pp. 921-926. Anaheim, CA. (First author co-supervised by candidate) (154 papers accepted out of 735 submissions) (21% acceptance rate)
263. Kim, J-H., D. Park, T. Theocharides, N. Vijaykrishnan, C. R. Das. June 2005. A Low Latency Router Supporting Adaptivity for On-Chip Interconnects. Proceedings of the Forty-Second Design Automation Conference (DAC'05). pp. 559-564. Anaheim, CA. (Third author supervised by candidate) (154 papers accepted out of 735 submissions) (21% acceptance rate)
264. Saputra, H., O. Ozturk, N. Vijaykrishnan, M. Kandemir, R. Brooks. May 2005. A Data-driven Approach for Embedded Security. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI '05). pp. 104-109. Tampa, FL. (First author co-supervised by candidate)
265. Lee, J., N. Vijaykrishnan, M. J. Irwin. May 2005. High Performance Array Processor for Video Decoding. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI '05). pp. 28-33. Tampa, FL. (First author co-supervised by candidate)

266. Reddy, S. S., E., V. Chandrasekhar, M. Sashikanth, V. Kamakoti Veezhinathan, N. Vijaykrishnan. April 2005. Online Detection and Diagnosis of Multiple Configuration Upsets in LUTs of SRAM-based FPGAs. Proceedings of the Twelfth Reconfigurable Architectures Workshop (RAW 2005). p. 172a. Denver, CO.
267. Hung, W-L., Y. Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin. March 2005. Thermal-Aware Floor planning Using Genetic Algorithms. Proceedings of the Sixth International Symposium on Quality Electronic Design (ISQED 2005). pp. 634-639. San Jose, CA. (Fourth author supervised and fifth author co-supervised by candidate)
268. Hu, J., F. Li, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. March 2005. Compiler-directed Instruction Duplication for Soft Error Detection. Proceedings of the Design, Automation, and Test in Europe (DATE 2005). pp. 1056-1057. Munich, Germany. (Poster) (First and third authors supervised by candidate)
269. Hung, W-L., Y. Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. March 2005. Thermal-Aware Allocation and Scheduling for Systems-on-a-Chip Design. Proceedings of the Design, Automation, and Test in Europe (DATE 2005). pp. 898-899. Munich, Germany (Poster)
270. Link, G., N. Vijaykrishnan. March 2005. Hotspot Prevention Through Runtime Reconfiguration in Network-On-Chip Designs. Proceedings of the Design, Automation, and Test in Europe (DATE 2005). pp. 648-649. Munich, Germany. (Poster) (First author supervised)
271. Tsai, Y-F., N. Vijaykrishnan, Y. Xie, M. J. Irwin. March 2005. Leakage-Aware Interconnect for On-Chip Network. Proceedings of the Design, Automation, and Test in Europe (DATE 2005). pp. 230-231. Munich, Germany. (Poster) (First author co-supervised by candidate)
272. Srinivasan, S., N. Vijaykrishnan. March 2005. Simultaneous Partitioning and Frequency Assignment for On-chip Bus Architectures. Proceedings of the Design, Automation, and Test in Europe (DATE 2005). pp. 218-223. Munich, Germany. (First author supervised by candidate) (176 papers accepted out of 825 submissions) (21% acceptance rate)
273. Yang, S., W. Wolf, N. Vijaykrishnan, Y. Xie. March 2005. Power Attack Resistant Crypto Design: A Dynamic Voltage and Frequency Switching Approach. Proceedings of the Design, Automation, and Test in Europe (DATE 2005). pp. 64-69. Munich, Germany. (176 papers accepted out of 825 submissions) (21% acceptance rate)
274. Reddy, S. S., E., V. Chandrasekhar, M. Sashikanth, V. Kamakoti, N. Vijaykrishnan. January 2005. Cluster-based Detection of SEU-caused Errors in LUTs of SRAM-based FPGAs. Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC 2005). pp. 1200-1203. Shanghai, China.
275. Srinivasan, S., A. Gayasen, N. Vijaykrishnan, T. Tuan. January 2005. Leakage Control in FPGA Routing Fabric. Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC 2005). pp. 661-664. Shanghai, China. (First author supervised and second author co-supervised by candidate)
276. Yang, S., W. Wolf, W. Wang, N. Vijaykrishnan, Y. Xie. January 2005. Low-Leakage Robust SRAM Cell Design for Sub-100nm Technologies. Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC 2005). pp. 539-544. Shanghai, China.
277. Reddy, S. S., E., S., M. Sashikanth, V. Chandrasekhar, N. Vijaykrishnan, V. Kamakoti. January 2005. Detecting SEU-caused Routing Errors in SRAM-based FPGAs. Proceedings of the Eighteenth International Conference on VLSI Design. pp. 736-741. Kolkata, India. (97 regular papers accepted out of 352 submissions) (28% acceptance rate)
278. Tsai, Y-F., N. Vijaykrishnan, M. J. Irwin, Y. Xie. January 2005. Influence of Leakage Reduction Techniques on Delay/Leakage Uncertainty. Proceedings of the Eighteenth International Conference on VLSI Design. pp. 374-379. Kolkata, India. (First author co-supervised by candidate) (97 regular papers accepted out of 352 submissions) (28% acceptance rate)

279. Irick, K., W. Xu, N. Vijaykrishnan, M. J. Irwin. January 2005. A Nanosensor Array Based VLSI Gas Discriminator. Proceedings of the Eighteenth International Conference on VLSI Design. pp. 241-248. Kolkata, India. (First author co-supervised and second author supervised by candidate) (97 regular papers accepted out of 352 submissions) (28% acceptance rate)
280. Yang, S., W. Wolf, W. Wang, N. Vijaykrishnan, Y. Xie. January 2005. Accurate Stacking Effect Macro-Modeling of Leakage Power in Sub-100nm Circuits. Proceedings of the Eighteenth International Conference on VLSI Design. pp. 165-170. Kolkata, India. (97 regular papers accepted out of 352 submissions) (28% acceptance rate)
281. Theocharides, T., G. Link, N. Vijaykrishnan, M. J. Irwin. January 2005. Implementing LDPC Decoding on Network on Chip. Proceedings of the Eighteenth International Conference on VLSI Design. pp. 134-137. Kolkata, India. (First author co-supervised and second author supervised by candidate)
282. Reddy, S. S., E., S. Kanth, V. Chandrasekhar, S. Srinivasan, N. Vijaykrishnan, V. Kamakoti. December 2004. A Novel CLB Architecture to Detect and Correct SEU in LUTs of SRAM-based FPGAs. Proceedings of the 2004 IEEE International Conference on Field- Programmable Technology (FPT'04). pp. 121-128. Brisbane, Australia. (Accepted 34 full papers out of 122 submissions)
283. Kim, J. S., C. Nicopoulos, N. Vijaykrishnan, Y. Xie, E. Lattanzi. November 2004. A Probabilistic Model for Soft-Error Rate Estimation in Combinatorial Logic. Proceedings of the First International Workshop on Probabilistic Analysis Techniques for Real Time and Embedded Systems (PARTES 2004). Pisa, Italy.
284. Unlu, K., V. Degalahal, M. S. Cetiner, N. Vijaykrishnan, M. J. Irwin. November 2004. Testing Neutron-Included Soft Errors in Semiconductors. Proceedings of the American Nuclear Society Winter Meeting. pp. 825-826. Washington, D.C. (Second author supervised by candidate) (Equal contributions by authors)
285. Srinivasan, S., A. Gayasen, N. Vijaykrishnan, M. Kandemir, Y. Xie, M. J. Irwin. November 2004. Improving Soft-error Tolerance of FPGA Configuration Bits. Proceedings of the International Conference on Computer Aided Design (ICCAD-2004). pp. 107-110. San Jose, CA. (First author supervised and second author co-supervised by candidate) (24% acceptance rate)
286. Kang, B. T., N. Vijaykrishnan, M. J. Irwin. November 2004. Analyzing Software Influences on Substrate Noise: An ADC Perspective. Proceedings of the International Conference on Computer Aided Design (ICCAD-2004). pp. 916-922. San Jose, CA. (Equal contributions by authors) (24% acceptance rate)
287. Chen, G., M. Kandemir, N. Vijaykrishnan, M. J. Irwin. October 2004. Field-level Analysis for Heap Space Optimization in Embedded Java. Proceedings of the International Symposium on Memory Management (ISMM'04). pp. 131-142. Vancouver, British Columbia, Canada. (Contributing author) (35% acceptance rate)
288. Lee, J., N. Vijaykrishnan, M. J. Irwin, R. Radhakrishnan. October 2004. Inverse Discrete Cosine Transform Architecture Exploiting Sparseness and Symmetry Properties. Proceedings of the IEEE Workshop on Signal Processing Systems (SiPS'04). pp. 361-366. Austin, TX. (First author co-supervised by candidate)
289. Hung, W., C. Addo-Quaye, T. Theocharides, Y. Xie, N. Vijaykrishnan, M. J. Irwin. October 2004. Thermal-Aware IP Virtualization and Placement for Networks-on-Chip Architecture. Proceedings of the International Conference on Computer Design (ICCD 2004). pp. 430-437. San Jose, CA. (Second author supervised and fourth author co-supervised by candidate)
290. Xie, Y., L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. September 2004. Reliability-aware Cosynthesis for Embedded Systems. Proceedings of the Fifteenth IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP'04). pp. 41-50. Galveston, TX. (Second author co-supervised by candidate)

291. Tsai, Y-F., A. Hegde, N. Vijaykrishnan, M. J. Irwin. September 2004. ChipPower: An Architecture-Level Leakage Simulator. Proceedings of the IEEE International Systems-on-Chip Conference (SOCC 2004). pp. 395-398. Santa Clara, CA. (First author co-supervised by candidate)
292. Theocharides, T., G. Link, N. Vijaykrishnan, M. J. Irwin, V. Srikantam. September 2004. A Generic Reconfigurable Neural Network Architecture Implemented as a Network on Chip. Proceedings of the IEEE International Systems-on-Chip Conference (SOCC 2004). pp. 191-194. Santa Clara, CA. (First author co-supervised and second author supervised by candidate)
293. Kang, B. T., N. Vijaykrishnan, M. J. Irwin, T. Theocharides. September 2004. Power-Efficient Implementation of Turbo Decoder in SDR Systems. Proceedings of the IEEE International Systems-on-Chip Conference (SOCC 2004). pp. 119-122. Santa Clara, CA. (Fourth author supervised by candidate)
294. Chen, G., M. Kandemir, N. Vijaykrishnan, A. Sivasubramaniam, M. J. Irwin. September 2004. Analyzing Object Error Behavior in Embedded JVM Environments. Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and Systems Synthesis (CODES+ISSS'04). pp. 230-235. Stockholm, Sweden. (Equal contributions by authors) (39 papers accepted out of 159 submissions) (25% acceptance rate)
295. Gayasen, A., K. Lee, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, T. Tuan. August-September 2004. A Dual Vdd Low-power FPGA Architecture. Proceedings of the International Conference on Field-programmable Logic and Its Applications (FPL'04). pp. 145-157. Antwerpen, Belgium. (First two authors co-chaired by candidate)
296. Hung, W., Y. Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. August 2004. Total Power Optimization Through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing With Stack Forcing. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED 2004). pp. 144-149. Newport Beach, CA. (Contributing author) (34% acceptance rate)
297. Li, L., V. Degalahal, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. August 2004. Soft Error and Energy Consumption Interactions: A Data Cache Perspective. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED 2004). pp. 132-137. Newport Beach, CA. (First author co-supervised and second author supervised by candidate) (34% acceptance rate)
298. Yang, S., W. Wolf, N. Vijaykrishnan. June 2004. Search Speed and Power Driven Integrated Software and Hardware Optimizations for Motion Estimation Algorithms. Proceedings of the 2004 IEEE International Conference on Multimedia and Expo (ICME 2004). pp. 707-710. Taipei, Taiwan. (Contributing author) [218 accepted out of 740 submissions] (29% acceptance rate)
299. Saputra, H., G. Chen, R. Brooks, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. June 2004. Code Protection for Resource-constrained Embedded Devices. Proceedings of the ACM SIGPLAN/SIGBED 2004 Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES '04). pp. 240-248. Washington, D.C. (First author supervised by candidate) [28 accepted out of 120 submissions] (23% acceptance rate)
300. Tsai, Y-F., D. Duarte, N. Vijaykrishnan, M. J. Irwin. May 2004. Impact of Process Scaling on the Efficacy of Leakage Reduction Scheme. Proceedings of the International Conference on IC Design and Technology (ICICDT 2004). pp. 3-11. Austin, TX. (First author co-supervised by candidate)
301. Lee, J., N. Vijaykrishnan, M. J. Irwin. May 2004. Efficient VLSI Implementation of Inverse Discrete Cosine Transform. Proceedings of the International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2004). pp. 177-180. Montreal, Canada. (First author co-supervised by candidate) [1262 accepted out of 2,434 papers] (52% acceptance rate)
302. Xu, W., N. Vijaykrishnan, Y. Xie, M. J. Irwin. April 2004. Design of a Nanosensor Array Architecture. Proceedings of the 2004 Great Lakes Symposium on VLSI (GLSVLSI 2004). pp. 298-303. Boston, MA. (First author supervised by candidate) [23 full papers accepted out of 235 submissions] (10% acceptance rate)

303. Lattanzi, E., A. Bogliolo, A. Gayasen, M. Kandemir, N. Vijaykrishnan, L. Benini. April 2004. Improving Java Performance by Dynamic Method Migration on FPGAs. Proceedings of the Eleventh Reconfigurable Architectures Workshop (RAW 2004). p. 134. Santa Fe, NM. (Third author co-supervised by candidate)
304. Swankoski, E., R. Brooks, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. April 2004. A Parallel Architecture for Secure FPGA Symmetric Encryption. Proceedings of the Eleventh Reconfigurable Architectures Workshop (RAW 2004). p. 132. Santa Fe, NM.
305. Degalahal, R. Ramanarayanan, N. Vijaykrishnan, Y. Xie, M. J. Irwin. March 2004. The Effect of Threshold Voltages on the Soft Error Rate. Proceedings of the Fifth International Symposium on Quality Electronic Design (ISQED 2004). pp. 503-508. San Jose, CA. (First author supervised and second author co-supervised by candidate)
306. Gayasen, A., Y. Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. February 2004. Reducing Leakage Energy in FPGAs Using Region-constrained Placement. Proceedings of the ACM International Symposium on Field-Programmable Gate Arrays (FPGA'04). pp. 51-58. Monterey, CA. (First author co-supervised by candidate)
307. Theocharides, T., G. Link, E. Swankoski, N. Vijaykrishnan, M. J. Irwin, H. Schmit. February 2004. Evaluating Alternative Implementations for LDPC Decoder Check Node Function. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2004). pp. 77-82. Lafayette, LA. (First author co-supervised and second author supervised by candidate) [29 accepted out of 123 submissions] (24% acceptance rate)
308. Pirreti, M., G. Link, R. Brooks, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. February 2004. Fault-tolerant Algorithms for Network-on-chip Interconnect. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2004). pp. 46-51. Lafayette, LA. (Second author supervised by candidate) [29 accepted out of 123 submissions] (24% acceptance rate)
309. Kadayif, I., I. Kolcu, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. February 2004. Exploiting Processor Workload Heterogeneity for Reducing Energy Consumption in Chip Multiprocessor. Proceedings of the Design Automation and Test in Europe Conference (DATE'04). Volume 2, pp. 158-163. Paris, France. [181 accepted out of 780 submissions] (23% acceptance rate)
310. Hu, J. S., N. Vijaykrishnan, S. Kim, M. Kandemir, M. J. Irwin. February 2004. Scheduling Reusable Instructions for Power Reduction. Proceedings of the Design Automation and Test in Europe Conference (DATE'04). Volume 1, pp. 148-155. Paris, France. (First author supervised by candidate) [181 accepted out of 780 submissions] (23% acceptance rate)
311. Li, L., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. February 2004. A Crosstalk Aware Interconnect with Variable Cycle Transmission. Proceedings of the Design Automation and Test in Europe Conference (DATE'04). Volume 1, pp. 102-107. Paris, France. (First author co-supervised by candidate) [181 accepted out of 780 submissions] (23% acceptance rate)
312. Hu, J. S., N. Vijaykrishnan, M. J. Irwin. February 2004. Exploring Wakeup-Free Instruction Scheduling. Proceedings of the Tenth International Symposium on High Performance Computer Architecture (HPCA-10). pp. 232-243. Madrid, Spain. (First author supervised by candidate) [27 accepted out of 151 submissions] (17.8% acceptance rate)
313. Lee, J., N. Vijaykrishnan, M. J. Irwin, W. Wolf. January 2004. An Architecture for Motion Estimation in the Transform Domain. Proceedings of the Seventeenth International Conference on VLSI Design. pp. 1077-1082. Mumbai, India. (First author co-supervised by candidate)
314. Derenzo, M., M. J. Irwin, N. Vijaykrishnan. January 2004. Designing Leakage-Aware Multipliers. Proceedings of the Seventeenth International Conference on VLSI Design. pp. 654-657. Mumbai, India.
315. Theocharides, T., G. Link, N. Vijaykrishnan, M. J. Irwin, W. Wolf. January 2004. Embedded Hardware Face Detection. Proceedings of the Seventeenth International Conference on VLSI Design. pp. 133-138. Mumbai, India. (First author co-supervised and second author supervised by candidate)

316. Yang, S., W. Wolf, N. Vijaykrishnan. December 2003. Power Modeling of VLSI Motion Estimation Architecture. Proceedings of the Fifth Workshop on Media and Streaming Processors (MSP), held in conjunction with MICRO-6. pp. 39-49. San Diego, CA.
317. Vijaykrishnan, N. December 2003. Designing Energy-Efficient and Reliable Hardware. Proceedings of the IFIP International Conference on VLSI. pp. 6-9. Darmstadt, Germany (Invited)
318. Li, L., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. November 2003. Adaptive Error Protection for Energy Efficiency. Proceedings of the International Conference on Computer Aided Design (ICCAD-2003). pp. 2-7. San Jose, CA. [130 accepted out of 490 submissions] (26.5% acceptance rate) (First author co-supervised by candidate)
319. Chen, G., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, B. Mathiske, M. Wolczko. October 2003. Heap Compression for Memory-constrained Java Environments. Proceedings of the Eighteenth Annual ACM SIGPLAN Conference on Object-Oriented Programming, Systems, Languages, and Applications (OOPSLA'03). pp. 282-301. Anaheim, CA. [26 accepted out of 142 submissions] (18.3% acceptance rate)
320. De La Luz, V., A. Sivasubramaniam, M. Kandemir, M. J. Irwin, N. Vijaykrishnan. October 2003. Reducing dTLB Energy Through Dynamic Resizing. Proceedings of the Twenty-First International Conference on Computer Design (ICCD). pp. 358-363. San Jose, CA. [78 accepted out of 233 submissions] (33.4% acceptance rate)
321. Chen, G., N. Vijaykrishnan, M. Kandemir, M. J. Irwin, M. Wolczko. October 2003. Tracking Object Life Cycle for Leakage Energy Optimization. Proceedings of the CODES-ISSS Merged Conference (CODES/ISSS'03). pp. 213-218. Newport Beach, CA. [30 accepted out of 143 submissions] (21% acceptance rate)
322. Hegde, A., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. October 2003. VL-CDRAM: Variable Line Sized Cached DRAMs. Proceedings of the CODES-ISSS Merged Conference (CODES/ISSS'03). pp. 132-137. Newport Beach, CA. (First author supervised by candidate) [30 accepted out of 143 submissions] (21% acceptance rate)
323. Duarte, D., N. Vijaykrishnan, M. J. Irwin. September 2003. Energy and Timing Characterization of VLSI Charge-pump Phase-locked Loops. Proceedings of the IEEE International SOC Conference (ASIC/SOC'03). pp. 341-344. Portland, OR.
324. Kang, B., N. Vijaykrishnan, M. J. Irwin, D. Duarte. September 2003. Substrate Noise Detector for Noise Tolerant Mixed-Signal IC. Proceedings of the IEEE International SOC Conference (ASIC/SOC'03). pp. 279-280. Portland, OR. (First author co-supervised by candidate)
325. Ramanarayanan, R., V. Degalahal, N. Vijaykrishnan, M. J. Irwin, D. Duarte. September 2003. Analysis of Soft-Error Rate for Flip-Flops and Scannable Latches. Proceedings of the IEEE International SOC Conference (ASIC/SOC'03). pp. 231-234. Portland, OR. (First author co-supervised and second author supervised by candidate)
326. Chen, G., G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. September 2003. Energy-aware Code Cache Management for Memory-constrained Java Devices. Proceedings of the IEEE International SOC Conference (ASIC/SOC'03). pp. 179-182. Portland, OR.
327. Li, L., N. Vijaykrishnan, M. Kandemir, M. J. Irwin, I. Kadayif. September 2003. CCC: Crossbar Connected Caches for Reducing Energy. Proceedings of the Euromicro Symposium on Digital System Design (DSD'2003). pp. 41-48. Belek, Turkey.
328. Lee, J., N. Vijaykrishnan, M. J. Irwin, R. Chandramouli. August 2003. An Efficient Implementation of Hierarchical Image Coding. Proceedings of the IEEE Workshop on Signal Processing Systems (SIPS'03). pp. 363-368. Seoul, Korea. (First author co-supervised by candidate)
329. Saputra, H., N. Vijaykrishnan, M. Kandemir, R. Brooks, M. J. Irwin. August 2003. Exploiting Value Locality for Secure Energy Aware Communication. Proceedings of the IEEE Workshop on Signal Processing Systems (SIPS'03). pp. 116-121. Seoul, Korea. (First author co-supervised by candidate)

330. Kim, E. J., K. H. Yum, G. Link, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, C. R. Das. August 2003. Energy Optimization Techniques in Cluster Interconnects. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03). pp. 459-464. Seoul, Korea. (Third author supervised by candidate) [17 accepted as long out of 221 submissions] (7.6% acceptance rate)
331. Hu, J. S., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. August 2003. Exploiting Program Hotspots and Code Sequentiality for Instruction Cache Leakage Management. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03). pp. 402-407. Seoul, Korea. (First author supervised by candidate) [91 accepted out of 221 submissions] (41% acceptance rate)
332. Kim, S., N. Vijaykrishnan, M. J. Irwin, L. K. John. August 2003. On Load Latency in Low-Power Caches. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03). pp. 258-261. Seoul, Korea. (First author supervised by candidate) [91 accepted out of 221 submissions] (41% acceptance rate)
333. Kim, H. S., N. Vijaykrishnan, M. Kandemir, E. Brockmeyer, F. Catthoor, M. J. Irwin. August 2003. Estimating Influence of Data Layout Optimizations on SDRAM Energy Consumption. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03). pp. 40-43. Seoul, Korea. (First author supervised by candidate) [91 accepted out of 221 submissions] (41% acceptance rate)
334. Bhatkar, A., R. Chandramouli, N. Vijaykrishnan, M. J. Irwin. July 2003. Computation and Transmission Energy Modeling Through Profiling for MPEG4 Video Transmission. Proceedings of the IEEE International Conference on Multimedia & Expo (ICME 2003). Volume 1, pp. 281-284. Baltimore, MD.
335. Kim, H. S., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. June 2003. Adapting Instruction Level Parallelism for Optimizing Leakage in VLIW Architectures. Proceedings of the Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES'03). pp. 275-283. San Diego, CA. [29 accepted out of 128 submissions] (23% acceptance rate)
336. Tsai, Y-F., D. Duarte, N. Vijaykrishnan, M. J. Irwin. June 2003. Implications of Technology Scaling on Leakage Reduction Techniques. Proceedings of the Fortieth Design Automation Conference. pp. 187-190. Anaheim, CA. (First author co-supervised by candidate) (24% acceptance rate)
337. Schmit, H., T. Kroll, M. Khusid, I. Kourtev, N. Vijaykrishnan, D. Landis. June 2003. The Sandbox Experience Course. Proceedings of the International Conference on Microsystem Education. pp. 41-42. Anaheim, CA.
338. Chen, G., B. Kang, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, R. Chandramouli. April 2003. Energy-Aware Compilation and Execution in Java-Enabled Mobile Devices. Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS 2003). (CD-ROM). Nice, France. (Second author co-supervised by candidate) [119 accepted out of 407 submissions] (29.3% acceptance rate)
339. Gurumurthi, S., N. An, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. April 2003. Energy and Performance Considerations in Work Partitioning for Mobile Spatial Queries. Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS 2003). (CD-ROM). Nice, France. [119 accepted out of 407 submissions] (29.3% acceptance rate)
340. Zhang, W., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, V. De. March 2003. Compiler Support for Reducing Leakage Energy Consumption. Proceedings of International Conference on Design Automation and Test in Europe (DATE 2003). pp. 11146-11147. Munich, Germany. (Equal contributions by authors) [20 accepted out of 590 submissions] (34% acceptance rate)

341. Saputra, H., N. Vijaykrishnan, M. Kandemir, M. J. Irwin, R. Brooks, S. Kim, W. Zhang. March 2003. Masking the Energy Behavior of DES Encryption. Proceedings of International Conference on Design Automation and Test in Europe (DATE 2003). pp. 10084-10089. Munich, Germany. (First author co-supervised by candidate) (Equal contributions) [98 long papers accepted out of 590 submissions] (16.6% acceptance rate for long papers)
342. Gurumurthi, S., J. Zhang, A. Sivasubramaniam, M. Kandemir, H. Franke, N. Vijaykrishnan, M. J. Irwin. March 2003. Interplay of Energy and Performance for Disk Arrays Running Transaction Processing Workloads. Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS'03). pp. 123-132. Austin, TX. (Contributing author) [22 accepted out pf 62 submissions] (35.4% acceptance rate)
343. Hu, J. S., N. Vijaykrishnan, M. J. Irwin, M. Kandemir. February 2003. Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch. Proceedings of the IEEE Annual Symposium on VLSI (ISVLSI'03). pp. 127-132. Tampa, FL. (First author supervised by candidate) [26 accepted out of 115 submissions] (22.6% acceptance rate)
344. Degalahal, V., N. Vijaykrishnan, M. J. Irwin. January 2003. Analyzing Soft Errors in Leakage Optimized SRAM Designs. Proceedings of the Sixteenth International Conference on VLSI Design. pp. 539-545. New Delhi, India. (First author supervised by candidate) [84 accepted out of 210 submissions] (40% acceptance rate)
345. Chen, G., M. Kandemir, N. Vijaykrishnan, M. J. Irwin. November 2002. Penn Bench: A Benchmark Suite for Embedded Java. Proceedings of the Fifth Annual IEEE Workshop on Workload Characterization (WWC'02). pp. 71-80. Austin, TX. (Equal contributions by authors)
346. Zhang, W., J. S. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. November 2002. Compiler-directed instruction cache leakage optimization. Proceedings of the Thirty-Fifth Annual International Symposium on Microarchitecture (MICRO-35). pp. 208-218. Istanbul, Turkey. (Second and third authors supervised by candidate) (Equal contributions by authors) (36 accepted out of 150 submissions) (24% acceptance rate)
347. Li, T., L. K. John, A. Sivasubramaniam, N. Vijaykrishnan, J. Rubio. October 2002. Understanding and Improving Operating System Effects in Control Flow Transfer. Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X). San Jose, CA. pp. 68-80. (Contributing author) [24 accepted out of 130 submissions] (18% acceptance rate)
348. Charles, D., A. Hurson, N. Vijaykrishnan. October 2002. Improving ILP with Instruction-reuse Cache Hierarchy. Proceedings of the Fifth International Conference on Algorithms and Architectures for Parallel Processing. pp. 206-213. Beijing, China. (First author supervised by candidate)
349. Zhao, J., R. Chandramouli, N. Vijaykrishnan, M. J. Irwin, B. Kang, S. Somasundaram. September 2002. Influence of MPEG-4 Parameters on System Energy. Proceedings of the Fifteenth Annual IEEE International ASIC/SOC Conference. pp. 137-142. Rochester, NY. (First author supervised and fifth author co-supervised by candidate)
350. Esakkimuthu, G., N. Vijaykrishnan, M. J. Irwin. September 2002. An Analytical Power Estimation Model for Crossbar Interconnects. Proceedings of the Fifteenth Annual IEEE International ASIC/SOC Conference. pp.119-123. Rochester, NY. (First author supervised by candidate)
351. Ramanarayanan, R., N. Vijaykrishnan, M. J. Irwin. September 2002. Characterizing Dynamic and Leakage Power Behavior in Flip-Flops. Proceedings of the Fifteenth Annual IEEE International ASIC/SOC Conference. pp. 433-437. Rochester, NY. (First author co-supervised by candidate)
352. Duarte, D., N. Vijaykrishnan, M. J. Irwin. September 2002. Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques. Proceedings of the Fifteenth Annual IEEE International ASIC/SOC Conference. pp. 244-248. Rochester, NY. (Contributing author)

353. Kim, S., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. September 2002. Predictive Precharging for Bitline Leakage Energy Reduction. Proceedings of the Fifteenth Annual IEEE International ASIC/SOC Conference. pp. 36-40. Rochester, NY. (First author supervised by candidate)
354. Li, L., I. Kadayif, Y-F. Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, A. Sivasubramaniam. September 2002. Leakage Energy Management in Cache Hierarchies. Proceedings of the Eleventh International Conference on Parallel Architectures and Compilation Techniques (PACT 2002). pp. 131-140. Charlottesville, VA. (First and third authors co-supervised by candidate) [25 accepted out of 119 submissions] (21% acceptance rate)
355. Duarte, D., N. Vijaykrishnan, M. J. Irwin, H. S. Kim, G. McFarland. September 2002. Scaling of the Effectiveness of Power Reduction Schemes and the Impact of Temperature Management. Proceedings of the International Conference on Computer Design (ICCD 2002). pp. 382-387 Freiburg, Germany. (Fourth author supervised by candidate) [47 long papers accepted out of 173 submissions] (27% acceptance rate)
356. Chen, G., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, M. Wolczko. August 2002. Adaptive Garbage Collection for Battery-Operated Environments. Proceedings of the Second USENIX JavaTM Virtual Machine Research and Technology Symposium (JVM'02). pp. 1-12. San Francisco, CA. (Equal Contributions by authors) [18 accepted out of 50 submissions] (36% acceptance rate)
357. De La Luz, V., A. Sivasubramaniam, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. June 2002. Scheduler-Based DRAM Energy Management. Proceedings of the Thirty-Ninth Design Automation Conference (DAC). pp. 697-702. New Orleans, LA. (Contributing author) [148 accepted out of 491 submissions] (30% acceptance rate)
358. Hu, J. S., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, H. Saputra, W. Zhang. June 2002. Compiler-Directed Cache Polymorphism. Proceedings of the ACM SIGPLAN Joint Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES'02) and Software and Compilers for Embedded Systems (SCOPES'02). pp. 165-174. Berlin, Germany. (First author supervised and fifth author co-supervised by candidate) [25 accepted out of 73 submissions] (34% acceptance rate)
359. Saputra, H., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, J. S. Hu, C-H. Hsu, U. Kremer. June 2002. Energy-Conscious Compilation Based on Voltage Scaling. Proceedings of the ACM SIGPLAN Joint Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES'02) and Software and Compilers for Embedded Systems (SCOPES'02). pp. 2-10. Berlin, Germany. (First author co-supervised and fifth author supervised by candidate) [25 accepted out of 73 submissions] (34% acceptance rate)
360. Chen, G., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Wolf. May 2002. Energy Savings Through Compression in Embedded Java Environments. Proceedings of the ACM/SIGDA/SIGSOFT Tenth International Conference on Hardware/Software Codesign (CODES '02). pp.163-168. Estes Park, CO. (Equal contributions by authors) [25 full papers accepted out of 75 submissions] (33% acceptance rate)
361. Kang, B-T., N. Vijaykrishnan, M. J. Irwin, R. Chandramouli. May 2002. Power Efficient Adaptive M-QAM Design Using Adaptive Pipelined Analog-to-Digital Converter. Proceedings of the International Conference on Acoustics, Speech and Signal Processing (ICASSP 2002). (CD ROM Proceedings). Orlando, FL. (First author co-supervised by candidate) [1007 accepted out of 1770 submissions] (56% acceptance rate)
362. Kadayif, I., M. Kandemir, N. Vijaykrishnan, M. J. Irwin. April 2002. Hardware-Software Co-Adaption for Data-Intensive Embedded Applications. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2002). pp. 20-25. Pittsburgh, PA. (Equal contributions by authors)
363. Duarte, D., N. Vijaykrishnan, M. J. Irwin, Y-F. Tsai. April 2002. Impact of Technology Scaling on the Clock System Power. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2002). pp. 59-64. Pittsburgh, PA. (Fourth author co-supervised by candidate)

364. Sivasubramaniam, A., M. Kandemir, N. Vijaykrishnan, M. J. Irwin. April 2002. Designing Energy-Efficient Software. Proceedings of the Next Generation Software Workshop, held in conjunction with the International Parallel and Distributed Processing Symposium (IPDPS 2002). p. 176. Fort Lauderdale, FL. (Equal contributions by authors)
365. Kadayif, I., N. Orr, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. March 2002. Instruction Selection/Scheduling Using an Energy-aware Instruction Set Architecture. Proceedings of the Sixth Workshop of Languages, Compilers, and Runtime Systems for Scalable Computers (LCR '02). pp. 1-10. Washington, D.C.
366. Duarte, D., N. Vijaykrishnan, M. J. Irwin. March 2002. A Complete Phase-Locked Loop Power Consumption Model. Proceedings of International Conference on Design Automation and Test in Europe (DATE 2002). p. 1108. Paris, France. (Contributing author) (44% acceptance rate)
367. Hu, J. S., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. March 2002. Power-Efficient Trace Caches. Proceedings of International Conference on Design Automation and Test in Europe (DATE 2002). p. 1091. Paris, France. (First author supervised by candidate) (44% acceptance rate)
368. Kadayif, I., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramaniam. March 2002. EAC: A Compiler Framework for High-Level Energy Estimation and Optimization. Proceedings of the International Conference on Design Automation and Test in Europe (DATE). pp. 436-442. Paris, France. (Equal contributions by authors) [88 accepted as long papers out of 476 submissions] (18% acceptance rate for long papers)
369. Gurumurthi, S., A. Sivasubramaniam, M. J. Irwin, N. Vijaykrishnan, M. Kandemir, T. Li, L. K. John. February 2002. Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach. Proceedings of the Eighth International Symposium on High-Performance Computer Architecture (HPCA-8). pp. 141-150. Cambridge, MA. (Equal contributions by Authors) [26 accepted out of 130 submissions] (20% acceptance rate)
370. Chen, G., R. Shetty, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, M. Wolczko. February 2002. Tuning Garbage Collection in an Embedded Java Environment. Proceedings of the Eighth International Symposium on High-Performance Computer Architecture (HPCA-8). pp. 92-103. Cambridge, MA. (Second author supervised) [26 accepted out of 130 submissions] (20% acceptance rate)
371. Duarte, D., Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin. January 2002. Evaluating Run-Time Techniques for Leakage Power Reduction. Proceedings of the Seventh Asia and South Pacific Design Automation Conference and the Fifteenth International Conference on VLSI Design (VLSI Design/ASP-DAC '02). Bangalore, India. pp. 31-38. (Second author co-supervised) [113 accepted out of 269 submissions] (42% acceptance rate)
372. De La Luz, V., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramaniam, I. Kolcu. January 2002. Compiler-Directed Array Interleaving for Reducing Energy in Multi-Bank Memories. Proceedings of the Seventh Asia and South Pacific Design Automation Conference (ASP-DAC '02) and the Fifteenth International Conference on VLSI Design (VLSI Design 2002). pp. 288 -293. Bangalore, India. (Contributing author) [113 accepted out of 269 submissions] (42% acceptance rate)
373. Zhang, W., N. Vijaykrishnan, M. Kandemir, M. J. Irwin, D. Duarte, Y-F. Tsai. December 2001. Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction. Proceedings of the Thirty-Fourth Annual International Symposium on Microarchitecture (MICRO-34). pp. 102-113. Austin, TX. (Equal contributions by authors) (Sixth author co-supervised by candidate) (Equal contributions by authors) [29 accepted out of 144 submissions] (20% acceptance rate)
374. Kirubanandan, N., A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. December 2001. Memory Energy Characterization and Optimization for the SPEC2000 Benchmarks. Proceedings of the IEEE Fourth Annual Workshop on Workload Characterization (WWC-4) (held in conjunction with MICRO-34). pp. 193-201. Austin, TX. (First author supervised by candidate) (~50% acceptance rate)

375. Kim, S., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. November 2001. Energy-Efficient Instruction Cache Using Page-Based Placement. Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2001). pp. 229-237. Atlanta, GA. (First author supervised by candidate) [28 accepted out 80 submissions] (35% acceptance rate)
376. Duarte, D., N. Vijaykrishnan, M. J. Irwin, M. Kandemir. September 2001. Evaluating the Impact of Architectural-Level Optimizations on Clock Power. Proceedings of the Fourteenth Annual IEEE International ASIC/SOC Conference. pp. 447-451. Washington, D.C. (Contributing author) (Proceedings were published, but Conference was cancelled due to National Disaster)
377. Thirugnanam, G., N. Vijaykrishnan, M. J. Irwin. September 2001. A Novel Low Power CAM Design. Proceedings of the Fourteenth Annual IEEE International ASIC/SOC Conference. pp. 198-202. Washington, D.C. (First author supervised) (Proceedings were published, but Conference was cancelled due to National Disaster)
378. Tomar, S., S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. September 2001. Use of Local Memory for Efficient Java Execution. Proceedings of the International Conference on Computer Design (ICCD 2001). pp. 468-473. Austin, TX. (First and second authors supervised by candidate) [61 accepted out of 181 submissions] (34% acceptance rate)
379. Kim, H. S., N. Vijaykrishnan, M. Kandemir, M. J. Irwin. September 2001. A Framework for Exploring Energy-Efficient VLIW Architectures. Proceedings of the International Conference on Computer Design (ICCD 2001). pp. 40-45. Austin, TX. (First author supervised) [61 accepted out of 181 submissions] (34% acceptance rate)
380. Hezavei, J., N. Vijaykrishnan, M. J. Irwin, M. Kandemir, D. Duarte. September 2001. Input Sensitive High-level Power Analysis. Proceedings of the 2001 IEEE Workshop on SiGNAL Processing Systems (SiPS 2001). pp. 149-156. Antwerp, Belgium. (First author supervised by candidate) (~70% acceptance rate)
381. An, N., A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, S. Gurumurthi. September 2001. Analyzing Energy Behavior of Spatial Access Methods for Memory-Resident Data. Proceedings of the Twenty Seventh International Conference on Very Large Databases (VLDB 2001). pp. 411-420. Rome, Italy. (Contributing author) [59 accepted out of 339 submissions] (17% acceptance rate)
382. Kim, S., N. Vijaykrishnan, M. Kandemir, A. Sivasubramaniam, M. J. Irwin, E. Geethanjali. August 2001. Power-aware Partitioned Cache Architectures. Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED '01). pp. 64-67. Huntingdon Beach, CA. (First and sixth authors supervised by candidate) [73 accepted out of 194 submissions] (38% acceptance rate)
383. Khosla, P., H. Schmit, M. J. Irwin, N. Vijaykrishnan, T. Cain, S. Levitan, D. Landis. June 2001. SoC Design Skills: Collaboration Builds a Stronger SoC Design Team. Proceedings of the 2001 International Conference on Microelectronic Systems Education (MSE 2001). pp. 42-43. Las Vegas, NV. (Contributing author)
384. Kadayif, I., M. Kandemir, N. Vijaykrishnan, M. J. Irwin, J. Ramanujam. June 2001. Morphable Cache Architectures: Potential Benefits. Proceedings of ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES 2001). pp. 128-137. Snowbird, UT. (Equal contributions by authors) [20 accepted out of 68 submissions] (29% acceptance rate)

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2. N. Vijaykrishnan and M. Wolczko (editors). Java Microarchitectures. April 2002. Kluwer Academic.

Parts of Books.

1. V Narayanan, Y Cao, P Panda, N Reddy Challapalle, X Du, Y Kim, et. al. 2023. Overview of Recent Advancements in Deep Learning and Artificial Intelligence. Advances in Electromagnetics Empowered by Artificial Intelligence and Deep Neural Networks. 2023.
2. Kaisheng Ma, Shuangchen Li, Vijaykrishnan Narayanan, Yuan Xie. 2020. Nonvolatile Processor Architecture Exploration for Energy-Harvesting Application Scenarios. In Embedded, Cyber-Physical, and IoT Systems. pp. 175-202 (Book Chapter)
3. Ahmedullah Aziz, Sandeep Krishna Thirumala, Danni Wang, Sumitha George, Xueqing Li, Suman Datta, Vijaykrishnan Narayanan, Sumeet Kumar Gupta. 2019. Sensing in Ferroelectric Memories and Flip-Flops. In Sensing of Non-Volatile Memory Demystified. pp. 47-80. Springer. (Book Chapter)
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5. Eachempati*, S., R. Das, N. Vijaykrishnan, Y. Xie, S. Datta, C. R. Das. February 2011. HeTERO: Hybrid Topology Exploration for RF Based On Chip Networks. In Communication Architectures for Systems-on-Chip. J. L. Ayala, Editor. CRC Press. (First author co-supervised by candidate) (Book chapter)
6. Eachempati*, S., A. Gayasen*, N. Vijaykrishnan, M. J. Irwin. January 2011. Leveraging Emerging Technology Through Architectural Exploration for the Routing Fabric of Future FPGAs. Nanoelectronic Circuit Design. N. Jha, D. Chen, Editors. Springer. (First two authors co-supervised by candidate) (Book chapter)
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23. Kandemir, M., N. Vijaykrishnan, M. J. Irwin. 2002. Compiler Optimizations for Low-Power Systems. Book Chapter for Power Aware Computing. Edited by R. Graybill and R. Melhem. Kluwer Academic/Plenum Publishers. pp. 191-210. (Equal contributions by authors)
24. Li, T., L. K. John, N. Vijaykrishnan, A. Sivasubramaniam. May 2001. Characterizing Operating System Activity in SPECjvm98 Benchmarks. Book Chapter for Characterization of Contemporary Workloads. pp. 53-82. Kluwer Academic. Edited by L. K. John and A. M. Grizzaffi-Maynard. (Contributing author)
25. Kim, H. S., M. Kandemir, N. Vijaykrishnan, M. J. Irwin. May 2001. Characterization of Memory Energy Behavior. Book Chapter for Characterization of Contemporary Workloads. pp. 165-180. Kluwer Academic. Edited by L. K. John and A. M. Grizzaffi-Maynard. (First author co-supervised by candidate)

Patents

Granted:

1. Xueqing Li, Sumitha George, John Sampson, Sumeet Gupta, Suman Datta, Vijaykrishnan Narayanan, Kaisheng Ma. Nonvolatile digital computing with ferroelectric FET. US Patent 10475514
2. Sumeet Kumar Gupta, Ahmedullah Aziz, Nikhil Shukla, Suman Datta, Xueqing Li, Vijaykrishnan Narayanan. Low power sense amplifier based on phase transition material. US Patent number:10262714.
3. Huichu Liu, Ramesh Vaddi, Vijaykrishnan Narayanan, Suman Datta, Moon Seok Kim, Xueqing Li, Alexandre Schmid, Mahsa Shoaran, Unsuk Heo. Low power nanoelectronics. US Patent number: 9800094
4. Huichu Liu, Ramesh Vaddi, Vijaykrishnan Narayanan, Suman Datta. Power rectifier using tunneling field effect transistor. US Patent number: 9391068
5. Vinay Saripalli, Dheeraj Mohata, Saurabh Mookherjea, Suman Datta, Vijaykrishnan Narayanan. TFET based 4T memory devices. US Patent number: 8638591
6. Jawar Singh, Ramakrishnan Krishnan, Saurabh Mookerjea, Suman Datta, Vijaykrishnan Narayanan. TFET based 6T SRAM cell. US Patent number: 8369134
7. Kevin. M. Irick, Vijaykrishnan Narayanan, Hankyu Moon, Rajeev Sharma and Namsoon Jung. Apparatus and method for hardware implementation of object recognition from an image stream using artificial neural network, US Patent 8081816
8. Kevin. M. Irick, Vijaykrishnan Narayanan, Hankyu Moon, Rajeev Sharma and Namsoon Jung. Apparatus and method for measuring audience data from image stream using dynamically-configurable hardware architecture. US Patent 8165386.

Filed:

1. Narayanan, V. et. al., Insect Eye: An Autonomous, adaptive and continuous insect monitoring system. U.S. Provisional Application No.: 63/187,356 filed on May 11, 2021.
2. Troncoso, N., Narayanan, V., Patent Application, "Augmented Reality Hand Guidance Application for People with Visual Impairments.", Sponsor/Agency Award number: International Patent PCT/US2021/042358. (application: January 27, 2021).

Recent Invited Talks (Sep 2018- current)

1. Narayanan, V., Accelerating Visual Analytics across the Memory and Storage Stack. U. of Moratuwa, Sri Lanka. 25 August 2023
2. Narayanan, V., Accelerating Visual Analytics across the Memory and Storage Stack. U. of Moratuwa, U. of Jaffna, Sri Lanka. 23 August 2023.
3. Narayanan, V., Advances in Ferroelectric devices for supporting data-intensive applications. University of Dhaka. 20 August 2023
4. Narayanan, V., Accelerating Visual Analytics across the Memory and Storage Stack. BUET, Bangladesh. 19 August 2023
5. Narayanan, V., Accelerating Visual Analytics across the Memory and Storage Stack. Federal University of Rio De Janeiro, Brazil. June 26, 2023.
6. Narayanan, V., Accelerating Visual Analytics across the Memory and Storage Stack. Federal University of Uruguay, Montevideo. June 20, 2023.

7. Narayanan, V., Advances in Ferroelectric devices for supporting data-intensive applications. U. Buenos Aires. June 16, 2023.
8. Narayanan, V., Accelerating Visual Analytics across the Memory and Storage Stack. University of New South Wales, Sydney, Australia, March 2023
9. Narayanan, V., Zheng, Y., CRISP-IBM talk series, IBM, Virtual, "Accelerating Visual Analytics across the Memory and Storage Stack." (December 12, 2022).
10. Narayanan, V., Mondays in Memory (MiM): an in-memory computing webinar series, TU Vienna, Virtual, "Ferroelectric-based Logic and Memory Architectures." (November 7, 2022).
11. Narayanan, V., International SoC Conference 2022 (ISOCC 2022),, IEEE, Hybrid -Korea and Virtual, "Ferroelectric-based Logic and Memory Architectures." (October 20, 2022 - Present). Keynote
12. Narayanan, V, Advances in Ferroelectric devices for supporting data-intensive applications. Europe Union InvasIC Research Center, Erlangen, Germany, Oct 7 2022. Keynote
13. Narayanan, V., IIT Madras, Chennai, India, "Ferroelectric-based Logic and Memory Architectures.." (August 19, 2022).
14. Narayanan, V., Distinguished Lecture, IIT Guwahati, Guwahati, India, "Processing-in-Memory Architectures for Deep Learning and Graph Applications.." (August 9, 2022).
15. Narayanan, V., IIT Delhi, Delhi, India, "3D Integrated Ferroelectric Logic and Memory Architectures.." (August 5, 2022).
16. Narayanan, V., University of Cyprus, Nicosia, Cyprus, "Distributed Visual Analytics: Algorithm-Architecture Interactions." (July 7, 2022 - Present).
17. Narayanan, V., IEEE Computer Society Annual Symposium on VLSI, IEEE CS, Paphos, Cyprus, ". Recent Advances in Ferroelectric-based Logic and Memory Architectures,." (July 5, 2022 - Present). Keynote
18. Narayanan, V., SRC/SIA Webinar on Collaboration towards Decadal Plan Goals: Advances and Challenges in Semiconductor, SRC/SIA, Virtual, "The Case for Intelligent Memory/Storage Hardware." (June 23, 2022).
19. Narayanan, V., Raytheon 2022 Electro-Optical Symposium, Raytheon, Virtual, "Distributed Sensing and Fusion." (June 27, 2022).
20. Narayanan, V., Technical University of Vienna, Vienna, Austria, "Distributed Visual Analytics." (June 23, 2022).
21. Narayanan, V., Technical University of Dresden, Dresden, Germany, "Ferroelectric-based Logic and Memory Architectures." (June 20, 2022).
22. Narayanan, V., Brandenburg Technical University, Cottbus, Germany, "Ferroelectric-based Logic and Memory Architectures Cottbus6/17/2022." (June 17, 2022).
23. Narayanan, V., Analog Devices, Virtual, "Distributed Sensing and Fusion." (April 4, 2022).
24. AI for Eco-Friendly Insect Traps. Center for Pollinator Research Symposium, State College, November 16, 2021.
25. Distributed Intelligence. DARPA/SRC Center for Brain Inspired Computing. October 5, 2021.
26. Implications of 3D Architecture. DoE 3DFEM Center Annual Review. October 5, 2021. Virtual
27. Advances in Distributed Video Analytics. Keynote. IEEE CAS Seasonal School, France (Hybrid mode – virtual presentation). Sept 24, 2021. IOT BORDEAUX - Home (iot-bordeaux.org)
28. Enabling New Computation Paradigms with Circuits and Architectures Using Ferroelectric FETs. Keynote. 8th International Conference on Signal Processing and Integrated Networks. 26-27 August 2021 (Virtual)

29. Advances in Distributed Visual analytics, AIoT Workshop in conjunction with KDD, 15 August 2021 (Virtual)
30. The case for device to application interactions: A ferro-electric Perspective. National Science Foundation Workshop on Future of Semiconductors: Devices to Systems for in-memory computing. Invited Talk. Virtual. May 12, 2021
31. Distributed Visual Analytics, IEEE CEDA Virtual Distinguished Lecture. Inaugural Global Virtual Lecture Series. April 22, 2021
32. Processing in Memory for AI/ML. Systems Invited Panel Speaker. 2021 NSF Workshop on Processing-In-Memory Technology, March 17-18, 2021, Virtual Workshop.
33. InsectEye. Workshop on developing systems for automated insect identification and development, Virtual.
34. Advances in Distributed Video Analytics. Distinguished Lecture. University of Louisville (Virtual) Jan 22, 2021.
35. Foundational Technology Panel, NSF Workshop on Micro/Nano Circuits and Systems Design. Invited Moderator. Virtual. Dec 14-16, 2020 https://www.src.org/library/publication/p102567/
36. Video Grand Challenge: Reshaping Video Analytics with Processing in Memory, SRC/DARPA CRISP Annual Research Review, Virtual. November 5, 2020
37. In Memory Visual Analytics. Semiconductor Research Corporation Decadal Plan Memory Workshop, Virtual. Oct 27-29, 2020; https://www.src.org/library/publication/p102566/
38. Monolithic 3D enabled Processing-in- SRAM Memory, Keynote, Virtual Conference, Design and Automation of Circuits and Systems Symposium, CSTIC 2020, 20 June 2020
39. Is it Logic or Memory? - Blurring the Gap. IEEE CEDA Distinguished Lecture. NYU, Abu Dhabi, November 2019 (~40)
40. Beyond Von Neumann Systems. IEEE CEDA Distinguished Lecture. Middle East College, Oman, November 2019 (~200 attendees)
41. Beyond Von Neumann Systems. IEEE CEDA Distinguished Lecture. Sultan Qaboos University, Oman, November 2019 (~25 attendees)
42. Exploring Monolithic-3D enabled In-Memory Compute", CRISP 2nd Annual Research Review - UVA Darden School of Business - Charlottesville, VA, November 5. 2019.
43. "In-memory Computing: The Resurgence." October 23 2019. Global Foundries and the IEEE EDS Schenectady Chapter (~300 attendees)
44. "Technology-Assisted Computing-In-Memory Design for Matrix Multiplication Workloads", Invited talk Nanoarch Conference, Qingdao, China, July 19. 2019 (~60 attendees)
45. "Monolithic 3D based Compute in Memory Architectures", Intel Labs, Bangalore, India, August 19. 2019 (~30 attendees)
46. Visual Cortex on Silicon: Helping the Visually Impaired See. Shanghai Jiao Tong University, July 2019 (~20)
47. Visual Cortex on Silicon: Helping the Visually Impaired See. Tsinghua University, July 2019 (~50)
48. Visual Cortex on Silicon. National Cheng Keung University, Tainan, March 2019 (~150)
49. Visual Cortex on Silicon. National Tsinghua University, Taiwan, March 2019 (~40)
50. Visual Cortex on Silicon. IEEE CEDA Summer School, UFRGS, Brazil, March 2019 (~100)
51. In-Memory Computing. Analog Devices, MA (~70), Feb 2019.
52. Processing in Memory Architectures, Keynote Talk, VLSI Design Conference, New Delhi, January 2019.

53. Blurring the Gap Between Memory and Logic. Invited Tutorial on Nanotechnology-Enabled Beyond-von-Neumann Computing. Army Research Laboratory, Adelphi Laboratory Center. November 14, 2018
54. Distributed Intelligence. SRC/DARPA Center for Brain Inspired Computing Annual Review, Purdue University, October 8, 2019.
55. In-Memory Computing: The Resurgence (plenary talk), IEEE System on Chip Conference, Washington DC September 4, 2018
56. Technology-Driven Emerging Computational Models and Systems (Invited Talk) SSDM 2018, Tokyo Japan. September 2018 (Virtual Talk to a Physical audience)
57. Distributed Intelligence - Applications. Intel Corporation, Portland, Oregon. September 24 2018.
58. Cognitive Vision Systems: Assisting Persons with Visual Impairments. Keynote. IEEE Workshop on Signal Processing Systems. 21-24 October 2018 — Cape Town, South Africa

Selected Plenary/Keynote (Prior to 2018)

INIS 2017, FutureChip Conference 2016, ESTIMEDIA 2016, SiPS 2015, ASQED 2015, CAD/GRAPHICS 2015, SASIMI 2015, CECNET 2014, IWLS 2014, VLSI Design 2013, ICIIS 2013, PrimeAsia 2013, FETCH 2012, Workshop on Low Power SoC (Green Computing Conference) 2011, Dhiyantra 2010, MPSoC 2008

Funded Research Projects

Current (11 projects)

- Narayanan, V. (Co-PI). Collaborative Research: FET: Medium: Compact and Energy-Efficient Compute-in-Memory Accelerator for Deep Learning Leveraging Ferroelectric Vertical NAND Memory. National Science Foundation. 10/23-09/27. $266,000.00.
- Narayanan, V. (PI). EFRI BRAID: Neuroscience Inspired Visual Analytics. National Science Foundation. 09/23-08/27. $1,999,675.00
- Narayanan, V. (Co-PI). NRT-HDR: Interdisciplinary Studies in Entomology, Computer Science and Technology NETwork (INSECT NET). National Science Foundation. 07/23-06/28. $3,000,000.00
- Narayanan, V. (PI). FAB: A Heterogeneous Ferroelectronics Platform for Accelerating Big Data Analytics. National Science Foundation. 01/23-12/24. $600,000.00
- Narayanan, V. (Co-PI). PRISM - Processing with Intelligent Storage and Memory. DARPA/SRC. 01/23-12/28. $1,375,000.00
- Narayanan. V. (PI). Spiking Neural Network Benchmarking. Chromologic Inc. 01/23-12/24.

- Trolier-McKinstry, S. (PI and Director), V. Narayanan (Co-PI, Associate Director). Additional PIs list can be found online. Center for 3D Ferroelectric Microelectronics. Department of Energy. October 2020 to August 2024 Total Award Amount (including Indirect Costs): $13,914,194
- Narayanan, V. (Co-PI) ASCENT: Ferroelectric-based Compute-in-Memory Dynamical Engine (Ferro-CoDE) to Solve Hard Combinatorial Optimization. National Science Foundation. October 2021 to Sept 2025. Total Award Amount (including Indirect Costs): $398,328 (Penn State share of Collaborative project with University of Virginia)
- Narayanan, V. (Principal Investigator), FET: Small: Leveraging Monolithic 3D for Architectural Innovations" National Science Foundation. Start Date:08/01/2020; Award Amount: $500,000.00;
- Das, C. (Principal Investigator), V. Narayanan (Co-PI), A. Sengupta (Co-PI). National Science Foundation. SHF: Medium: A Technology-Architecture-Algorithm Co-Design Exploration of Scalable Spiking Neural Networks (SNNs) Start Date:08/01/2020; Award Amount: $999,000.00;
- Sampson, J. (Principal Investigator), V. Narayanan (Co-PI), M. Kandemir (Co-PI). National Science Foundation. SPX: SOPHIA: Support for Opportunistic Parallelism with Heterogeneous Intermittently-powered Accelerators Start Date:10/01/2018; Award Amount:$900,000.00;

Completed

- Tirupatikumara, Soundar R. (Principal Investigator). Kandemir, Mahmut T. (Co-Principal Investigator), Narayanan, Vijaykrishnan (Co-Principal Investigator), Sampson, John (Co-Principal Investigator), Yang, Hui (Co-Principal Investigator). DoE Self-Powered Sensing and Data Science for Smart Manufacturing. Start Date: 11/01/2020 End Date 03/30/2023. Award Amount: $542,491
- Narayanan, V. (Principal Investigator), Anand Sivasubramaniam (Co-PI) In Memory Computing. Joint University Microelectronics Program, DARPA SRC. Subaward from U. Virginia. $3,562,090 (includes $1,237,090 Match). January 2018-June 2023.
- Narayanan, V. (Principal Investigator), John Sustersic (Co-PI) Distributed Neuromorphic Systems. Joint University Microelectronics Program, DARPA SRC. Subaward from Purdue University. $1,823,061 (includes $501,000 match). January 2018-Sep 2023.
- Narayanan, V. (Principal Investigator), "Collaborative Research: Visual Cortex on Silicon," National Science Foundation, Federal Agencies. Total awarded: $9,700,000.00 (Penn State Share $4,913,456.00) (funded: October 1, 2013 - September 30, 2021).
- Narayanan, V. (Principal Investigator), Contract, " E2CDA: Type I: Extremely Energy Efficient Collective Electronics (EXCEL)," University of Notre Dame, Prime Sponsor (Nanoelectronics Research Center). Total requested: $354,343 (1 July 2016- 30 June 2019). Total awarded: $116,000. (Date funding awarded: March 2017, funded: October 1, 2016 - September 30, 2017.
- Narayanan, V. (Principal Investigator), Contract, "Center for low energy systems technology (LEAST)," University of Notre Dame, Universities and Colleges. Prime Sponsor DARPA/SRC Total requested: $3,974,604.00. Total awarded: $3,974,604.00. (submitted: October 23, 2012, date funding awarded: March 25, 2013, funded: January 1, 2013 - December 31, 2017).
- Narayanan, V. (Principal Investigator), Contract, "Co-Design of Cognitive Vision Algorithms on FPGA," Naval Sea Systems Command, Federal Agencies. Total awarded: $148,213.00. (funded: November 15, 2015 - December 31, 2016).
- Narayanan, V. (Principal Investigator), Contract, "Intel Siskiyou Peak Program," Intel Corp., Corporations. Total awarded: $55,721.00. (date funding awarded: February 13, 2013, funded: December 1, 2012 - December 31, 2014).

- Narayanan, V. (Principal Investigator), Datta, S. (Co-Principal Investigator), Contract, "A Hybrid Reconfigurable Logic Architecture Using Classical & Non-Classical Multi Gate Quantum Well FETs (MuQFETs)," National Security Agency, Federal Agencies. Total requested: $663,886.00. Total awarded: $628,201.00. (submitted: June 27, 2012, date funding awarded: March 20, 2013, funded: August 1, 2012 - July 31, 2014).
- Datta, S. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Mayer, T. S. (Co-Principal Investigator), Contract, "Midwest Institute for Nanoelectronics Discovery Project 1.5 (MIND 1.5)," Notre Dame, University of, Universities and Colleges. $560,000.00. (submitted: December 21, 2010, funded: April 1, 2008 - December 31, 2011).
- Narayanan, V. (Principal Investigator), Contract, "NeoVision2 (Previous Award No. 000176-DS)," HRL Laboratories, LLC, Corporations. $279,826.00 (funded: May 19, 2010 - September 19, 2011).
- Narayanan, V. (Principal Investigator), Contract, "NeoVision Teledyne," Teledyne Scientific & Imaging, LLC, Corporations. $707,803 (submitted: June 30, 2009, funded: May 21, 2010 - September 12, 2011).
- Narayanan, V. (Principal Investigator), Contract, "USC subcontract: Neuromorphic visual systems for intelligent unmanned sensors," University of Southern California, Universities and Colleges. $477,641.00. (submitted: June 30, 2009, funded: November 1, 2009 - March 1, 2011).
- Narayanan, V. (Principal Investigator), Datta, S. (Co-Principal Investigator), Contract, "Architecture-Device Co-Design for Ultra-Low Power Systems," National Security Agency, Federal Agencies. $606,764.00. (submitted: June 9, 2008, funded: September 8, 2009 - December 31, 2010).
- Narayanan, V. (Principal Investigator), Xie, Y. (Co-Principal Investigator), Contract, "Inductively-Powered Self-Recharging Battery System," Harris RF Communications Division, Corporations. $38,000.00. (funded: January 1, 2010 - June 30, 2010). Narayanan, V. (Principal Investigator), Irwin, M. J. (Co-Principal Investigator), Contract, "System on Chip Curriculum Enhancement," The Technology Collaborative, Associations, Institutes, Societies and Voluntary Health Agencies. $50,000.00. (submitted: December 4, 2007, funded: September 1, 2007 - May 31, 2010).
- Narayanan, V. (Principal Investigator), Kandemir, M. T. (Principal Investigator), Contract, "FANTOM-II: Algorithm-Architecture Codesign for High-Performance Application-on Chips in SAR Systems," Duke University, Universities and Colleges. Total requested: $557,333.00. (May 3, 2005 - February 29, 2008).
- Narayanan, V. (Senior Personnel), Grant, "NSF Nanosystems Engineering Research Center (ERC) on Advanced Self-Powered Systems of Integrated Sensor Technologies (ASSIST)," North Carolina State University, Universities and Colleges. $3,833,798.00. (September 1, 2012 - August 31 2017.)
- Narayanan, V. (Principal Investigator), Sampson, J. (Co-Principal Investigator), Grant, "A Configurable Vision Platform for Cognitive Image Analytics," Intel Corporation, Corporations. $90,000.00. (submitted: August 20, 2015, date funding awarded: September 15, 2016, funded: September 1, 2016 - August 31, 2017)
- Narayanan, V. (Principal Investigator), Sampson, J. (Co-Principal Investigator), Grant, "A Configurable Vision Platform for Cognitive Image Analytics," Intel Corporation, Corporations. $90,000.00. (submitted: August 20, 2015, date funding awarded: September 15, 2015, funded: September 1, 2015 - August 31, 2016).

- Narayanan, V. (Co-Principal Investigator), Grant, "SHF:LARGE: Collaborative Research: Architecting Next generation Memory Hierarchy: A Holistic Approach," National Science Foundation, Federal Agencies. $1,360,000.00. (submitted: April 10, 2012, date funding awarded: June 6, 2012, funded: August 1, 2012 - July 31, 2016).
- Narayanan, V. (Principal Investigator), Grant, "STTR: Visible EO System and LIDAR Fusion for Low-Cost Perception by Autonomous Ground Vehicles: Phase II Option II SAF-T Program Support," Toyon Research Corporation/Office of Naval Research, Federal Agencies. $60,000.00. (submitted: May 27, 2015, date funding awarded: September 18, 2015, funded: July 6, 2015 - June 23, 2016).
- Narayanan, V. (Co-Principal Investigator), Grant, "II-NEW: INSpiRE: Infrastructure for HeterogeNeous System Research," National Science Foundation, Federal Agencies. $550,000.00. (submitted: July 31, 2012, date funding awarded: September 27, 2012, funded: October 1, 2012 - September 30, 2015).
- Narayanan, V. (Principal Investigator), Grant, "Hierarchical Object Recognition Pipeline with Diversified Classification Abilities," Intel Corp., Corporations. $80,000.00. (funded: January 1, 2014 - December 31, 2014).
- Narayanan, V. (Principal Investigator), Grant, "Intel Science and Technology Center in Embedded Computing: Disruptive Advances in Algorithms and Systems to Transform Connected Embedded Computing," Intel Corp., Corporations. $42,000.00. (funded: January 1, 2014 - December 31, 2014).
- Datta, S. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Grant, "Collaborative: Mixed Anion and Cation Based Transistor Architecture for Ultra-Low Power Complementary Logic Applications," National Science Foundation, Federal Agencies. $241,102.00. (submitted: February 9, 2010, funded: October 1, 2010 - September 30, 2014).
- Narayanan, V. (Principal Investigator), Grant, "Smart Cameras," Intel Science and Technology Center, Corporations. Total awarded: $252,000.00. (funded: August 1, 2011 - July 31, 2014).
- Narayanan, V. (Principal Investigator), Grant, "A Visual Saliency-based Classifier for Autonomous Target Classification for Remote Identification (VISCATI)," Office of Naval Research, Federal Agencies. $85,000.00. (funded: May 14, 2013 - May 13, 2014).
- Xie, Y. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Grant, "ADAMS: Architecture and Design Automation for 3D Multi-core Systems," National Science Foundation, Federal Agencies. $480,000.00. (submitted: May 12, 2009, funded: August 1, 2009 - April 30, 2014).
- Xie, Y. (Principal Investigator), Narayanan, V. (Principal Investigator), Contract, "ADAMS: Architecture and Desing Automation for 3DMulti-core Systems SRC: Semiconductor Research Corporation," Semiconductor Research Corporation, Corporations. $120,000.00. (submitted: May 26, 2009, funded: August 1, 2009 - April 30, 2014).
- Narayanan, V. (Principal Investigator), Grant, "Collaborative Research: Planning Grant: I/UCRC for Nexys: Next Generation Electronic System Design," National Science Foundation, Federal Agencies. $11,500.00. (submitted: September 26, 2011, date funding awarded: April 13, 2012, funded: April 15, 2012 - September 30, 2013).
- Das, C. (Principal Investigator), Kandemir, M. T. (Co-Principal Investigator), Narayanan, V. (Co-Principal Investigator), Xie, Y. (Co-Principal Investigator), Grant, "NSF: EAGER: SHF: Harnessing Cross-Layer Heterogeneity for future CMPs," National Science Foundation, Federal Agencies. $300,000.00. (submitted: July 13, 2011, funded: September 1, 2011 - August 31, 2013).
- Narayanan, V. (Principal Investigator), Grant, "Intel Science and Technology Center in Embedded Computing:," Intel Corp., Corporations. $42,000.00. (date funding awarded: February 28, 2012, funded: January 17, 2012 - January 16, 2013).

- Narayanan, V. (Principal Investigator), Datta, S. (Co-Principal Investigator), Grant, "EMT/NANO: Co-Exploration of Device and System Architecture for Quantum NanoElectronics," National Science Foundation, Federal Agencies. $200,020.00. (submitted: July 7, 2008, funded: September 1, 2008 - August 31, 2012).
- Narayanan, V. (Principal Investigator), Xie, Y. (Co-Principal Investigator), Grant, "HoDoo: Holistic Design of On-Chip Interconnects," National Science Foundation, Federal Agencies. $630,894.00. (submitted: April 20, 2007, funded: July 1, 2007 - June 30, 2012).
- Narayanan, V. (Principal Investigator), Acharya, R. (Co-Principal Investigator), Irwin, M. J. (Co-Principal Investigator), Albert, R. (Co-Principal Investigator), Lesk, A. M. (Co-Principal Investigator), Reason, R. D. (Co-Principal Investigator), Grant, "CPATH: CDO: Integrating Biology and Computing: Empowering Future Computer Professionals," National Science Foundation, Federal Agencies. $149,028.00. (submitted: March 11, 2008, funded: September 1, 2008 - August 31, 2011).
- Narayanan, V. (Principal Investigator), Xie, Y. (Co-Principal Investigator), Grant, "TC: Small: Improving Lifetime Reliability for Reconfigurable Embedded Systems," National Science Foundation, Federal Agencies. $400,000.00. (submitted: February 1, 2009, funded: September 1, 2009 - August 31, 2010).
- Narayanan, V. (Principal Investigator), Unlu, K. (Co-Principal Investigator), Irwin, M. J. (Co-Principal Investigator), Xie, Y. (Co-Principal Investigator), Grant, "CRI: SEAT: Soft Error Analysis Toolset," National Science Foundation, Federal Agencies. $449,997.00. (submitted: September 23, 2004, funded: September 15, 2005 - August 31, 2007).
- Irwin, M. J. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Kandemir, M. T. (Co-Principal Investigator), Contract, "Collaborative Research in the Design, Verification, and Test of Integrated Gigascale System: The Gigascale Systems Research Center," University of California at Berkeley, Universities and Colleges. $600,000.00. (September 1, 2003 - December 31, 2006).
- Narayanan, V. (Principal Investigator), Kandemir, M. T. (Co-Principal Investigator), Xie, Y. (Co-Principal Investigator), Grant, "Transaction Level Power Modeling Methodology (Note: Includes $76,000 in Cost Sharing from IBM)," The Technology Collaborative, Associations, Institutes, Societies and Voluntary Health Agencies. $225,903.00. (funded: August 1, 2004 - December 31, 2005).
- Narayanan, V. (Principal Investigator), Grant, "Exploring Network-on-Chip (NoC) Architecture Design Space," National Science Foundation, Federal Agencies. $190,000.00. (submitted: March 17, 2004, funded: September 15, 2004 - August 31, 2005).
- Narayanan, V. (Principal Investigator), Kandemir, M. T. (Co-Principal Investigator), Contract, "Fantom: Algorithm-Architecture Co-design for High Performance Signal and Image Processing," Duke University, Universities and Colleges. Total requested: $234,957.00. (submitted: March 4, 2005, funded: May 3, 2005 - September 30, 2006).
- Narayanan, V. (Principal Investigator), Contract, "Embedded Hardware Face Detection and Classification," Video Mining Corporation^, Corporations. $36,659.00. (funded: January 1, 2005 - December 31, 2005).
- Irwin, M. J. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Kandemir, M. T. (Co-Principal Investigator), Contract, "Energy-Efficient On-Chip Communication and Storage for Multiprocessor SoCS," Semiconductor Research Corporation, Corporations. Total requested: $312,959.00. (April 1, 2004 - March 31, 2005).
- Irwin, M. J. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Das, C. (Co-Principal Investigator), Contract, "SoC Curriculum Faculty Start-Up Package Proposal," The Technology Collaborative, Associations, Institutes, Societies and Voluntary Health Agencies. $300,000.00. (funded: August 15, 2001 - June 30, 2005).

- Sivasubramaniam, A. (Principal Investigator), Irwin, M. J. (Co-Principal Investigator), Kandemir, M. (Co-Principal Investigator), Narayanan, V. (Co-Principal Investigator). NGS: POWERful Software for Power Constrained Systems. Start Date:09/15/2001; Award Amount: $600,667.00.
- Sivasubramaniam, A. (Principal Investigator), Irwin, M. J. (Co-Principal Investigator), Kandemir, M. (Co-Principal Investigator), Narayanan, V. (Co-Principal Investigator). CISE Research Resources: From High Performance to Low Power: Infrastructure for Ubiquitous Computing. Start Date: 03/15/2002; Award Amount: $49,556.00.
- Narayanan, V. (Principal Investigator). CAREER: Energy-Efficient Architectures and Their Interaction with Software: A Java Perspective. National Science Foundation. Start Date:08/15/2001; Award Amount: $268,642.00.
- Irwin, M. J. (Principal Investigator), Narayanan, V. (Co-Principal Investigator), Chandramouli, R. (Co-Principal Investigator), ITR: Collaborative Research: Optimization and Integrated Control of Low Power Wireless Multimedia Networks. National Science Foundation. Start Date:09/01/2000; Award Amount: $498,565.00
- Narayanan, V. (Principal Investigator). Designing Efficient Java Runtime Systems. National Science Foundation. Start Date:09/01/2000; Award Amount: $110,626.00.
- Narayanan, V. (Principal Investigator). Java Virtual Machines. Sun Microsystem. Start Date: 01/01/199. Award Amount: $35,000.00

Students Advised

Summary: Students have won prestigious fellowships during their course of graduate study under Narayanan including IBM fellowship, Alfred Sloan Fellowship, GEM Scholarship and CAC Fellowship. Two of his advisees won the Best Dissertation Award, a global recognition given by the European Design Automation Association. His former students have been successful in academia, entrepreneurship and industry (examples – Tenured Associate Professor (KAIST, Korea;), Principal Engineers (Samsung) and successful entrepreneurs (EDAplayground). He has been a major driver for diversity with multiple African-American and women students that he has mentored. His students won the 2016 IEEE Computer Society Global Student Competition for their entry on 'Computer Vision for assisting Visually Impaired".

GRADUATE STUDENT SUPERVISION

Total Number of Students Supervised: 54 Ph.D. and 13 current, 72 Masters students and 2 current.

Summary: Students have won prestigious fellowships during their course of graduate study under Narayanan including IBM fellowship, Alfred Sloan Fellowship, GEM Scholarship and CAC Fellowship. One of his advisees won the Best Dissertation Award, a global recognition given by the European Design Automation Association. His former students have been successful in academia, entrepreneurship and industry (examples – Tenured Faculty (KAIST, Korea;), Principal Engineers (Samsung) and successful entrepreneurs (Gnoll Technologies). He has been a major driver for diversity with multiple African-American and women students that he has mentored.

SECTION I: PH.D. STUDENTS:

1. Zeinab Hakimi, Efficient Deep Neural Networks Architecture for Video Analytics Systems. Dissertation Advisor (2019-2023). Engineer at Lowes.
2. Sonali Singh. Spiking Neural Network Architectures. Dissertation Co-Advisor (2017-2023) (With Chita Das). Engineer at AMD.
3. Akshay Ramanathan. 2022. Stacked-3D and Processing-in-memory Solutions for Data-intensive and Persistent Applications. Engineer at MediaTek.
4. Eric Homan. 2022. Context-Aware Perception for Edge and Embedded Devices. Engineer at Raytheon BBN,
5. Nagadastagiri Reddy. 2022. Design of processing-in-memory architectures for deep learning and graph. Engineer at nVidia.
6. Peter Zientra, 2021, Design of a vision-based assistive system for visually impaired persons. Ph.D. Dissertation Co-Advisor. (Co-advised with Sampson). Presented demonstrations of his research prototypes at the US Senate and featured on Big Ten Television. - Google
7. Nicolaus Jao, 2021, Non-volatile memory design based on crossbar architecture towards low power systems and processing in-memory - Dissertation Advisor (2016-present) - AMD
8. Sumitha George, 2020. Technology Driven Architecture Support for Memory Hierarchies – Assistant Professor, North Dakota State University
9. Srivatsa Rangachar. 2020. In-Memory Logic using Monolithic 3D. (Co-advised with Swaroop Ghosh – Intel Corporation
10. Jinhang Choi. 2019. Context-Aware Design and Optimization of Embedded Deep Neural Network Architectures (Co-advised with Sampson) – Microsoft Corporation.
11. Kaisheng Ma, 2018 "Nonvolatile Processor" Ph.D. Dissertation Co-Advisor. (Co-advised with Sampson). Winner of EDAA Outstanding Dissertation Award and the China Overseas Talent and Innovation Entrepreneur based on innovation resulting from Ph.D. Research and co-founded PI2Star. Assistant Professor in Tsinghua University.
12. Wei-Yu Tsai, 2017 "Enabling New Computation Paradigms with Emerging Technologies (Co-advised with Sampson) – Meta.
13. Advani, Siddharth, 2016. Large-scale object recognition for embedded wearable platforms (Co-advised with Jack Sampson) – Senior Hardware Engineer at Samsung Research America. Developing key hardware technology for next generation Samsung Mobile products. In the past one year at Samsung, work has led to an invention disclosure which is currently under review. Winner of 2013 Richard Newton Young Fellowship Program.
14. Chandramoorthy, Nandhini. 2016. Design and Exploration of Accelerator-rich Multi-core Systems – Research Staff Member, IBM Watson Research Labs. Her work, funded by the DARPA PERFECT program, consists of examining techniques for reliable operation at very low voltages and designing a chip to establish proof of concept. She is also involved in developing pre-RTL optimization tools for modeling power, performance and reliability to aid IBM product transitions.
15. Kim, Moon Seok. 2016 Digital/mixed-signal circuit designs with steep slope III-V tunnel transistors – Intel Corporation
16. Lee, Chris. 2016. Data dependent optimization vision architecture – Game Software Designer.
17. Cotter, Matthew Joseph. 2015. Enabling intelligent vision systems in a configurable multi-algorithm pipeline – Research Engineer, Applied Research Labs, Penn State.

18. Liu, Huichu. 2015 Device Circuit Interactions for Steep Switching Slope Devices (Co-advised with Suman Datta) Senior Research Scientist, Facebook
    Huichu Liu has been leading researcher in novel technology and process integration with future computer microarchitecture at Intel labs. She has filed over 10 patents at Intel labs on novel logic and memory technologies. Winner of Design Automation Conference under 40 innovators award.
19. Xiao, Yang. 2014. Using attention to enhance efficiency in video-based computer systems. Senior R&D Engineer, Synopsys Inc. Contributed to physical placer development and optimization for the new generation of Design Compiler, the industry leading tool for logic synthesis.
20. Xu, Cong. 2014. Modeling, circuit design, and microarchitectural optimization of emerging resistive memory (Co-advised with Yuan Xie) Research Engineer at Hewlett Packard Labs. Acceleration of deep learning workloads on Moonshot servers with integrated GPUs
21. Swaminathan, Karthik. 2014. An examination of post-CMOS computing techniques using steep slope device-based architectures. Research Staff Member, IBM T.J Watson Research Center at Yorktown Heights, NY. His work is focused on resilience-aware designs for very low voltage operation of processors. In addition to publication at top conferences, his work has resulted in several patents as well as in key contributions to government project deliverables and IBM server and mainframe systems. Winner of IBM PhD Fellowship Award when at Penn State.
22. Park, Mi Sun. 2014. Configurable accelerators for visual and text analytics (co-advised with Prof. Mary Jane Irwin). Machine Learning Engineer, Intel, Santa Clara.
23. Park, Sungho 2013. System-on-Chip integration of heterogeneous accelerators for perceptual computing. Hardware Design Engineer, Intel, Folsom. Contributed to enhanced cache design for Intel core
24. Eze, Melvin. 2013. Sub-50 nm multi-segment interconnect design: A treatise on speed, reliability and signal integrity. Independent Consultant. Winner of Paul H. Schweitzer Memorial Graduate Fellowship and Bunton-Waller Fellowship during graduate study.
25. Maashri, Ahmed Al. 2012. Accelerating design and implementation of embedded vision systems. Assistant Professor at Sultan Qaboos University, Oman (premiere university in Oman). Appointed as a member of the National Committee for Approving Programs for all universities in Oman. Founder and Chair of the IEEE Computer Society in Oman.
26. Cho, Yong Cheol Peter. 2012. Accelerating Cortical Processing for Real Time Neuromorphic Vision Systems. Senior Researcher at Electronics and Telecommunications Research Institute (ETRI), Taiwan. Involved with design of neuromorphic hardware accelerators and embedded systems.

27. Kestur Vyasa Prasanna, Srinidhi. 2012. Domain-specific accelerators on reconfigurable platforms (Co-advised Suman Datta). Sr Hardware Engineer in the Technical Infrastructure group at Google, where he drives efforts to navigate the end of Moore's law by contributing to custom Chip development activities for the Google Datacenter. Before joining Google in 2016, Dr Kestur was a Principal Engineer at Broadcom Ltd where he led the Emulation and FPGA prototyping efforts of an ARM-based server-class Processor SoC. Prior to that he worked at Intel Labs as a Research Scientist and contributed to the design and verification of the CPU subsystem in the SoFIA smartphone SoC. Notable awards include Broadcom President's award in 2017 which is offered to select few employees throughout the company for outstanding contributions to the company.
28. DeBole, Michael. 2011. Configurable accelerators for video analytics (Co-advised with Yuan Xie) Research Staff Member at IBM Almaden Research Center. IBM Corporate Award for Development of Cryptographic Hardware Module for System Z Mainframe (used by 96% of the banks around the world). Recipient of Misha Mahowald prize for Neuromorphic Engineering (TrueNorth), one of the first commercial neuromorphic chips in the world.
29. Saripalli, Vinay. 2011 Device and architecture co-design for ultra-low power logic using emerging tunneling-based devices (Co-advised with Suman Datta). Staff Software Engineer, Intel, Santa Clara. Develops RTL2GDS methodologies intended to reduce the impact of parasitic on timing convergence of SoC blocks.
30. Mangalagiri, Prasanth. 2010. A reliable design flow for platform FPGAs (Co-advised with Yuan Xie). Senior Staff Software Engineer, Intel, Santa Clara. He is a member of Product Development Solutions, which is a Research & Development group that develops innovative solutions and standards that span and connect Intel’s Product Life Cycle. He serves as a strategic planner and technical lead for Analog Memory Solutions, where he is involved in end-to-end activities of Tools, Flows, and Methodologies development and deployment, with an emphasis on significantly reducing Analog Circuit and Physical Design Turn-Around-time. Analog design migration capabilities developed under Dr. Mangalagiri's technical leadership, were deployed in high-speed IO IPs in Intel SOCs and the original contributions of his research were recognized as "Best of Published" in Intel DTTC-2017 conference. He has also won three internal Intel Awards for outstanding work.
31. Ricketts, Andrew Jonathan Sylvester. 2010. Towards minimizing the adverse effects of temperature on high performance digital systems. Graphics Hardware Engineer at Intel, Folsom, CA. Responsible for the RTL verification and development for various codecs including the encode and decode of HEVC and VP9
32. Eachempati, Soumya S.. 2010. Influence of emerging technologies on interconnect architectures (Co-advised with Suman Datta). Component Design Engineer, Intel, Santa Clara. Performance Architect for server platforms.
33. Yanamandra, Aditya. 2010. Exploring power reliability tradeoffs in on-chip networks (Co-advised with Mary Jane Irwin). Principal Engineer, Intel, Santa Clara.

34. Krishnan, Ramakrishnan. 2010. Analysis of failures in nanoscale devices (Co-advised with Suman Datta). Section Manager at TSMC Taiwan. (largest foundry in the world). Test Chip Design and Development Division. In charge of test-chip design team for TSMC internal test-chips and customer test chips. Owns 4 patents.
35. Bae, Sungmin. 2010. Closing the gap between FPGA and ASICS: The applications of clock skew scheduling on FPGAs. CAD Software Engineer at Intel Santa Clara.
36. Soundararajan, Niranjan. 2010. Addressing reliability issues in performance-critical processor structures (Co-advised with Anand Sivasubramaniam). Research Scientist at Intel Technologies India. The work involves anticipating architectural and application trends several years ahead and extending this best-in-class architecture accordingly. Five Intel patents at different stages of filing on improving core performance and SoCs
37. Irick, Kevin Maurice. 2009. A configurable platform for sensor and image processing. Founder SiliconScapes, LLC. Siliconscapes produces custom accelerators for Defense and Commercial applications. Siliconscapes emerged from a Ben Franklin TechCelerator @State College award to transition research to commercial products.
38. Kim, Jung Sub. 2008. High-performance signal processing on reconfigurable platforms. Principal Engineer, Samsung, Korea. Research and Development of next generation television systems.
39. Nicopoulos, Chrysostomos A. 2007. Network-on-Chip architectures: A holistic design exploration (Co-advised with Ken Jenkins). Assistant Professor, Department of ECE, University of Cyprus. His Ph.D. dissertation received the prestigious Outstanding Dissertation Award in the area of “New directions in logic and system design” in 2008-09 by the European Design and Automation Association (EDAA). Most recently, he won a Best Paper Award at the DATE-2015 conference, Europe’s premiere and biggest electronic system design & test conference.
40. Pirretti, Matthew G.. 2007. Secure communications in sensor networks. Software Engineer at Intel Corporation, Phoenix. Have designed, developed, and evaluated highly complex cryptosystems, including eventual release into multiple products. Served as secure boot architect for Intel's 2014 tablet product.
41. Ramanarayanan, Rajaraman. 2007. Soft errors in logic circuits: Analysis and modeling. Component Design Engineer, Intel, Bangalore.
42. Lin, Ing-Chao. 2007. System level power and reliability modeling. Associate professor in Department of Computer Science and Information Engineering, National Cheng Kung University, Taiwan. Recipient of Excellent Young Electric Engineer award by Chinese institute of Electric Engineering Society in 2015 and the recipient of Best Graduate in Last Decade (GOLD) award by IEEE Tainan Section. IEEE Senor Member and ACM Senior Member.

43. Srinivasan, Suresh. 2007. Tackling power and reliability issues in field programmable gate arrays. Founded Gnoll Technologies Pvt. Ltd., a company excelling in the most advanced IOT solutions. an entrepreneur (Gnoll Technologies Pvt. Ltd.) and Senior Vice President of a joint venture of his company with a multi-million dollar firm (yet to be public) developing hardware and software integrated IOT solutions catering to numerous industries. In the past, lead the performance and power analysis team of ARM, the front face to all ARM IP going out to partners for 4 years and before that worked with Intel Labs and Design teams for 5 years, on their future products. He owns the patent for the current world's best circuit for True Random Number Generator (digital) and the fastest Floating-Point MAC Algorithm, both implemented in Intel's main core
44. Gayasen, Aman. 2006. Implications of future technologies on the design of FPGAs (Co-advised with Mahmut Kandemir) Senior Software Engineer, Xilinx, Hyderabad. Developed Vivado physical synthesis, a leading FPGA design tool in industry, from the ground up. Architected the solution. Developed incremental placement algorithm and timing optimizations.
45. Theocharides, Theocharis. 2006. Embedded hardware face detection for digital surveillance systems. Associate Professor, Department of Electrical and Computer Engineering, University of Cyprus. Director of Research, KIOS Research and Innovation Center of Excellence, University of Cyprus. Approximately 80+ peer-reviewed publications in Journals, Conferences and Book Chapters, significant funding (excess of 750,000 as PI, excess of 40 million as Co-PI. Supervised 3 Ph.D. students to graduation, supervising 5 more currently.
46. Lee, Jooheung. 2006. Efficient VLSI architectures for image and video signal processing algorithms (Co-advised with Ken Jenkins). Associate Professor, Department of Electronic and Electrical Engineering, Sejong Campus, Hongik University, South Korea.
47. Link, Gregory M. 2006. Temperature -aware computing. Manager, Embedded Software, Magic Leap. Defining and implementing Linux kernel module interfaces. High performance embedded framework design and implementation, including hard timing constraints. Internal team support.
48. Saputra, Hendra. 2005. Security issues in embedded system design (Co-advised with Mahmut Kandemir). Research Staff, Agency for Science, Technology and Research (A*STAR), Singapore. Working on developing secure embedded systems software.
49. Degalahal, Vijay S. R. 2005. Soft errors: Modeling and interactions with power optimizations. Principal Engineer, Intel. Served SOC and Power Architect for Intel's mainstream Client microprocessors. For the past 12 years, Vijay has been responsible in making several generations of Intel CoreTM products to have lower power and longer battery life.
50. Li, Lin. 2005. Designing energy-efficient and reliable caches and interconnects (Co-advised with Mary Jane Irwin). Staff Engineer, Qualcomm, North Carolina. Processor and system performance modeling and analysis.
51. Tsai, Yuh-Fang. 2005. Tools and techniques for leakage power analysis (Co-advised with Mary Jane Irwin). Failure Analysis Manager, Microsemi Corporation, Taiwan. She set up and hired all the people in Microsemi, Taiwan Hsinchu office. Winner of the ASPDAC retrospective most influential paper in 2013 for her dissertation work on leakage modeling.

52. Hu, Jie. 2004. Orchestrating the compiler and microarchitecture for reducing cache energy. DataCenter Power Management Technologist, Intel, Santa Clara. 40+ publications and one patent. Sets the enabling strategy for power management at silicon & platform levels. Provides leadership role in the resolution of major customer power management issues & requirements.
53. Kim, Soontae. 2003. Energy-efficient high performance cache architectures. Associate Professor at KAIST, premier institution in Korea. Winner of multiple best paper awards and the 2015 KAIST 10 best research accomplishment for work on small Drone-detecting RADAR. His students are faculty members in Pakistan and Bangladesh and at IBM Watson Research Center in USA.
54. Kim, Hyun Suk. 2003. Energy -aware hardware and software optimizations for embedded systems (Co-advised with Mary Jane Irwin). Senior Engineer, Samsung Electronics, Korea.

Current Ph.D. Advisees

1. Faysal Khan. Embedded Machine Learning Architectures. Dissertation Advisor (2018-present)
2. Chonghan Lee. Contextual Machine Inference. Dissertation Advisor (2019-present)
3. Yixin Xu, Technology Implications on Computer Architecture, Dissertation Advisor (2020-present)
4. Zheyu Li, Processing-in-memory architectures for video analytics. Dissertation Advisor (2020-present)
5. Yi Xiao. Ferroelectric device-based circuit design. Dissertation Advisor (2021-present)
6. Anusha Devulapally, Sensor fusion. Dissertation Advisor (2021 - Present).
7. Pingyi Huo, Disaggregated processing-in-memory architectures. Dissertation Advisor (2021 - Present).
8. Sadia Tumpa, Spiking neural networks. Dissertation Advisor (2021 - Present).
9. Tianyi Shen, Self-Powered IoT architectures. Dissertation Advisor (2021 - Present).
10. Varun Parekh, SNN Architectures. Dissertation Advisor (2022 - Present).
11. Rishika Kushwah, AI Accelerators. Dissertation Advisor (2023 - Present).
12. Sadik Yasir. Ferroelectric-based Circuits and Systems. Dissertation Advisor (2023 - Present)
13. Philip Shen. InsectNet IoT System. Dissertation Advisor (2023 – Present).

SECTION II: M.S. STUDENTS:

14. Anupama Murthy, MS/CSE, Memory System Characterization of Java Applications, May 2000. First job after graduation: Software Designer at HP
15. Rajendra Athavale, MS/CSE, Annotation Based Energy Optimization for Java, December 2000. Enterprise Architect, Dell. Directs the technology strategy for Dell Inventory and Digital Fulfillment.
16. Tendai P. Chinoda, MS/CSE, Protecting Java Applications Against Decompilation via Control Flow Obfuscation, December 2000. Vice-President, Enterprise Architect, PNC, Pittsburgh.
17. Samarjeet Tomar, MS/CSE, Characterizing and Optimizing Memory Energy in Java, May 2001. Director of Software Development, Oracle, Bangalore.
18. Jeyran Hezavei, MS/CSE, Power Modeling and Optimization of Memories and Functional Units, May 2001 (co-advised with Dr. Irwin). Co-Founder, CEO at AVAtronics, Switzerland.
19. Gandhi Thirugnanam, MS/CSE, Low Power Content Addressable Memory Design, May 2001. Primary Patent Examiner, USPTO.
20. David Charles, MS/CSE, Improving ILP with Instruction Reuse Cache Hierarchy, May 2001 (Co-advised with Dr. Hurson)

21. Jun Zhao, MS/CSE, Influence of MPEG-4 Parameters on System Energy, August 2001 (at Synopsys, CA). R&D Manager at Synopsys.
22. Preeti Garg, MEng/CSE, Implementation of a Java Accelerator: Interfacing the Java Virtual Machine with the FPGA, August 2001. Senior Application Engineer, Accenture.
23. Nandagopal Kirubanandan, MS/CSE, Memory Energy Characterization and Optimization of SPEC2000 Benchmarks, December 2001 (co-advised with Dr. Sivasubramaniam). Principal Software Engineering Lead at Microsoft
24. Geethanjali Esakkimuthu, MS/CSE, Memory Energy: Modeling and Optimizations, December 2001 (co-advised with Dr. Irwin). Ph.D. student at Penn State after multiple years in industry.
25. Balaji Viswanathan, MS/CSE, OS Paging Issues for DRAM Energy Management, December 2001 (Co-advised with Dr. Sivasubramaniam)
26. Hendra Saputra, MS/CSE, Compiler-directed Voltage Scaling for Reducing Energy, December 2001 (co-advised with Dr. Kandemir). Continued for Ph.D.
27. Xiheng Xu, MS/CSE, Evaluating Energy-Efficiency of Channel Coders, May 2002 (co-advised with Dr. Irwin).
28. Yuh-Fang Tsai, MS/CSE, Characterization and Modeling for Run-time Leakage Reduction Techniques, December 2002 (co-advised with Dr. Irwin). Continued for Ph.D.
29. Nachiket Shikhare, MS/CSE, Leakage Power Estimation Tool for CMOS Circuits, May 2003 (co-advised with Dr. Irwin). Program Manager at Cypress Semiconductor.
30. Ananth Hegde Ankadi, MS/CSE, Variable Line Sized Cached DRAM, August 2003. VP, Architecture at J.P. Morgan, New York.
31. Grace Eberhardt, MEng/CSE, Analyzing the Common Language Runtime, August 2003 (co-advised with Dr. Saraswat)
32. Christopher Oster, MS/CSE, A Workload Characterization and Performance Analysis of Multiprocessor Immersive Display Environments, December 2003. Principal Systems Architect at Lockheed Martin Space Systems Company
33. Eric Swankoski, MS/CSE, Encryption and Security in SRAM FPGAs, May 2004. Senior Principal Systems Engineer / Software Development Lead at General Dynamics Information Technology
34. Swapna Dontharaju, MS/CSE, Soft error analysis of CAMs, August 2004. Test R&D Engineer at Intel Corporation, Oregon.
35. Kiyoung Lee, MS/CSE, Leakage control mechanism for FPGAs, August 2004
36. Kevin Irick, MS/CSE, Embedded Face Detection, May 2005. Continued as Ph.D. Student at Penn State.
37. Thomas Richardson, MS/CSE, On-Chip Interconnects, Dec 2005 (co-advised with Y. Xie). First Job: Availink Inc.
38. Raghavan Ramadoss, December 2006, M.S./CSE, Static and Runtime Optimization Strategies for Variation Aware MPSoC Platforms. Hardware Design Engineering Manager. Cisco, San Francisco.
39. Priya Sundararajan, MS/CSE, Mapping Signal Processing Applications on FPGAs, Dec 2006. Hardware Design Engineer at HCL America, Rochester.
40. Adil Sarwar, December 2006, M.S./CSE, Performance Evaluation of System C and Verilog for RTL Synthesis and System Modeling. MBA Candidate. Worked for Intel as first job after graduation.
41. Charles Addo-Quaye, May 2007, M.S./CSE, Thermal-Aware Placement and Variation for Three-Dimensional Network-on-Chip Designs (Co-advised with Prof. Xie). Assistant Professor, Lewis-Clark State College, in Lewiston, Idaho.
42. Han-Wei Chen, August 2007, M.S./CSE, Impact of Circuit Degradation on Design Security of Field programmable Devices. Intellectual Property Attorney, Perkins Coie LLP
43. Srinath Sridharan, May 2008, M.S./CSE, Performance-Reliability Tradeoffs in designing reorder buffers. Senior Software Engineer at Google.

44. Amol Mupid, Dec 2008, M.S./CSE, Variation-aware CAM structures. Deceased.
45. Kate Kilroy, Dec 2008, M.S./CSE, A Signal Based Approach to an Instrument Driver System.
46. Srijith Rajmohan, MS/EE, May 2009, A Neural Network Based Classifier on Cell Broadband Engine. (co-advised with Dr. Datta). Computational Scientist, Virginia Tech.
47. Aditi Rathi, MS/EE, Dec 2009, A GPU based implementation of Center Surround Distribution Distance Algorithm for feature recognition. (co-advised with Dr. Jenkins). Technical Sales Specialist, Intel India,
48. Vikram Sampath Kumar, MS/EE, May 2010 Connected Component Labeling on FPGAs. IP Logic Designer at Intel.
49. Jesse Scott, MS/CSE, Dec 2010 FPGA based Image recognition. Continued for Ph.D. at Penn State with Bob Collins
50. Dharav Dantara, August 2011. MS/EE, Reconfigurable Accelerators for Neuromorphic Systems. Senior Verification Engineer at Xilinx. He works on New Verification flows/methodology and verification infrastructure automation.
51. Aarti Chandrasekar, October 2011. MS/EE, A Fine-Grained Dataflow Library for Reconfigurable Streaming Accelerators. Logic Design Engineer, Intel, Folsom.
52. Ravindhiran Mukundarajan, December 2011. MS/CSE, Tunnel FET based Field Programmable Gate Arrays. Intel India
53. Kyle Wray, MS/CSE, November 2012 A Game Theoretic Approach To Multi-Agent Systems In Highly Dynamic, Information-Sparse, Role Assignment Scenarios. Ph.D. Student at U Mass.
54. Ranade, Rohit. 2013. MS/EE Image processing using coupled oscillators (Co-advised with Jenkins, Kenneth). Senior Imaging Engineer, GEO Semiconductor Inc, Bay Area.
55. Anusha Chandrasekar, July 2014. MS/CSE, Depth Estimation using monocular cameras. Component Design Engineer, Intel, Folsom.
56. Brigid Smith, MS/BS Honors, March 2015 improving object recognition performance through semantic context extraction. Software Engineer, Amazon.
57. Joshua Snyder, MS/BS(Honors), March 2015 Optimization and Hardware Acceleration of Consensus-based Matching and Tracking. Embedded Systems Engineer, Philips Respironics, PA.
58. Heo, Unsuk. March 2015. MS/CSE A High-efficiency Switched-capacitance Htfet Charge Pump For Low-input-voltage Applications. Software Engineer, Google.
59. Davis, Kameran. April 2015. MS/CSE Real Time Object Tracking On Active Pan Tilt Zoom Camera Using CMT (Co-advised with John Sustersic). Engineer, Applied Research Labs.
60. Jagdish Sabarad, MS/CSE, April 2016 A Reconfigurable Accelerator For Neuromorphic Object Recognition. Staff Embedded Systems Designer, Edwards Lifesciences, Orange County, CA
61. Madineedi, Komala Subhadra. MS/EE June 2016. A platform for evaluating embedded multi-core systems. Verification Engineer, Intel, Phoenix.
62. Jagruti Mohapatra, MS/CSE, July 2016 Prediction and assessment of ambient energy signals for energy harvesting systems.
63. Priyanka Gomatam. MS/CSE. July 2017. Object Recognition Using Structured Feature Extraction With A Reconfigurable, Neurosynaptic Processor. Senior Software Engineer, Visa Inc., Austin.
64. Ikenna Okafor. MS/CSE. July 2017. Hardware Acceleration of Visual Search. Currently at Intel.
65. Vinayaka Krishna MS CSE. May 2018. Dense Convolutional Object Detection For Visual Assistive Systems on Mobile Platforms.
66. Gus Smith BS/MS IUG Honors Student. May 2018. Designing Processing in Memory Architectures Via Static Analysis on Real Programs.
67. Jake Eden BS/MS IUG Honors Student. May 2018. Employing Text Features for Visual Assistance in Navigation and Classification.

68. Skyler Anderson MS CSE May 2019 Adaptive Neural Network Architectures for Power Aware Inference.
69. Zeinab Hakimi MS CSE May 2019 Collaborative Inference for Distributed Camera System.
70. Philip Shin MS CSE May 2019. Context-Aware Collaborative Object Recognition for Multi Camera Time Series Data.
71. Steven Davis MS CSE May 2019. Reinforcement Learning: An Application to Maritime Navigation and Contact Avoidance. (Co-advised with Sustersic)
72. Dong Hyun Kim BS/MS IUG Honors Student. May 2019. Sensor Aware Machine Learning for Edge Devices.
73. Sahithi Ramipalli. A Processing-in-Memory Accelerator Architecture for Graph Analytics. May 2020.
74. Makesh Chandran. Processing in-Memory Architecture Incorporating Systolic Dataflow for Deep Neural Networks. May 2020. Thesis Advisor
75. Grant Eden. BS/MS IUG Honors Student. May 2020. Using a UAV and Edge Computing to Identify and Throw Away Trash.
76. Hariram Thirucherai. MS CSE. May 2021. Optimization of Inter-Cache Traffic Entanglement in Tagless Caches with Tiling Opportunities.
77. Rishab Gulati, 2021. MS CSE. A Toolchain for On-Chip Thermal Management of FPGA Designs.
78. Nelson Troncos, 2022. MS CSE. AIGuide: An Augmented Reality Hand Guidance Application for People with Visual Impairments
79. Abhijeet Kumar. 2022. MS CSE. Deepfake Video Detection in the compressed domain
80. Abhishek Kumar. 2022. MS CSE. Architectural support for in-cache data movements
81. Tongguang Yu. 2022. MS CSE. Hardware Functional Obfuscation With Ferroelectric Active Interconnects
82. Samuel Abrams. 2022. MS CSE. Extending Video Action Recognition in the Compressed Domain Video Analytics in Compressed Domain.
83. Viet Pham. 2022. MS CSE. An Analysis and Framework for Multi-label Image Classification of Insect Taxonomy with Convolutional Neural Networks.
84. Ashwath Swaminathan. 2023. MS CSE. Optimizing existing NLP tasks by employing Knowledge Graphs Knowledge Graph Embedding.
85. Aditya Kannan. 2023. Optimizing privacy preserving neural networks employing homomorphic encryption.

Current M.S. Students

1. Ajay Sridhar. AI Hardware Accelerators. (2022-present)
2. Samarth Tehri. Video Query Systems (2023-present) (IUG Student)

Schreyer's B.S. Honors Thesis (excluding IUG students)

1. Shivank Vatsal. 2023. Haptic Feedback System for Percussive Elements in Music.
2. Anand Raju. 2023. Detecting and Tracking Insects in the InsectEye Device.
3. Yao Xu, 2022. A Microscope Camera System for Producing High-Quality Insect Datasets.
4. Shivran Muralidharan. 2021. Addressing Overfitting Issues with Deep Learning Model for Video Action Recognition.
5. Tianyi Shen. 2021. Attention-Based Human Activity Recognition.
6. Matthew, David de. 2018. The Glove Project: Allowing the Visually Impaired to Understand and Interact with their Environment.
7. Kawchak, Thomas. 2018. Indoor Localization for the Visually Impaired.
8. Gallante, Eric. 2018. The Accuracy of Rhythm Recognition with Convolutional Neural Networks on TrueNorth Processor.

9. Caccese, Ronald. 2015. Comparing Integrate And Fire Neuron Circuits Using TFET And CMOS Technologies
10. Gallagher, Eugene Joseph. 2009. A scalable FPGA platform for LADAR acquisition, control, and processing
11. Turowski, Jacek T. 2007. Network-on-chip router design
12. Yoedt, Cedric T.. 2005 Exploring the impact of soft errors on memory cell design
13. Vuong, Lan N. 2003. Dynamic web design for multiple platforms
14. Rioja, Brandon. 2003. A remote execution framework for an embedded Java environment
15. Lyuboslavsky, Victor. 2000. Design of a databus charge recovery mechanism (Founder of EDAPlayground (Acquired by Doulous) and mdPortal)

Post Doctoral Scholars

1. Keni Qiu, January 2019- 2020, Assistant Professor. Capital Normal University, Beijing.
2. Yuhua Liang, July 2017-2018, Assistant Professor. Xidian University.
3. Xueqing Li, August 2015-December 2018. Associate Professor, Tsinghua University, China (Winner of China 1000 Scholar Program)
4. Ramesh Vaddi, 2014, Assistant Professor, Sivan Nadar University, India
5. Yasuki Tanabe, August 2014-2016, Researcher, Toshiba, Japan
6. Kevin Irick, 2010-2016, Founder, SiliconScapes
7. Michael Debole, 2011, IBM Research
8. Yongseok Jin, 2010, Intel
9. Luan Din, 2010-11
10. Madhu Mutyam, 2007-08, Professor, IIT Madras, India

High School K-12 Summer Interns

1. Tonya Dutta – South Bend, IN – Summer 2022
2. Brent McNeel – Tyrone Area HS – Summer 2019
3. Isabelle Fetzer – Grier School – Summer 2019
4. Eva McCracken – Grier School – Summer 2018
5. Jack Lewis – Tyrone Area HS – Summer 2018
6. Benjamin Hostler, Summer 2016
7. Hannah Schuster, Summer 2016
8. Aiden Call, Summer 2014
9. Megan Koegler, Summer 2014

Research Experience for Teachers

1. Justin Bush, Tyrone Area School District, Summer 2019 and Summer 2020
2. Kelly Forest, Grier School for Girls, Summer 2014 and Summer 2016

International Exchange Summer Interns

1. Gabriel R. Franzoni, Summer 2015 (Sponsored by Institute of International Education)
2. Bernardo Godinho, Summer 2016 (Sponsored by Institute of International Education)

Summary of Curricular Development/Teaching Contributions

Narayanan teaches a wide variety of courses targeted at students at all levels (100-level to 600-level) and involves K-12 students and teachers in his summer educational outreach activities. He has been leading efforts to enhance curriculum development that has been supported by grants from the National Science Foundation, The Technology Collaborative (formerly, Pittsburgh Digital Greenhouse) and through major gifts from Xilinx, and Altera. He developed two new undergraduate courses on digital design that have been widely adopted in several universities across the world. The functional verification instructor portal (2002-current) that he co-developed with Prof. Levitan at UPitt and Bruce Wile, and faculty workshops on Embedded Systems Design developed for the Indo-US Collaboration on Engineering Education (2011-current), his course material has been adopted by more than 100 universities worldwide (such as Technion, Israel; Bristol, UK; Syracuse; Osaka, Japan; JNTU, India). Additionally, course material co-developed with Prof. Irwin for the undergraduate VLSI Design course has been widely distributed since it reinforces the material in the most widely used popular digital integrated circuits book (including to UCLA, U. Maryland, Cairo U., U. Tehran). He co-led the development of a highly successful system-on-chip certificate program (2000-2010) offered along with Carnegie Mellon University and University of Pittsburgh that pioneered the design of virtual laboratory platform to enable geographically-distributed electronic system design. This program served as a role model for similar initiatives across the globe and featured in popular press (including coverage of an interview of Narayanan on NBC). He led an NSF-funded cross-disciplinary curriculum development (2008-2012) involving 23 faculty members from 14 academic disciplines with a vision of nurturing future leaders in areas at the intersection of Biology and Computing. This project seeded a culture of co-taught cross-disciplinary courses, helped form new research collaborations and curricular transition to smaller partner Universities across Pennsylvania. Narayanan has offered several tutorials and organized workshops to promote curricula design in VLSI design, FPGA design, functional verification, low power design, and reliable systems to the broader academic community. He has served as a lecturer under the Indo-U.S. Collaboration for Engineering Education for the last three years to help train faculty in Indian universities. Narayanan has taught a variety of courses from freshman level to graduate level. He also serves as the honors advisor of Computer Engineering majors. He redesigned the sophomore course on logic design with over 300 students, a required course for all electrical engineering, computer engineering and computer science majors. This course was significantly revised with the help of generous grants from industry (Altera and Xilinx).

Teaching (SRTE evaluations)

Year	Semester	Course	Course Rating (Max:7)	Instructor Rating (Max: 7)	Enrollment
1998	Fall	CSE 597K.1	6.13	6.25	10
1999	Spring	CSE 497E.1	5.73	5.67	14
1999	Fall	CSE 477.1	5.07	4.80	27
2000	Spring	CSE 497A	5.80	6.00	24
2000	Spring	CSE 597A	6.13	6.00	11
2000	Fall	CSE 477.1	5.75	5.68	38
2001	Spring	CSE 497A.1	5.91	6.09	25
2001	Spring	CSE 539.1	5.90	5.90	30
2001	Fall	CSE 477.1	6.19	5.94	44
2002	Spring	CSE 497A.1	5.43	5.29	11
2002	Spring	CSE 539.1	5.88	6.13	12
2002	Fall	CSE 497A.1	5.83	6.33	9
2003	Spring	CSE 477.1	5.87	6.04	40
2003	Spring	CSE 577.1	5.50	5.63	21
2003	Fall	CSE 497A.1	5.67	5.56	9
2003	Fall	CSE 597A.1**			
2003	Fall	CSE 598C.1***	5.93	6.13	19
2004	Spring	CSE 539.1	5.30	5.30	25
2004	Spring	CSE 577.1	5.50	4.83	10
2004	Spring	CSE 597B.1**			
2004	Fall	CSE 477.1	6.05	6.14	25
2004	Fall	CSE 597C.1**			
2005	Spring	CSE 575+	5.83	6.50	12
2005	Spring	CSE 598B.1	5.83	6.42	17
2005	Fall	CSE 477.1	5.89	6.33	21
2005	Fall	CSE 478.1~	5.63	5.96	14
2006	Fall	CSE 478-1	5.87	5.83	17
2007	Spring	CSE 539-1	6.21	6.58	26
2007	Fall	CSE 478-1	4.63	5.16	13
2008	Spring	CMPEN 431-1	5.23	5.69	63
2008	Fall	CSE 530-1	5.8	6.17	26
2008	Fall	CSE 597D-1	6.29	6.57	3
2009	Spring	CMPEN 475-1	4.44	4.63	22
2009	Fall	CSE 530-1	6.27	6.36	20
2010	Spring	CMPEN 475-1	4.95	5.71	24
2011	Fall	CMPEN 417-1	6.57	6.57	11
2011	Fall	EE 417-1	6.29	5.86	11
2012	Spring	CMPEN 431-1	4.95	5.05	39
2012	Spring	CSE 539-1	6.13	6.63	10
2012	Fall	CMPEN 417-1	6	6	17
2012	Fall	EE 417-1	6.33	6.5	12
2013	Spring	CMPEN 331-001	4.2	4.12	63
2013	Spring	CMPEN 331-002	5.2	5.6	62
2013	Fall	CMPEN 331-001	4.54	4	64
2013	Fall	CMPEN 331-002	4.19	3.9	60

2014	Spring	CSE 539-001	6.29	6.43	17
2014	Fall	CMPEN 270-001~~	2.1	2.5	16
2014	Fall	CMPEN 270-002~~	2.33	3	17
2014	Fall	CMPEN 270-003~~	2.75	3.13	16
2014	Fall	CMPEN 270-004~~	2.43	2.43	15
2014	Fall	CMPEN 270-005~~	2	3.25	14
2014	Fall	CMPEN 270-006~~	2.7	2.8	18
2014	Fall	CMPEN 271-001	3.25	3.58	31
2014	Fall	CMPSC 296-001	7	7	4
2015	Spring	CSE 539-001	6.56	6.44	12
2015	Fall	CMPEN 111S-001	5	5	24
2015	Fall	CMPEN 111S-002	3.33	3.17	21
2015	Fall	CMPEN 270-001	3.64	4.91	19
2015	Fall	CMPEN 270-002	5.43	6.14	19
2015	Fall	CMPEN 270-003	5.33	5.67	17
2015	Fall	CMPEN 270-004	6.4	6.4	18
2015	Fall	CMPEN 270-005	3.75	4.75	17
2015	Fall	CMPEN 270-006	4	4.75	18
2015	Fall	CMPEN 271-001	5.08	5.67	35
2016	Spring	CSE 577-001	5.63	6	18
2016	Fall	CMPEN 111-001	5.27	5.27	24
2016	Fall	CMPEN 111-002	5.08	5.25	24
2016	Fall	CMPEN 475-001	6	6.57	22
2017	Spring	CMPEN 417-001	5.92	6.08	27
2017	Spring	CSE 539-001	6.71	6.75	13
2017	Spring	EE 417-001	5.14	5.43	21
2018	Spring	EE 417-001	5.25	5.25	27
2018	Spring	CMPEN 417-001	6.33	6.50	38
2018	Fall	CMPEN 539-001	7.00	7.00	10
2018	Fall	CMPEN 475-001	6.75	6.75	5
2019	Spring	EE 417-001	6.69	6.77	34
2019	Spring	CMPEN 417-001	5.92	6.25	32
2019	Fall	CMPEN 597-004	6.71	6.71	20
2019	Fall	CMPEN 475-001	7.00	7.00	5
2020	Fall	CSE 539	7.00	7.00	11
2021	Fall	CSE 530	7.00	7.00	47
2022	Fall	CSE 530	7 (Mode)	7 (Mode)	75

*Mean Score

**Class size too small, no SRTE's done

***With Irwin, Kandemir

#Number of SRTEs exceeds enrollment

+With Irwin

~Cross-listed course with EE, but scores only shown for CSE

~~ Includes evaluation of lab sections offered by other instructors and involved major revamp of the curriculum for a required course for majors in computer engineering, electrical engineering and computer science.

SERVICE

Selected Leadership Experiences (Since 2015):

Lead, Academic and Startup Programming, India-US Defense Acceleration Eco-System (INDUS-X), March 2023 -

Narayanan supports the Penn State President and VP of Global Engagement in their leadership roles in INDUS-X effort. He coordinates with both the US Department of Defense (Office of Science Policy) and Indian Ministry of Defense towards establishing a program for academic partnerships for enabling defense startups. In this role, he engages with academic, government, industry and non-profit leadership in both countries towards developing specific aspects of this program. He has involved additional Penn State researchers in leading specific aspects of this initiative. The collective efforts of this team received a commendation in a joint release by US and India Governments.

Associate Dean of Innovation, College of Engineering, Jan 2023-

Narayanan engaging leaders from government agencies and industry to create more awareness of our unique research strengths. He is also working on creating better awareness among our researchers on aspects such as government relations, global engagement, industry commercialization and foundation funding through a new seminar series. He continues to spend effort in keeping the morale of our researchers high in this difficult budget environment.

Interim Director of Limited Submission, Office of Senior Vice President of Research, The Pennsylvania State University, January 2020 -

In this role, Narayanan supervises the selection process for all external research submissions that have institutional limits across Penn State and all of its campuses. Administrative responsibility includes interactions involving engagement with associate deans of research, foundations and corporate relations and the strategic research office, managing peer review process. He helped create a more transparent and equitable review process and institutionalized these through policy changes.

that were approved and adopted. He led the formation of an expert panel review system drawn from experts across the campus to assist the senior vice-president of research to make informed decisions for down select decisions for external competitions. This system has enabled to shift the review workload from administrators to topical experts. It has also enabled a robust feedback mechanism to help improve the quality of external submissions. The role involves coordination and interaction with the members of the University Research Council, foundation relations, and support staff.

Director, Center for Artificial Intelligence Foundations and Engineered Systems. The Pennsylvania State University, March 2021-

Narayanan initiated this inter disciplinary center in support of the University's AI initiative. The center formation was initiated in January 2020. He gained financial support and administrative approval from 24 participating units and has brought together 80 faculty members. The center has already helped bring together researchers from multiple units through successful external funded projects, partnerships with industry, new student recognition awards and regular research gatherings.

Associate Director, Department of Energy 3DFeM Research Center, September 2021-

Narayanan provides the system and architecture direction to this inter-disciplinary, inter-institution research center focused design of ferroelectrics for three dimensional chips. He assists the director with all administrative activities including policy design, external interactions, and budget support. He has been involved with enhancing team dynamics across research thrusts, mentoring junior faculty and helping with Key Performance Indicator design for center evaluation.

Thrust Leader, DARPA/Semiconductor Research Corporation Center for Brain-Inspired Computing, January 2018-Sep 2023

Narayanan led the thrust on distributed intelligence and provided technical leadership in shaping the collective efforts of this thrust. He is responsible for highlighting the technical advances and impact to the sponsors through quarterly reports, meetings with industry/DoD liaisons, presentations to industry sponsors and annual review. This role involves understanding and learning contributions of my research colleagues, connecting their contributions and amplifying their relevance to the sponsors.

Chair, Association of Computing Machinery Special Interest Group on Design Automation (SIGDA), July 2015-July 2018

Narayanan led the executive committee of SIGDA in this elected position. SIGDA sponsors or co-sponsors around 20 events a year. These include large conference-exhibits such as Design Automation Conference (DAC), Design Automation and Test in Europe, topical symposium, diversity focused events and student competitions. SIGDA made key structural changes to the sponsorship of DAC that increased the share of SIGDA to 50% and secured partnership with major exhibitors for a five-year period. SIGDA launched the first commercial partnership with two companies for sponsoring student events throughout year. SIGDA increased its footprint of activities outside the United States and increased its presence in Asia rapidly.

Lead PI, National Science Foundation Expeditions-in-Computing Visual Cortex on Silicon, 2014-2021

Narayanan helped bring together a team of 16 faculty from 9 institutions spanning disciplines from Neuroscience, Material Science, Computer Science, Psychology, and Electrical Engineering towards building intelligent vision systems that assist persons with visual impairment. The program resulted in many foundational advances in semiconductor technology and computing systems that have led to multiple follow-on funded centers. The work also resulted in novel AI and Human Computer Interface technologies that have proven to be successful in assisting persons with visual impairments and are currently being made aware to the public through partnerships.

Penn State Service Summary:

1. Narayanan has served in numerous leadership roles including serving as Director for Graduate Affairs for CSE, Chair of the College of Engineering Academic Integrity Committee, Endowed/Distinguished Professor Review Committee, Educational Liaison for Penn State for the System-on-Chip Certification Program (offered to EE/CSE students) offered jointly by CMU/UPitt/Penn State, member of the departmental promotion and tenure committee and awards committee, and as student advisor of the IEEE Computer Society and the Penn State Vegetarian Club.

2. Prof. Narayanan organized a workshop for high school and middle school teachers in Summer 2015 to introduce projects involving intelligent vision systems for K-12 education. He and his students have also been exhibiting in the State College Area K-12 Exploration-U science fairs for the past five years. He has also hosted high school teachers and high school children in summer research projects. In 2017, he co-developed and offered a week-long summer camp for middle school girls on “computing for societal benefits” that received coverage from local media and appreciation from community.

Summary of Service to Profession:

1. Dr. Narayanan served as the elected chair of the ACM Special Interest group on Design Automation, the technical group that sponsors over 15 annual technical conferences in the field of Electronic Design Automation.
2. Dr. Narayanan served as editor-in-chief (2014-2017) of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. He served as associate editor (2006-2009), deputy-editor-chief (2009-2013).
3. Dr. Narayanan served as founding co-editor-in-chief for ACM Journal on Emerging Technologies in Computer Systems from 2003-2005 and as the editor-in-chief from 2006-2009.
4. He served as associate editor for IEEE Transactions on VLSI (2003-2007) and Journal of Low Power Electronics (2003-current).
5. He has also served as a guest editor for ACM Transactions on Embedded Systems, IEEE Transaction on VLSI and IEEE Journal on IEEE Journal on Emerging and Selected Topics in Circuits and Systems.

6. Dr. Narayanan has played active role in various conferences most notably as the chair of advisory committee for Design Automation conference (2022-) and executive committee member (2017-2021), annual International Low Power Symposium on Electronics and Design series, serving as program co-chair in 2007, as general co-chair in 2008, and on the steering committee since 2009; as steering committee member of IEEE Computer Society Annual Symposium on VLSI since 2005; as steering committee member of IEEE/ACM Great Lakes Symposium on VLSI from 2007-2013.
7. He has served as the chair of IEEE CS technical committee on VLSI, vice-chair of student activities for IEEE CS, and as the chapter representative for student activities of IEEE.
8. He served as a member of the publications board of IEEE CEDA and served as the elected member of technical committee on design and implementation of signal processing systems of the IEEE Signal Processing Society.
9. He initiated and co-led a series of three workshops on "Hardware Support for Objects and Microarchitectures for Java" that helped nurture the technology that is now ubiquitous in most mobile and embedded devices.
10. He served on the program committees and in organizing committees of various design automation, VLSI and computer-architecture conferences.
11. Narayanan has served as a panelist/expert reviewer for funding agencies around the world including: National Research Foundation, Singapore, European Union, Research Grants Council, Hong Kong, The Technology Foundation STW, Dutch Research Agency, U.S. Department of Energy, U.S. National Science Foundation, Swiss National Science Foundation, Taibah University Research Funding, Saudi Arabia, Cyprus University of Technology External Promotion Evaluation Committee Member, Canada Foundation for Innovation.

Service to the University

University-Level Service

- Lead, Academic and Startup Programming, India-US Defense Acceleration Eco-System (INDUS-X), March 2023 -present. Narayanan supports the Penn State President and VP of Global Engagement in their leadership roles in INDUS-X effort. He coordinates with both the US Department of Defense (Office of Science Policy) and Indian Ministry of Defense towards establishing a program for academic partnerships for enabling defense startups. In this role, he engages with academic, government, industry and non-profit leadership in both countries towards developing specific aspects of this program. He has involved additional Penn State researchers in leading specific aspects of this initiative. The collective efforts of this team received a commendation in a joint release by US and India Governments.
- Interim Director of Limited Submission, Office of Senior Vice President of Research, The Pennsylvania State University, January 2020-present. Narayanan supervises the selection process for all external research submissions that have institutional limits across Penn State and all of its campuses. Administrative responsibility includes interactions involving engagement with associate deans of research, foundations and corporate relations and the strategic research office, managing peer review process. He helped create a more transparent and equitable review process and institutionalized these through policy changes that were approved and adopted. He led the formation of an expert panel review system drawn from experts across the campus to assist the senior vice-president of research to make informed decisions for down select decisions for external competitions. This system has enabled to shift

the review workload from administrators to topical experts. It has also enabled a robust feedback mechanism to help improve the quality of external submissions. The role involves coordination and interaction with the members of the University Research Council, foundation relations, and support staff.

- Director, Center for Artificial Intelligence Foundations and Engineered Systems. The Pennsylvania State University, March 2021-present. Narayanan initiated this inter disciplinary center in support of the University's AI initiative. The center formation was initiated in January 2020. He gained financial support and administrative approval from 24 participating units and has brought together 80 faculty members. The center has already helped bring together researchers from multiple units though successful external funded projects, partnerships with industry, new student recognition awards and regular research gatherings.
- Member, University Research Council, Jan 2023-
- Reviewer, Schreyer Honors College Selection Committee, 2022 and 2023.
- Member, SIMBA Task Force, January-February 2021
- Member, SIMBA Research Administration and Reporting Working Group, March 2021-August 2021.
- Member, Artificial Intelligence Director Search Committee, 2021
- Member, SIRO Associate Director Search, 2021
- Advisory Committee Member, Smart Spaces Center, 2008
- Penn State Educational Coordinator, The Technology Collaborative (formerly Pittsburgh Digital Greenhouse) System-on-Chip Graduate Certificate Program (2001-2010)

Service to Student Organizations

Faculty Advisor, Vegetarian Club, 2007-present; Cricket Club (6/05-6/06), IEEE Computer Society, 1999-2007, Augmented Reality Lab, 2016-18, Unmanned Aerial Systems Group, 2016-19

Service to College of Engineering

- Associate Dean of Innovation, College of Engineering, Jan 2023-present. Narayanan engaging leaders from government agencies and industry to create more awareness of our unique research strengths. He is also working on creating better awareness among our researchers on aspects such as government relations, global engagement, industry commercialization and foundation funding through a new seminar series. He continues to spend effort in keeping the morale of our researchers high in this difficult budget environment.
- Chair, Promotion and Tenure Committee, College of Engineering (September 2020-September 2021)
- Member, Promotion and Tenure Committee, College of Engineering (September 2019-September 2020)
- Chair, College Review Committee for Chaired and Endowed Professors. (September 2016 - 2017)
- Member, College Review Committee for Chaired and Endowed Professors. (September 2015 - 2016)
- Member, Committee to examine the relationship between Electrical Engineering and Computer Science and Engineering, Member. 2015-16
- Member, Search Committee for the Associate Dean for Research and Innovation (ADRI), 2014
- Member, Faculty Search Committee, Electrical Engineering, 2013, 2015-17.
- Member, PSEAS Awards Selection Committee, 2013
- Chair, College Academic Integrity Committee, 2010-11

- Member, Academic Integrity Committee, 2009-10
- Member, AD-14 Committee, Electrical Engineering Department Head AD-14 Review, 2008
- Member, Radiation Science & Engineering Center Director Search Committee, 2007-08
- Member, PSES Awards Selection Committee, 2007-08
- CSE Advisor, Engineering Advising Center (Spring), 2000

Service to CSE Dept and School of EECS

- Member, Graduate Committee, Curriculum (2022-23)
- Member, Undergraduate Committee, Workload (2022-23)
- Chair, CSE DEI Committee (2022-23)
- Member, Strategic Committee, CSE, Committee Member. (August 2013 - Present).
- Member, Strategic Committee, School of EECS, (2021-23)
- Chair, Outreach Committee K-12 Activities, Computer Science and Engineering Department, 2018-current (In this role, I initiated coordination with the SCASD leadership on engagement in their CS curricular design. During the COVID remote learning period, I coordinated the development of remote lectures for K-5 students after-school program. I also coordinated with CSATS to engage high school science teachers and summer interns in summer research programs.)
- Chair, PhD Qualifying Exam, Computer Architecture, Spring 2020
- Member, Curriculum Committee, Department of CSE (2020-Present)
- Hiring Committee, Chairperson. (October 2015 - 2017).
- Personnel Committee, Committee Member. (December 2014 - Present).
- Publications Committee, Committee Member. (August 2014 - Present).
- Search Committee, Associate Dean for Research and Innovation, Committee Member. (2014).
- Augmented Reality Lab, Faculty Advisor. (October 15, 2016 - Present).
- Unmanned Aerial Systems Group, Faculty Advisor. (October 15, 2016 - Present).
- Vegetarian Club, Faculty Advisor. (2007 - Present).
- Honors Advisor for Computer Engineering. (September 2015 - Present).
- Organized a workshop for high school and middle school teachers in Summer 2015 to introduce projects involving intelligent vision systems for K-12 education.
- Computer Science Girls Summer Camp (August 2017)
- Member, Laboratory Committee, 1998-2000
- Member, Climate Committee, 1999
- Member, ABET/CQI Committee, 1999-2001
- IEEE Computer Society Student Advisor, 1999-2007
- Chair, Ph.D. Candidacy Exam, Track B. 1999-2004
- Member, Graduate Committee, 2000-2004, 2007-09
- Chair, Colloquium Committee, 2001-02
- Member, Publications/Web Committee,2001-07, 12-13
- Member, Move Committee to new building, 2003-04
- Graduate Program Officer, Department of Computer Science and Engineering, 2005-07
- Member, Awards Committee, 2009-13
- Member, Promotion and Tenure Committee, CSE, 2009-10, 2016-17
- Member, Promotion and Tenure Committee, School of EECS, 2016-17
- Chair, Promotion and Tenure Committee, School of EECS, 2018-19.
- Co-Chair, Outreach Committee, CSE, 2016-2017

Service to Governmental Agencies

- Coordinator, India-US INDUS-X Academic and Startup Partnerships.
- Chair, Site Visit Team, NSF Expeditions in Computing Review Panel, MIT (2014).
- NSF Panelist (Multiple times on yearly basis)

Service to the Disciplines and to the Profession

Editorial Activities:

2014-17	Editor-in-Chief, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
2021-present	Associate Editor-in-Chief, IEEE Micro
2015-present	Associate Editor, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits
2003-18	Associate Editor, Journal of Low Power Electronics and Design
2009-13	Deputy Editor-in-Chief, IEEE Transactions on Computer-Aided Design
2006-09	Associate Editor, IEEE Transactions on Computer Aided Design
2006-09	Editor-in-Chief, ACM Journal of Emerging Technologies in Computing
2004-05	Founding Co-Editor-in-Chief, ACM Journal of Emerging Technologies in Computing
2004	Guest Editor, IEEE Transactions on VLSI, Special Issue on Low Power Design and Electronics
2003-2007	Associate Editor, IEEE Transactions on VLSI
2002	Co-Editor (with M. Wolczko), Java Microarchitectures, Book Volume, Kluwer Academic (In Press)
1998-00	Newsletter Editor, IEEE Technical Committee on VLSI
1995	Editor, looking .forward, IEEE Computer Society Student Newsletter, (Spring)
1994	Editor-in-Chief, looking .forward, IEEE Computer Society Student Newsletter (Fall)

Organizing Conferences and Service on Conference Committees:

1998-99	Publicity Chair, IEEE Computer Society Annual Workshop on VLSI (April 1999)
1999	Member, Program Committee, International Conference on Advanced Computing (December)
1999	Program Co-Chair, First Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with ICCD'99), Austin, TX (October)
2000	General Co-Chair; Member, Program Committee, IEEE Annual Workshop on VLSI (April)

2000 Workshop Chair, Design Automation Conference VLSI Design Educators Workshop

2000 Program Committee Member, Workshop on Compilers and Operating Systems for Low Power (COLP '00), Philadelphia, PA (September)

2000 Program Co-Chair, Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with ICCD'00), Austin TX (September)

2000 Member, Program Committee, 2000 IEEE Asia-Pacific Conference on Circuit and Systems, Crystal Palace Hotel, Tianjin, China (December 4-7)

2001 General Co-Chair, IEEE Annual Workshop on VLSI (WVLSI 2001), Orlando, FL (April 19-20)

2001 Member, Program Committee, International Conference on Microsystems Education (MSE 2001), Las Vegas, NV (June 17-18)

2001 Member, Program Committee, and Treasurer, International Symposium on Low Power Electronics and Design (ISLPED'01), Huntington Beach, CA (August 6-7)

2001 Member, Program Committee, Workshop on Compilers and Operating Systems for Low Power (COLP '01), Barcelona, Spain (September 9)

2001 Member, Program Committee, International Conference on Computer Design (ICCD 2001), Austin, TX (September 23-26)

2001 Member, Program Committee, International Conference on High Performance Computing (HiPC 2001), Hyderabad, India (December 17-20)

2001 Member, Program Committee, IEEE Fourth Annual Workshop on Workload Characterization (WWC-4), held in conjunction with MICRO-34, Austin, TX (December)

2002 General Co-Chair/Program Committee Member/Steering Committee Member, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2002), Pittsburgh, PA (April 25-26)

2002 Treasurer/Program Committee Member, International Symposium on Low Power Electronics and Design (ISLPED '02), Monterey, CA (August 12-14)

2002 Workshop Co-Chair, Teaching Functional Verification, DAC 2002, New Orleans, LA (June)

2002 Member, Program Committee, International Conference on Computer Design (ICCD 2002), Freiburg, Germany (September 16-18)

2002 Member, Program Committee, Workshop on Embedded System Codesign (ESCODES '02), San Jose, CA (September 24)

2002 Member, Program Committee, Workshop on Compilers and Operating Systems for Low Power (COLP '02), VA (September)

2002 Member, Program Committee, IEEE 5th Annual Workshop on Workload Characterization, Austin, TX (November 25)

2003 General Chair/Program Committee Member/Steering Committee Member, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2003), Tampa, FL (Feb 21-22)

2003 Member, Technical Program Committee, IEEE Design Automation and Test in Europe (DATE 2003), Munich, Germany (March 3-7)

2003 Member, Program Committee, Great Lakes Symposium on VLSI, Washington D.C. (April 28-29)

2003 Member, Program Committee, International Conference on Microsystems Education (MSE 2003), Anaheim, CA (June 1-2)

2003 Member, Program Committee/Treasurer, International Symposium on Low Power Electronics and Design (ISLPED '03), Seoul, Korea (August 25-27)

2003 Member, Program Committee, Workshop on Compilers and Operating Systems for Low Power (COLP '03), New Orleans, LA (September 27)

2004 Member, Program Committee, International Symposium on High Performance Computer Architecture (HPCA-10), Madrid Spain (February 14-18)

2004 Member, Technical Program Committee, IEEE Design Automation and Test in Europe (DATE 2004), Paris, France (February 16-20)

2004 Member, Program Committee/Steering Committee, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2004), Lafayette, LA (February 19-20)

2004 Member, Program Committee, IEEE International Symposium on Performance Analysis and Systems and Software (ISPASS '04), Austin, TX (March)

2004 Member, Program Committee, Great Lakes Symposium on VLSI (GLSVLSI 2004), Boston, MA (April 26-28)

2004 Treasurer, International Symposium on Low Power Electronics and Design (ISLPED '04), Newport Beach, CA (August 9-11)

2004 Technical Program Committee Member, System and Software Design, International Symposium on Low Power Electronics and Design (ISLPED '04), Newport Beach, CA (August 9-11)

2004 Program Committee Member, Processor Architecture Track, International Conference on Computer Design (ICCD 2004), San Jose, CA (October 11-13)

2005 Track Co-Chair, Technical Program Committee, Emerging and Innovative Technologies, IEEE Design Automation Test in Europe, Munich, Europe (March 7-11)

2005 Program Committee Member, 2005 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2005), Austin, TX (March 20-22)

2005 Member, Program Committee, Third IEEE/ACM Workshop on Optimizations for DSP and Embedded Systems (ODES), San Jose, CA (March 20)

2005 Track Chair, Emerging Technologies, Great Lakes Symposium on VLSI (GLSVLSI 2005), Chicago, IL (April 17-19)

2005 Member, Program Committee/Steering Committee, IEEE Computer Society Annual Symposium on VLSI, Tampa, FL (May 11-12)

2005 Member, Program Committee, International Workshop on Computer Architecture for Machine Perception (CAMP'05), Palermo, Italy (July 4-6)

2005 Treasurer, International Symposium on Low Power Electronics and Design (ISLPED 2005), San Diego (August 8-10)

2005 Member, Program Committee, IEEE Workshop on Signal Processing Systems (SiPS 2005), Athens, Greece (November 2-4)

2006 Web Chair, Twelfth International Symposium on High Performance Computer Architecture (HPCA-12), Austin, TX (February 11-15)

2006 Member, Program Committee/Steering Committee, IEEE Computer Society Annual Symposium on VLSI, Karlsruhe, Germany (March 2-3)

2006 Track Chair, Technical Program Committee, Emerging and Innovative Technologies, IEEE Design Automation Test in Europe (DATE 2006), Munich, Germany (March 6-10)

2006 Program Committee Member, 2006 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2006) (March 19-21)

2006 Member, Program Committee, Fourth IEEE/ACM Workshop on Optimizations for DSP and Embedded Systems (ODES), New York, NY (March 26)

2006 Program Co-Chair, Great Lakes Symposium on VLSI (GLSVLSI 2006), Philadelphia, PA (April 30-May 2)

2006 Member, Program Committee, 2006 IEEE International Conference on Acoustics, Speech, and Signal Processing, Toulouse, France (May 14-19)

2006 Member, Program Committee, International Workshop on Advanced Low Power Systems (ALPS 2006), in conjunction with Twentieth International Conference on Supercomputing, Cairns, Australia (July 1)

2006 Program Co-Chair, First International Conference on Nano-Networks (Nano-Net 2006). Lausanne, Switzerland (September)

2006 Member, Technical Program Committee and Treasurer, International Symposium on Low Power Electronics and Design (ISLPED 2006), Tegernsee, Germany (October 4-6)

2006 Member, Program Committee, IEEE Workshop on Signal Processing Systems (SiPS 2006), Banff, Canada (October)

2007 Member, Program Committee, Thirteenth International Symposium on High Performance Computer Architecture (HPCA-13), Phoenix, AZ (February)

2007 Member, Program Committee, CMP-MSI: Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMPMSI 2007), in conjunction with HPCA-13, Phoenix, AZ (February)

2007 Track Chair, Technical Program Committee, Emerging and Innovative Technologies, and Member, Steering Committee, IEEE Design Automation Test in Europe (DATE 2007), Nice, France (April)

2007 Member, Program Committee, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2007), Porto Alegre, Brazil (May)

2007 Member, Program Committee, International Workshop on Advanced Low Power Systems (ALPS 2007), in conjunction with ICS 2007, Seattle, WA (June)

2007 Program Co-chair, International Symposium on Low Power Electronics and Design (ISLPED 2007), Portland, OR (August)

2007 General Vice Chair, Second International Conference on Nano-Networks (Nano-Net 2007), Catania, Italy (September)

2007 Member, Program Committee, IEEE Seventh International Conference on Computer and Information Technology, Fukushima Japan (October)

2007 Member, Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2007), San Jose, CA (November)

2007 Member, Program Committee, 2007 IFIP International Conference on Embedded and Ubiquitous Computing, Taipei (December)

2008 Member, Program Committee, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2008), Montpellier, France (April)

2008 General Co-Chair, 2008 Great Lakes Symposium on VLSI (GLSVLSI 2008), Orlando, FL (May)

2008 Member, Program Committee, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH '08), Anaheim, CA (June)

2008 Member, Program Committee, IEEE Eighth International Conference on Computer Information Technology (CIT 2008), Sydney, Australia (July)

2008 General Co-Chair, International Symposium on Low Power Electronics and Design (ISLPED 2008), Bangalore, India (August)

2008 Member, Technical Program Committee, 2008 International Conference on Computer-Aided Design (ICCAD 2008), San Jose, CA (November)

2008 Member, Technical Program Committee, 2008 Design Automation Conference (DAC 2008), San Jose, CA (November)

2009 Member, Steering Committee, Great Lakes Symposium on VLSI (GLSVLSI 2009), Boston, MA (May)

2009 General Chair, IEEE Computer Society Annual Symposium on VLSI 2009, Tampa, FL (May)

2009 Member, Program Committee, Forty-Sixth Design Automation Conference (DAC 2009), San Francisco, CA (July)

2009 Member, Program Committee, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH 2009), San Francisco, CA (July)

2009 Member, Program Committee, IEEE Workshop on Signal Processing Systems (SiPS 2009), Tampere, Finland (October)

2009 Track Chair, Technical Program Committee, IEEE/ACM 2009 International Conference on Computer-Aided Design (ICCAD 2009), San Jose, CA (November)

2010 Track Chair, Technical Program Committee, Twenty-Third International Conference on VLSI Design (VLSI Design 2010), Bangalore, India (January)

2010 Treasurer/Member, Technical Program Committee, Sixteenth IEEE International Symposium on High-Performance Computer Architecture (HPCA-16), Bangalore, India (January)

2010 Member, Program Committee, Design, Automation & Test in Europe (DATE 2010), Dresden, Germany (March)

2010 Member, Steering Committee, Eighteenth ACM Great Lakes Symposium on VLSI (GLSVLSI 2010), Providence, RI (May)

2010 Member, Program Committee, Forty-Seventh Design Automation Conference (DAC 2010), Anaheim, CA (June)

2010 Member, Steering Committee, International Symposium on Low Power Electronics and Design (ISLPED 2010), Austin, TX (August)

2011 Member, Program Committee, Twenty Fourth International Conference on VLSI Design (VLSI Design 2011), Chennai, India (January)

2011 Member, Program Committee, IEEE Seventeenth International Symposium on High Performance Computer Architecture (HPCA 2011), San Antonio, TX (February)

2011 Member, Program Committee, Design, Automation and Test in Europe (DATE 2011), Grenoble, France (March)

2011 Member, Steering Committee, Twenty-First Great Lakes Symposium on VLSI (GLSVLSI 2011), Lausanne, Switzerland (May)

2011 General Co-Chair and Steering Committee Member, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2011), Chennai, India (July)

2011 Member, Steering Committee, International Symposium on Low Power Electronics and Design (ISLPED 2011), Fukuoka, Japan (August)

2011 Member, Program Committee, International Conference on Parallel Processing (ICPP 2011), Taipei, Taiwan (September)

2011 Member, Program Committee, IEEE Workshop on Signal Processing Systems (SiPS 2011), Beirut, Lebanon (October)

2011 Member, Program Committee, Nineteenth IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2011), Hong Kong, China (October)

2012 Chair, Special Session 2: Domain Specific Accelerators, Seventeenth Asia and South Pacific Design Automation Conference (ASP-DAC 2012), Sydney, Australia (January 30-February 2)

2012 Member, Technical Program Committee, Design, Automation & Test in Europe (DATE 2012), Dresden, Germany (March)

2012 Member, Technical Program Committee, Twenty-Second Great Lakes Symposium on VLSI (GLSVLSI 2012), Salt Lake City, UT (May)

2012 Member, Steering Committee, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2012), Amherst, MA (August)

2012 Organizer, First International Workshop on Domain-Specific Multicore Computing (DSMC 2012), in conjunction with ICCAD 2012, San Jose, CA (November)

2012 Member, Program Committee, Forty-Fifth Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-45), Vancouver, Canada (December)

2013 Member, Technical Program Committee, Twenty-Sixth International Conference on VLSI Design (VLSID 2013), Pune, India (January)

2013 Member, Technical Program Committee, Design, Automation & Test in Europe (DATE 2013), Grenoble, France (March)

2013 Member, Technical Program Committee, International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2013), Grenoble, France (March)

2013 Co-Chair, Low Power Track, Great Lakes Symposium on VLSI (GLSVLSI 2013), Paris, France (May)

2013 Member, Steering Committee, IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2013), Natal, Brazil (August)

2013 Executive Committee, International Symposium on Low Power Electronics and Design (ISLPED 2013), Beijing, China (September)

2013 Member, Technical Program Committee, Twenty-First IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SoC 2013), Istanbul, Turkey (October)

2013 Track Chair, Technical Program Committee, 2013 International Conference on Computer-Aided Design (ICCAD 2013), San Jose, CA (November)

2013 Member, Technical Program Committee and Advisory Committee, First IEEE International Conference on Control, Automation, Robotics & Embedded Systems (CARE 2013), Jabalpur, India (December)

2014 Member, Technical Program Committee, Design, Automation & Test in Europe (DATE 2014), Dresden, Germany (March)

2014 Member, Executive Committee, International Symposium on Low Power Electronics and Design (ISLPED 2014), La Jolla, CA (August)

2014 Member, Technical Program Committee, Eighth International Symposium on Networks-on-Chip (NOCS 204), Ferrara, Italy (September)

2014 Member, Technical Program Committee, Twenty-Second IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SoC 2014), Playa del Carmen, Mexico (October)

2014 Member, Technical Program Committee, Thirty-Third IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2014), San Jose, CA (November)

2015 Member, Technical Program Committee, Design, Automation & Test in Europe, Grenoble, France

2015 International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES 2015), Program Committee, Member. Amsterdam The Netherlands. (October 2015).

2015 IEEE/ACM WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD SELECTION COMMITTEE

2015 Member, Technical Program Committee, Thirty-Third IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2015), San Jose, CA (November)

2015 External Program Committee Member, International Symposium on Computer Architecture

2015-present Executive Committee, Member. Design Automation Conference Committee

2015-16 Vice-Chair, Steering Committee, IEEE Computer Society Annual Symposium on VLSI

2009-present Member, Executive Committee, International Symposium on Low Power Electronics and Design.

2016 Member, External Technical Program Committee, International Symposium on High Performance Computer Architecture, Barcelona, Spain

2016-present Member, Steering Committee, IEEE Computer Society Annual Symposium on VLSI

2016 Track Co-Chair, Embedded systems: Architecture, design, and software, IFIP VLSI SoC, Tallinn, Estonia

2016 Member, Program Committee, International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES 2016).

2016 Member, Technical Program Committee, Design, Automation & Test in Europe, Dresden, Germany

2016 General Co-Chair, The 2016 IEEE International Conference on Embedded Software and Systems (ICESS2016), Chengdu, China

2017 Member, Technical Program Committee, International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES 2017), Program Committee.

2017 Member, Technical Program Committee, Design, Automation & Test in Europe, Lausanne.

2017 Track Co-Chair, Embedded systems: Architecture, design, and software, IFIP VLSI SoC, Abu Dhabi

2018 Member, External Program Committee, IEEE International Symposium on High-Performance Computer Architecture

2018 Member, Program Committee, Design Automation and Test in Europe

2019 Member, Program Committee, International Conference on Computer Design

2019 Member, Program Committee, 25th IEEE International Symposium on High-Performance Computer Architecture

2020 Member, Program Committee, VLSI Design, India

2018-21 Member, Program Committee, International Conference on Compilers, Architectures, and Synthesis of Embedded Systems.

2020 Member, External Program Committee, International Symposium on Computer Architecture

2020 General Co-Chair, IEEE CS Annual Symposium on VLSI

2019-20 Chair, Design Automation Conference Late Breaking Results

2021 Member, Program Committee, International Symposium on Computer Architecture

2021 Member, Program Committee, IEEE International Symposium on High-Performance Computer Architecture

2022 Member, External Program Committee, International Symposium on Computer Architecture

2022 Member, External Program Committee, IEEE International Symposium on High-Performance Computer Architecture

2023 Chair, Advisory Committee, Design Automation Conference.

Participation in or Service to Professional and Learned Societies:

1997-98	Task Force Member, IEEE Computer Society Youth Forum in Computer Science and Engineering (YUFORIC)
1999-2006	Vice-Chair, Student Activities, IEEE Computer Society Chapter Activities Board
2001	Chair, IEEE Computer Society Technical Committee on VLSI
2004-2006	Chapter Representative, Student Activities Board, IEEE
2005-08	Elected Member, Technical Committee on Design and Implementation of Signal Processing Systems of the IEEE Signal Processing Society
2014	Member, IEEE Computer Society Fellows Selection Committee
2014-2017	IEEE Council on Electronic Design Automation, Publications Board, Member.
2015-2018	Chair, ACM Special Interest Group on Design Automation
2019-2021	Member, Executive Committee, ACM Special Interest Group on Design Automation
2020-2021	Member, Conferences Committee of ACM's Publications Board
2023	Member, IEEE CEDA Publications Board