Who we are

- We are the semiconductor device modeling group which is part of MSCAD laboratory at University of Arkansas, Fayetteville.

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UARK SiC Power MOSFET Model V1.0.0

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Fayetteville

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1. Overview of UARK SiC Power MOSFET model

2. The SiC Power MOSFET model presented here is based on the analytical model published in [1] and [2]. A 1200 V, CREE device (C2M0025120D) has been used in this work to illustrate the parameter extraction and model validation. Chapter 2 explains the process of parameter extraction sequence using the device datasheet and Chapter 3 shows the model validation using double pulse tester circuit. Chapter 4 shows the comparison between MAST and Verilog-A codes of the model. Chapter 5 entails all the parameters used in the model and Chapter 6 comprises of the model equations. Finally, chapter 7 includes the people involved in this project.

References:

[1] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. H. Ryu, " Silicon carbide power MOSFET model and parameter extraction sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353-363, Mar. 2007.

[2] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, Jr., H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model", *IEEE Trans. Power Electron*, vol. 29, no. 5, pp 2220-2228, May 2014.

Sponsor:

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2. Parameter Extraction Sequence

The SiC Power MOSFET model parameters are extracted in a set sequence such that only the characteristics that are readily available in the device datasheets of most commercial devices are required. In the absence of device datasheets, the user may be required to measure the device characteristics to extract the device model parameters.

The parameter extraction sequence requires the following device characteristics in the given order for the extraction of useful parameters for any transient simulation or power electronic application.

1) Capacitance vs. Voltage Characteristics (also referred to as CV characteristics)
2) Device Transfer Characteristics (also referred to as I_d – V_{gs} Characteristics)
3) Device Output Characteristics (also referred to as I_s – V_{ds} Characteristics)

To demonstrate the parameter extraction sequence, the characteristics from a commercially available datasheet of the 1200 V CREE power MOSFET (C2M0025120D) are used.

1) Capacitance vs. Voltage Characteristics:

   The parameters which must be adjusted to fit the CV characteristics are listed in the order below:

   C_{RSS} Curve: C_{oxd}, V_{td}, n_b, and a_{gd}

   C_{OSS} Curve: C_{ds}, and m

   C_{ISS} Curve: C_{gs}

   Fig. 1(a) shows the test schematic used to simulate the CV characteristics and Fig. 1(b) shows the CV characteristics for the C2M0025120D CREE device and the simulated characteristics after the extraction of the aforementioned parameters. The plots also reveal the regions within the curves that are affected by the parameters as shown in [2].

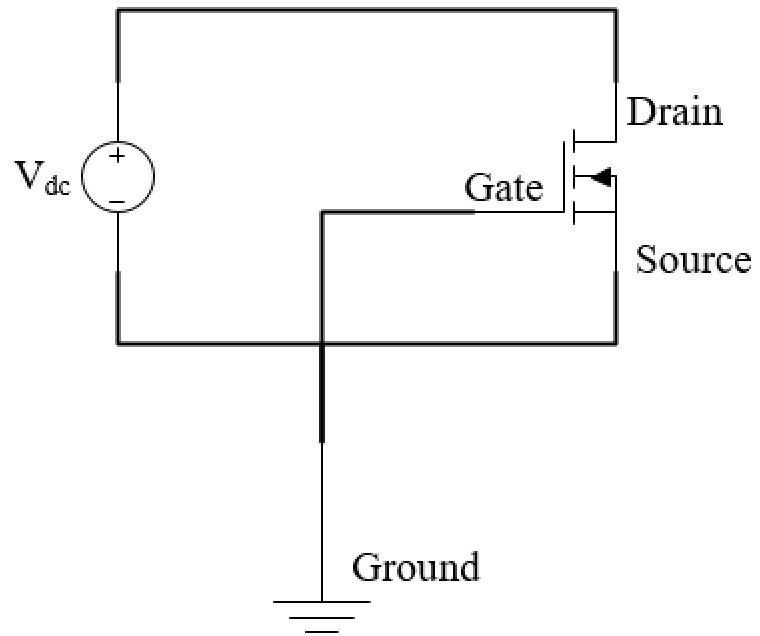


Fig. 1 (a) Test circuit implemented in Saber® simulator for C-V characteristics

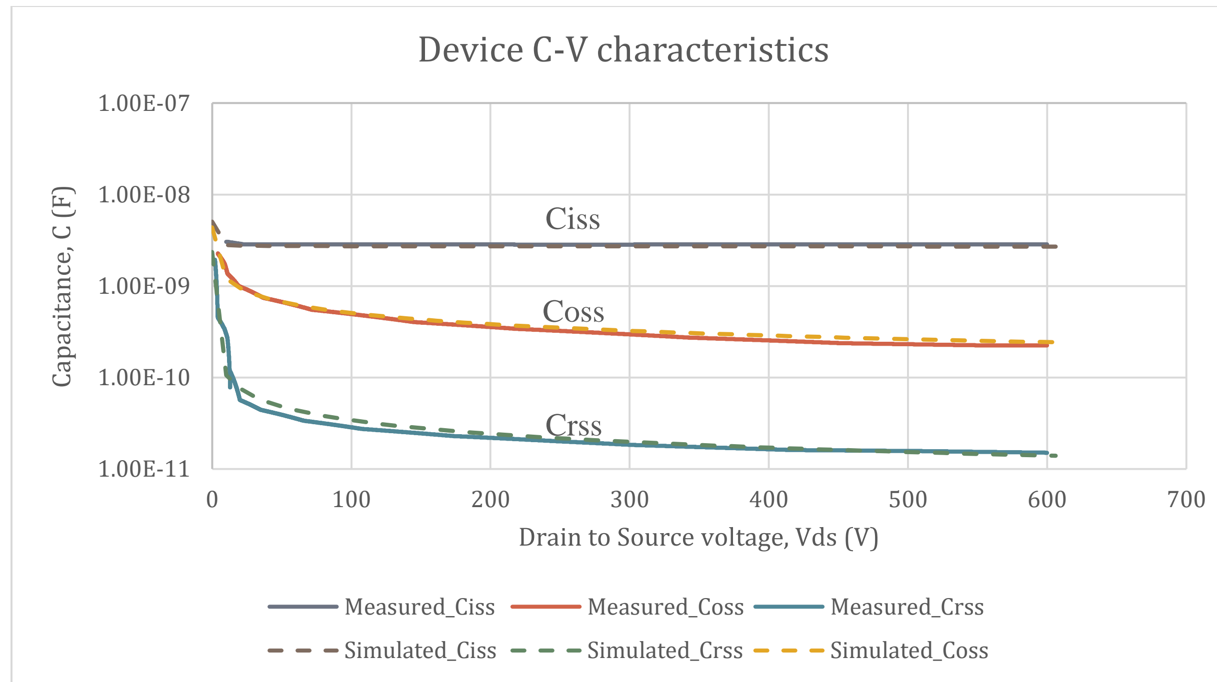


Fig. 1 (b) Simulated and datasheet C-V characteristics for C2M0025120D CREE device

2) Device Transfer Characteristics

The parameters which must be adjusted to fit the I_d-V_{gs} characteristics are listed below:

r_s, k_{ph}, k_{pl}, and v_t

Fig. 2(a) shows the test schematic used to simulate the Device Transfer Characteristics and Fig. 2(b) shows the transfer characteristics for the C2M0025120D CREE device and the simulated characteristics after the extraction of the aforementioned parameters. The extraction of the parameters is performed by adjusting the parameters in the appropriate regions of the curve as indicated in the figure [1] and [2].

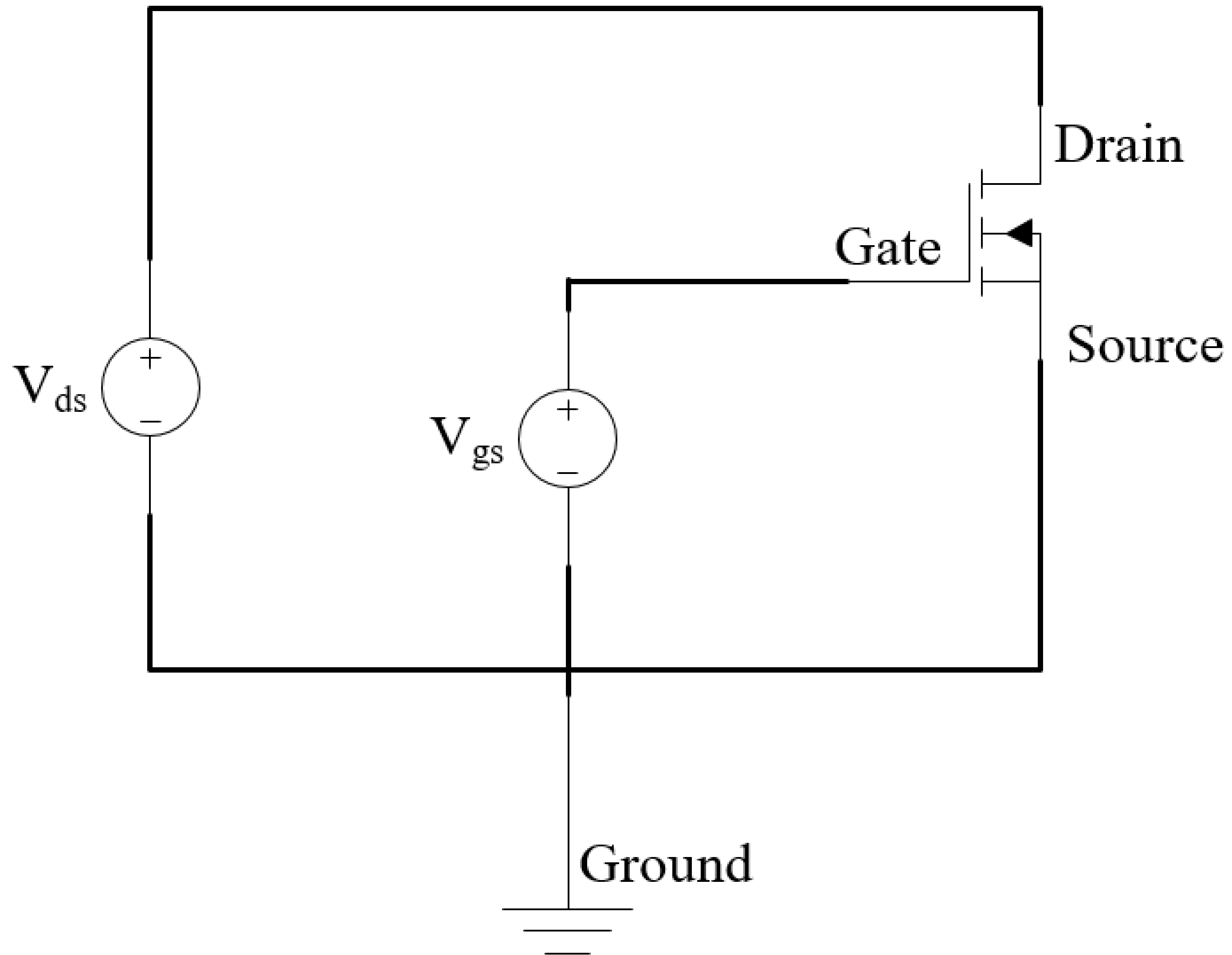


Fig. 2 (a) Test circuit implemented in Saber® simulator for dc characteristics

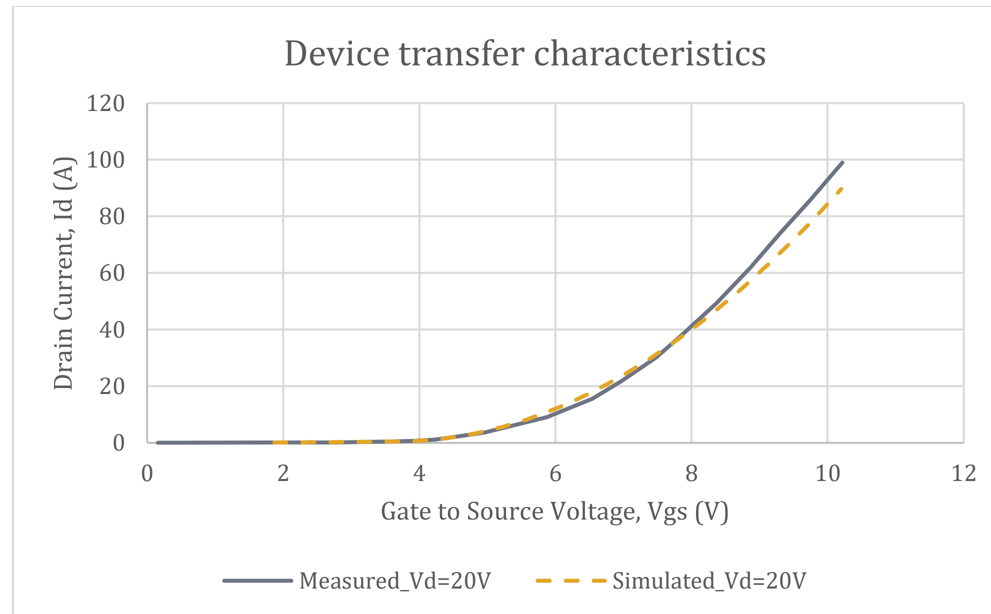


Fig. 2 (b) Simulated and datasheet transfer characteristics for C2M0025120D CREE device

3) Device Output Characteristics:

   The parameters which must be adjusted to fit the output characteristics are listed below:

   k_{fh}, k_{fl}, and p_{vf}

   Fig. 3 shows the output characteristics for the C2M0025120D CREE device and the simulated characteristics after the extraction of the aforementioned parameters. Fig. 3 also shows the regions within the output characteristics which are directly affected by the adjustment of the listed parameters as shown in [2].

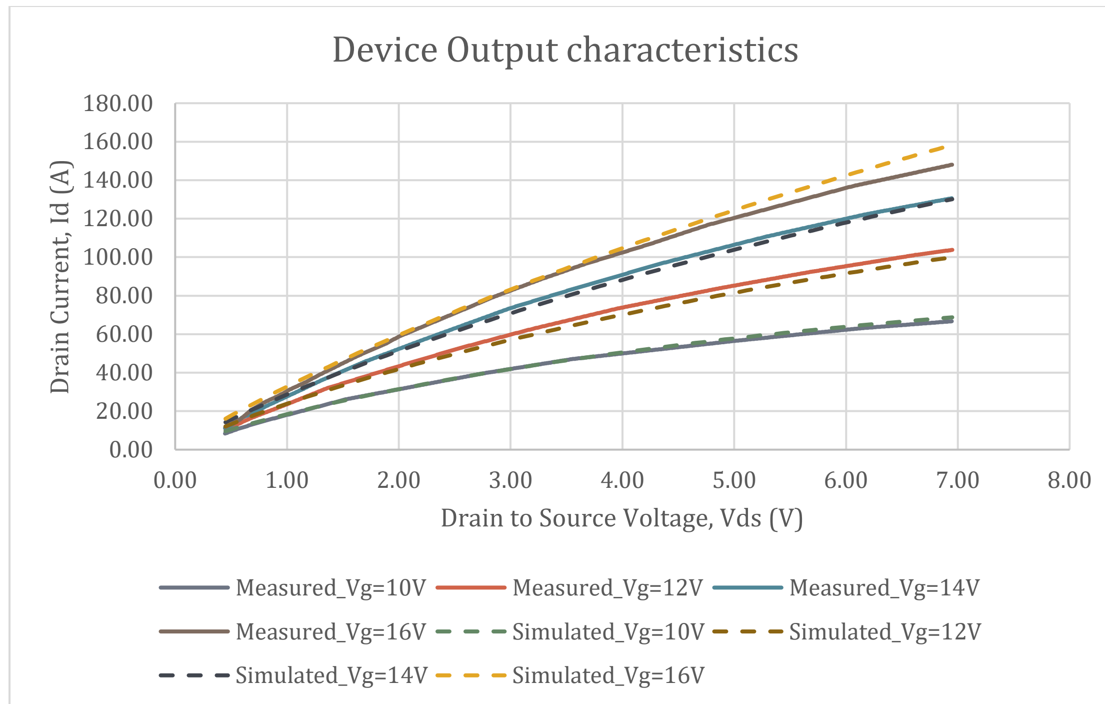


Fig. 3 Simulated and datasheet output characteristics for C2M0025120D CREE device

The described parameter extraction strategy is performed at room temperature, using T = TNOM in the model. To extract the temperature scaling parameters, the same extraction is performed at several temperature increments and the model temperature T is set equal to the simulation temperature in each case. Only the parameters which have temperature scaling are extracted at each temperature, and the rest of the parameters are fixed to their room temperature values. Finally, values for the temperature scaled parameters are obtained at several temperature points. Then, using the temperature scaling equations of the model, the temperature scaling parameters ($kphtexp$, $kpltexp$, $kfhtexp$, $kfltexp$, $thetahtexp$, $thetaltexp$, $vthtco$, $vtltco$) are extracted using the parameter values as function of the temperature.

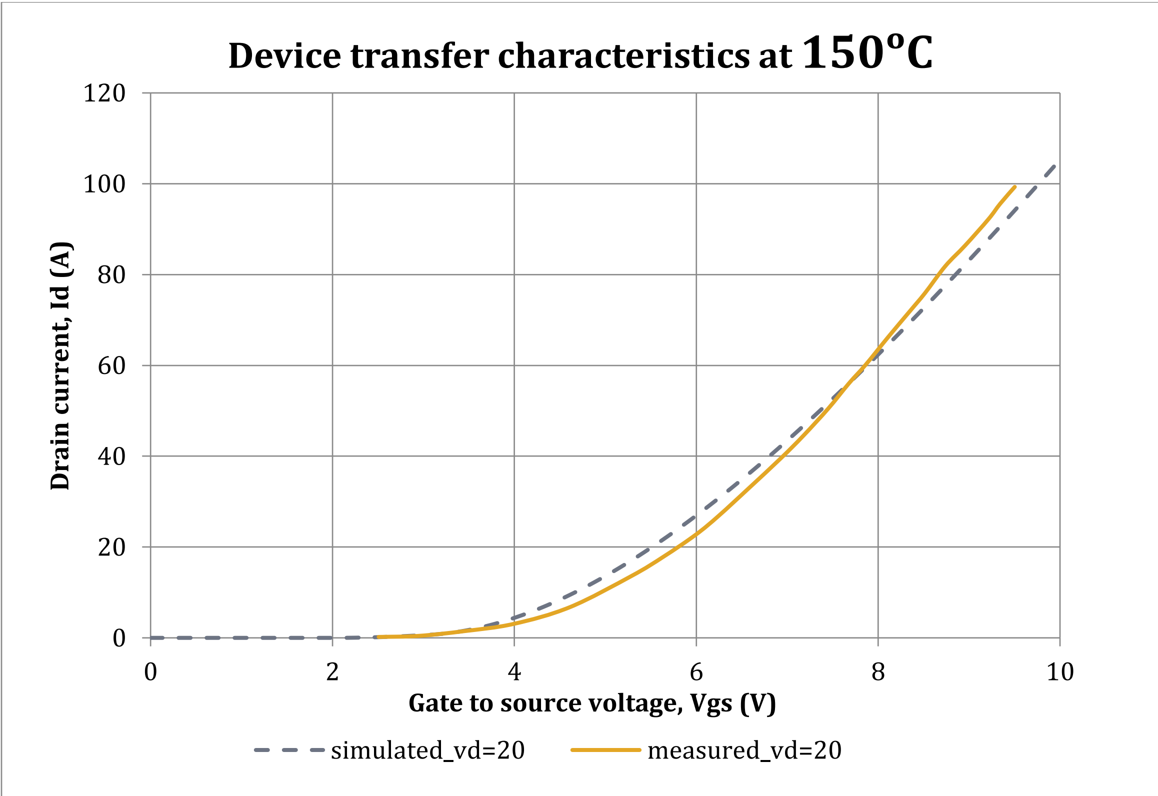


Fig. 4 Simulated and datasheet transfer characteristics for C2M0025120D CREE device at 150°C

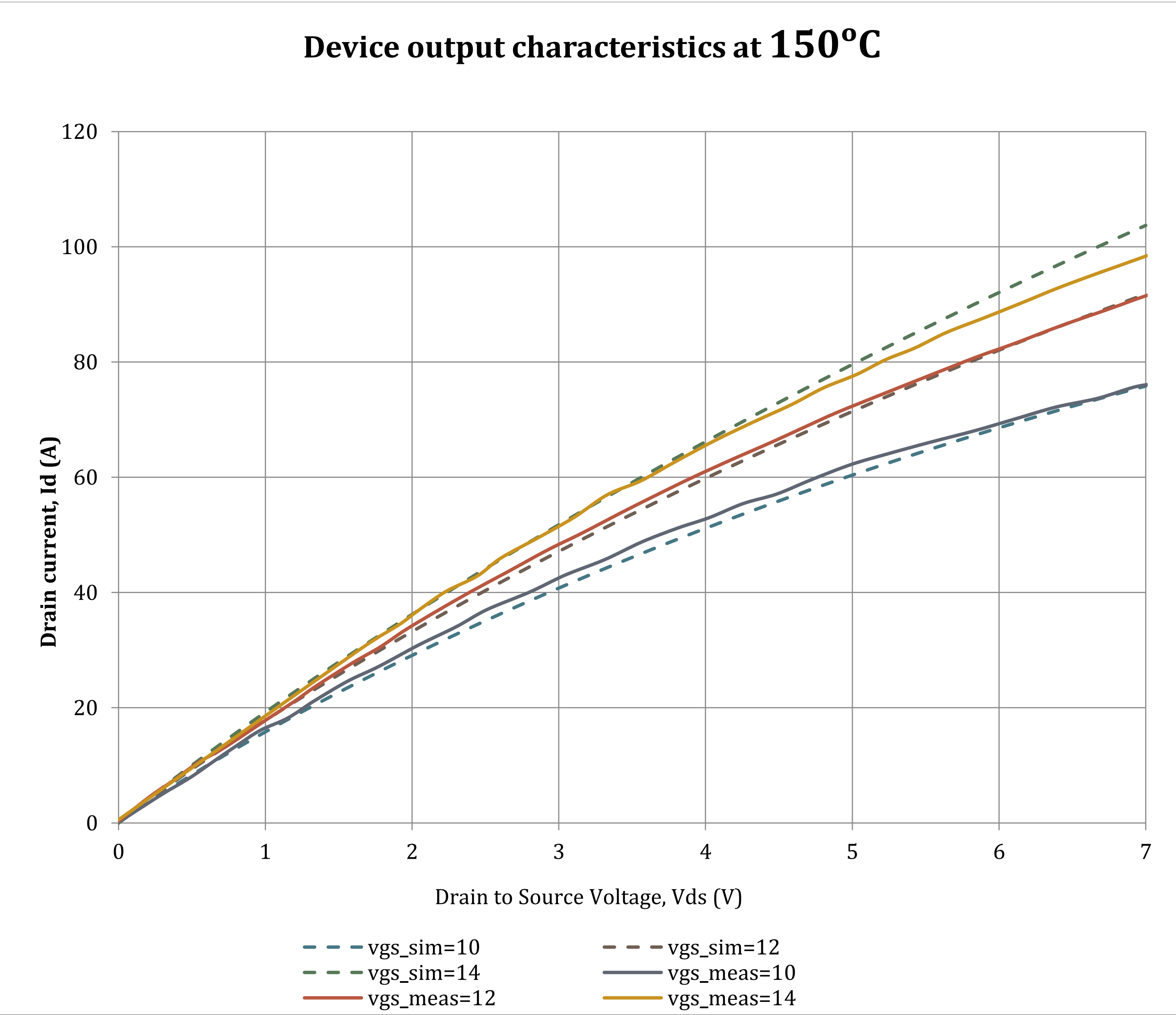


Fig. 5 Simulated and datasheet output characteristics for C2M0025120D CREE device at 150°C

3. Transient Simulation:

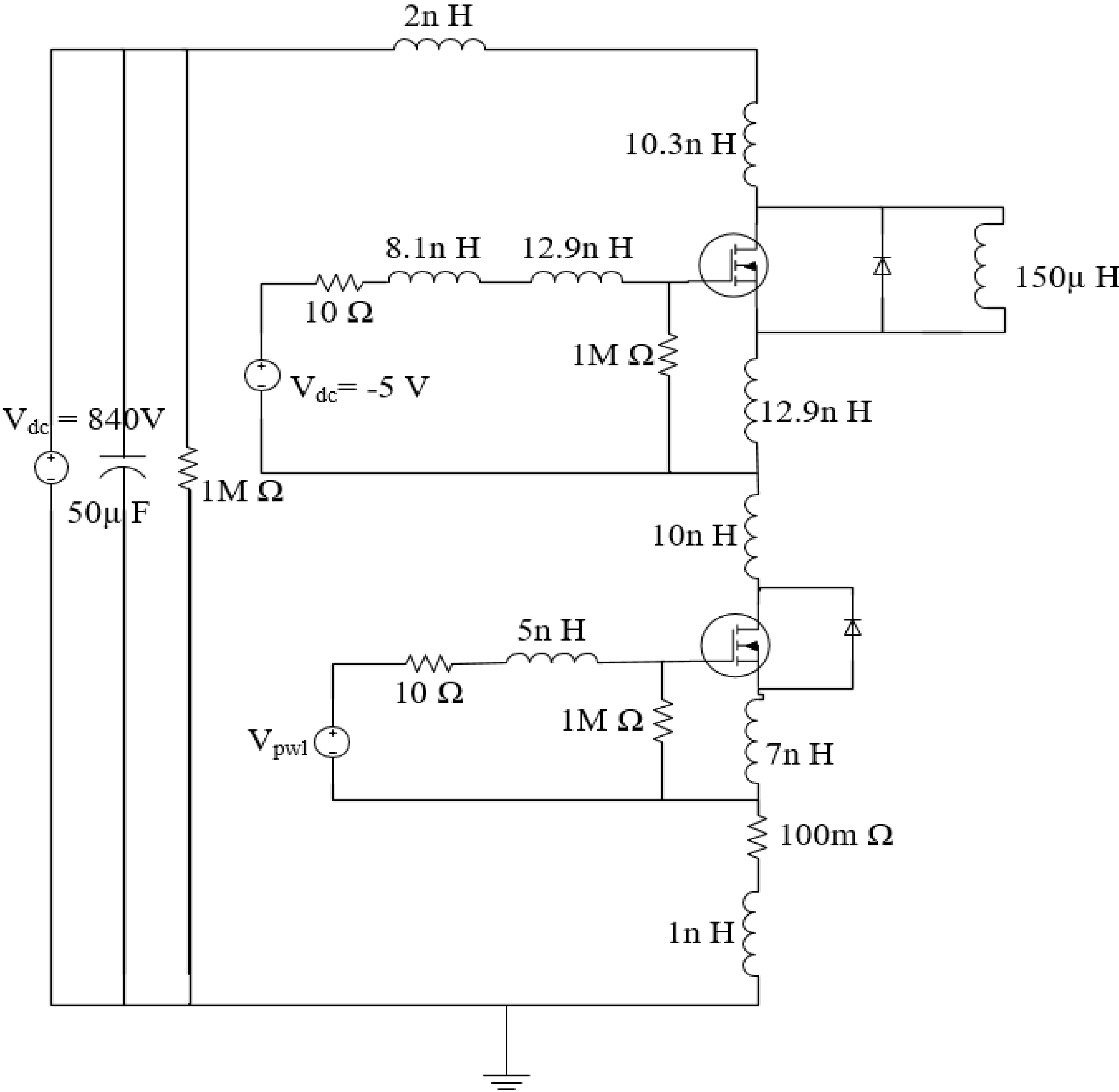


Fig. 6 (a) Double pulse test schematic in Saber®

After the extraction of useful parameters, the model is validated for transient simulations using a double-pulse tester switching circuit as shown in Fig. 6 (a). The dynamic current and voltage characteristics using a clamped inductive load are shown in fig. 6(b) and 6 (c), respectively.

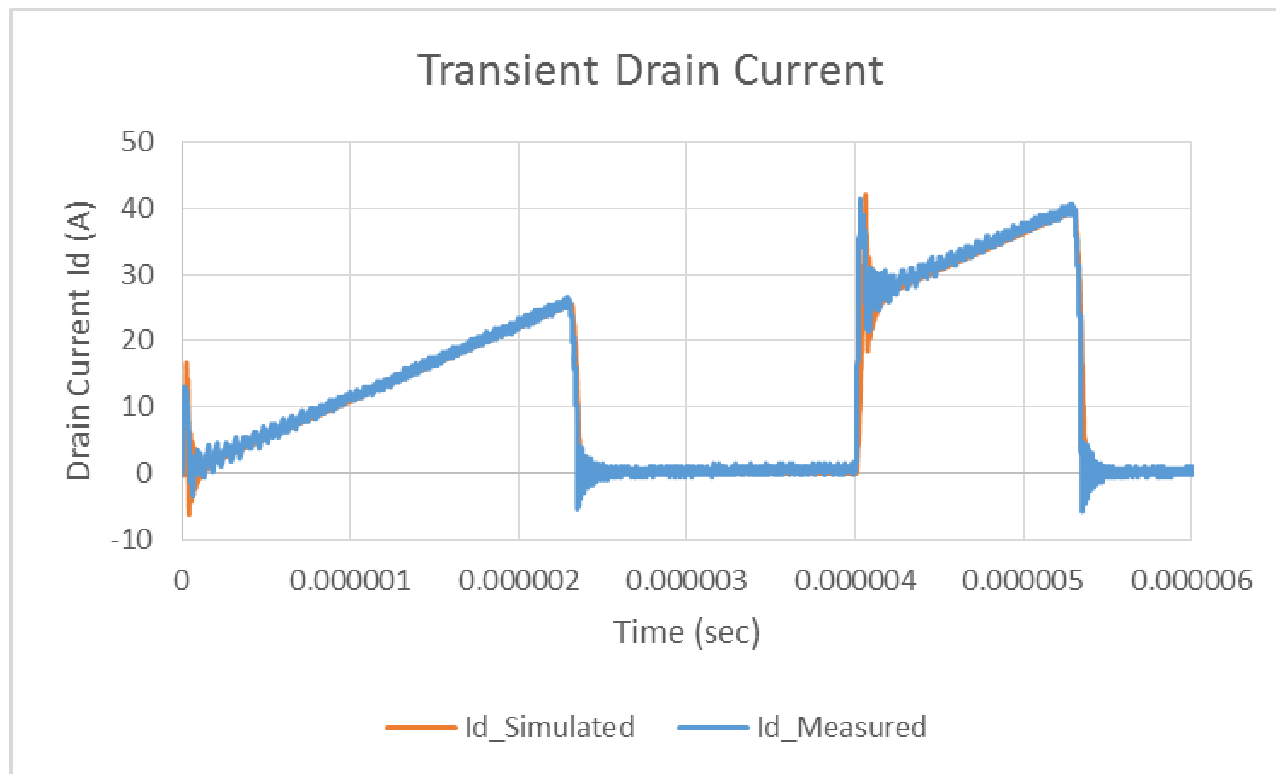


Fig. 6(b) Simulated and measured transient drain current using double pulse tester

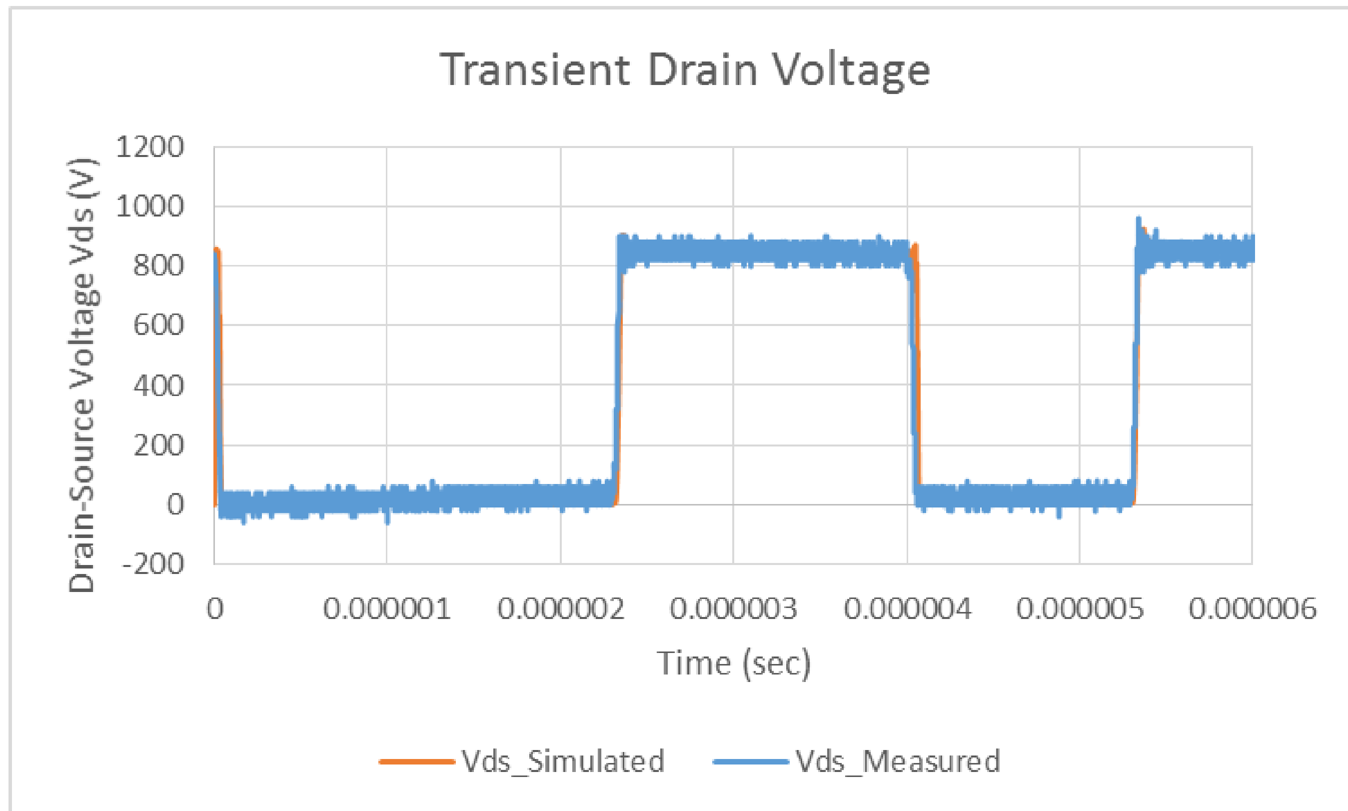


Fig. 6 (c) Simulated and measured transient drain-source voltage using double pulse tester

4. Comparison between Verilog-A and MAST codes

Comparison between Verilog-A and MAST code simulation for I_d-V_{ds}:

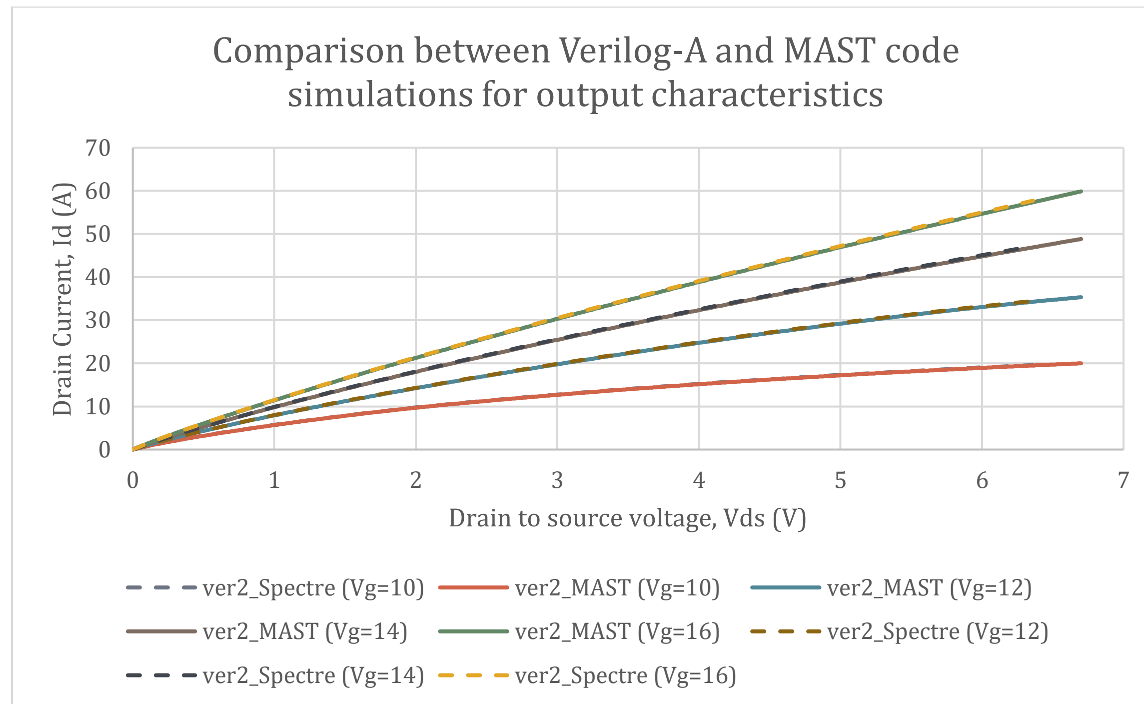


Figure 7(a): I_d-V_{ds} characteristics comparison between Verilog-A and MAST codes

Comparison between Verilog-A and MAST code simulation for I_d-V_{gs}:

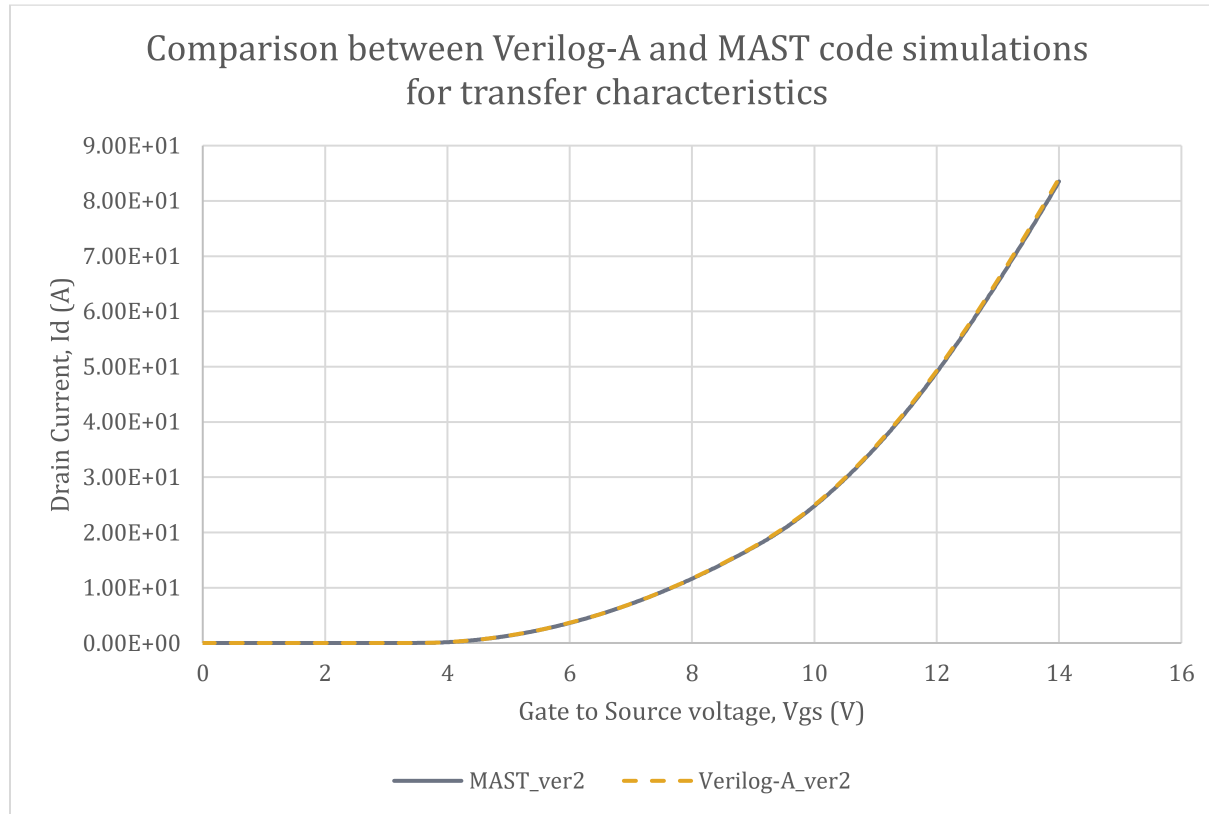


Figure 7(b): Id-V_{gs} characteristics comparison between Verilog-A and MAST codes

Comparison between Verilog-A and MAST code simulation for Input Capacitance (C_{iss}):

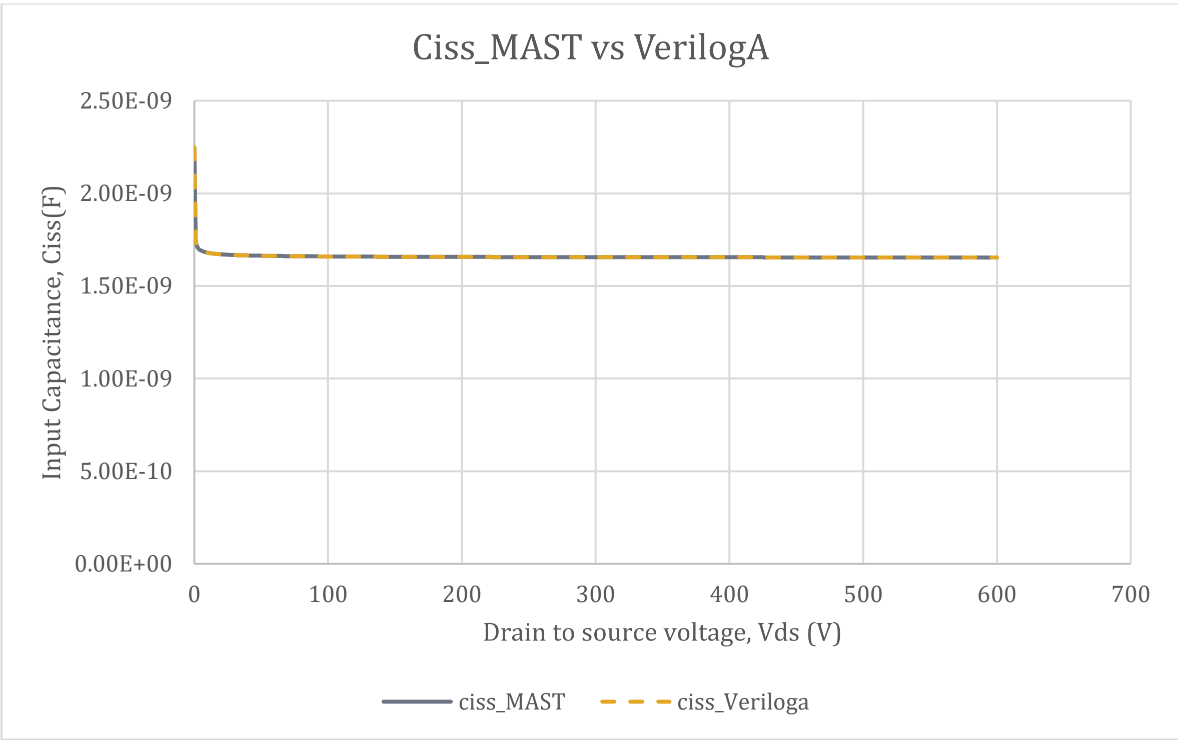


Figure 7(c): Input Capacitance (C_{iss}) characteristics comparison between Verilog-A and MAST

Comparison between Verilog-A and MAST code simulation for Input Capacitance (C_{iss}):

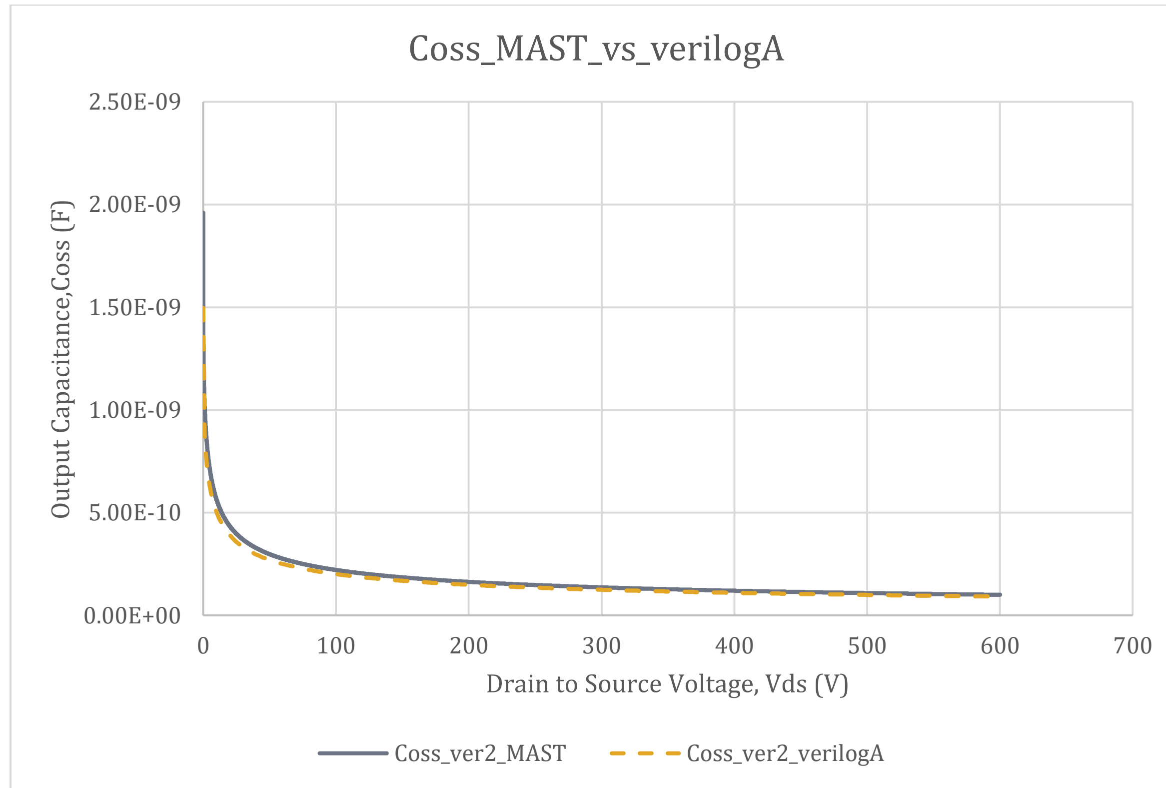


Figure 7(d): Output Capacitance (C_{oss}) characteristics comparison between Verilog-A and MAST

Comparison between Verilog-A and MAST code simulation for Reverse Transfer Capacitance (C_{rss}):

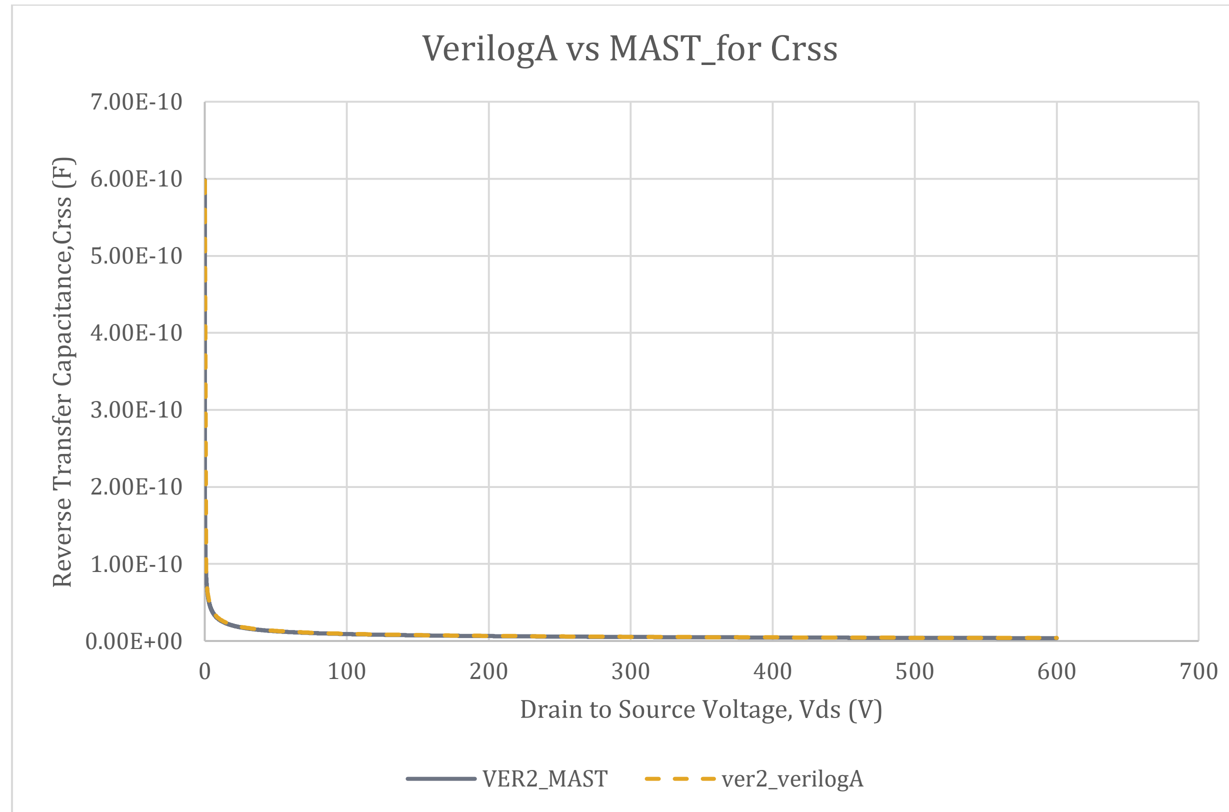


Figure 7(e): Reverse Transfer Capacitance (C_{rss}) characteristics comparison between Verilog-A and MAST

Transient characteristics comparison Verilog-A and MAST codes using double pulse test in Spectre:

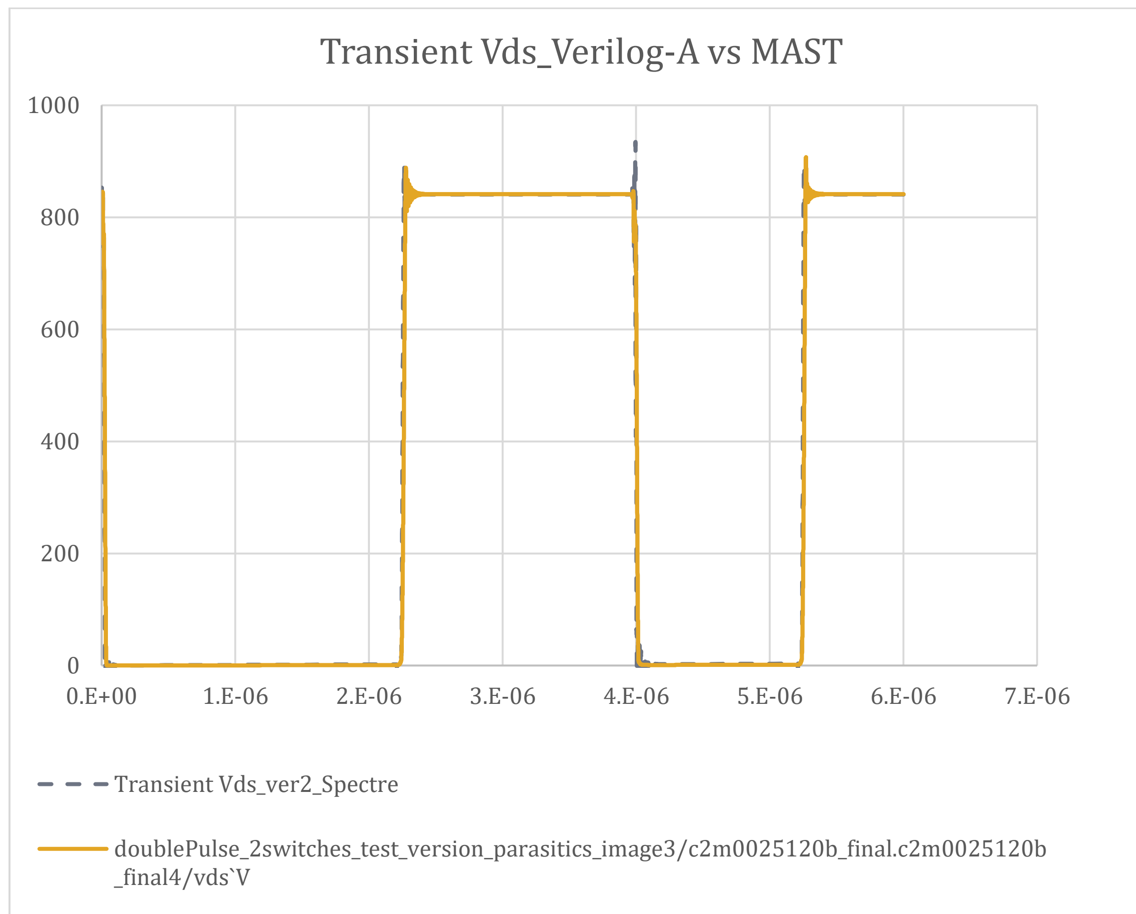


Figure 7(f): Comparison of transient V_{ds} characteristics between MAST in Saber and Verilog-A in Spectre simulations

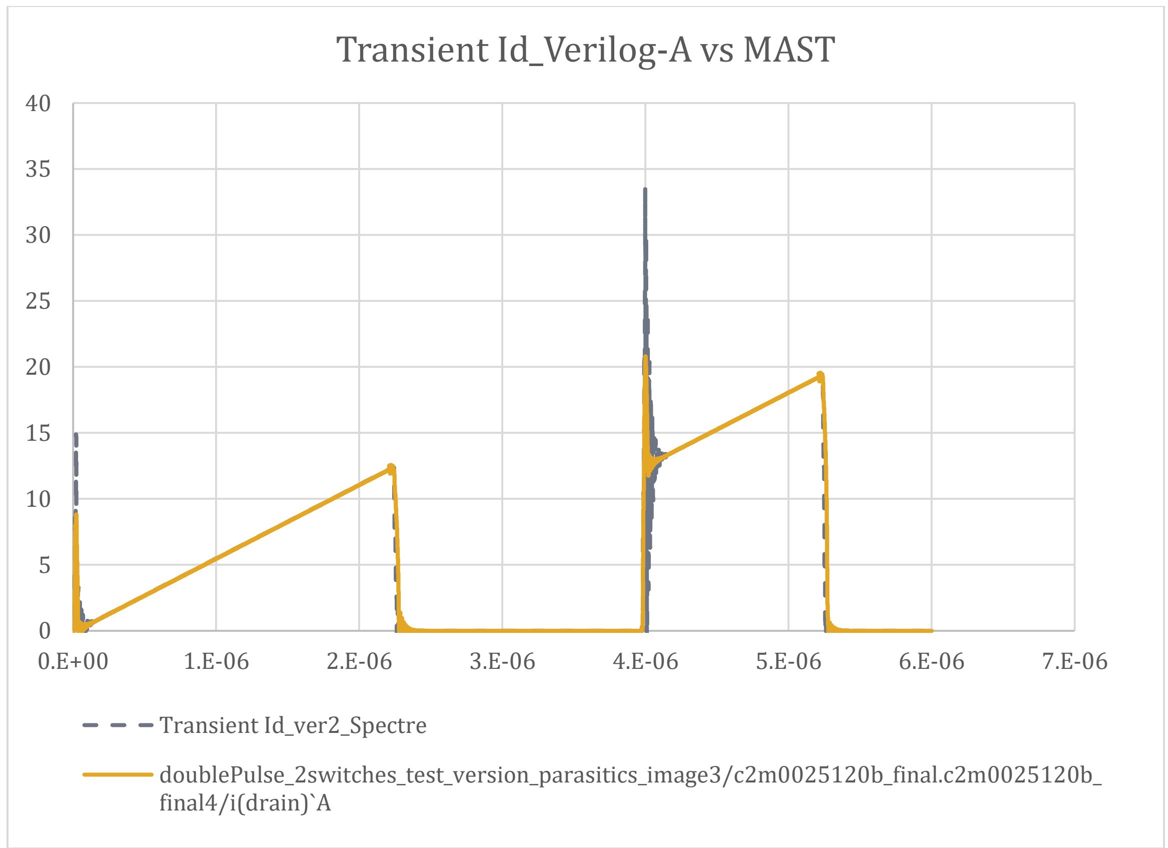


Figure 7(g): Comparison of transient I_d characteristics between MAST in Saber and Verilog-A in Spectre simulations

5. Synchronous mode:

When synchronous mode is activated the model supports both first and third quadrant of MOSFET characteristics. This mode incorporates internal bodydiode of PowerFET.

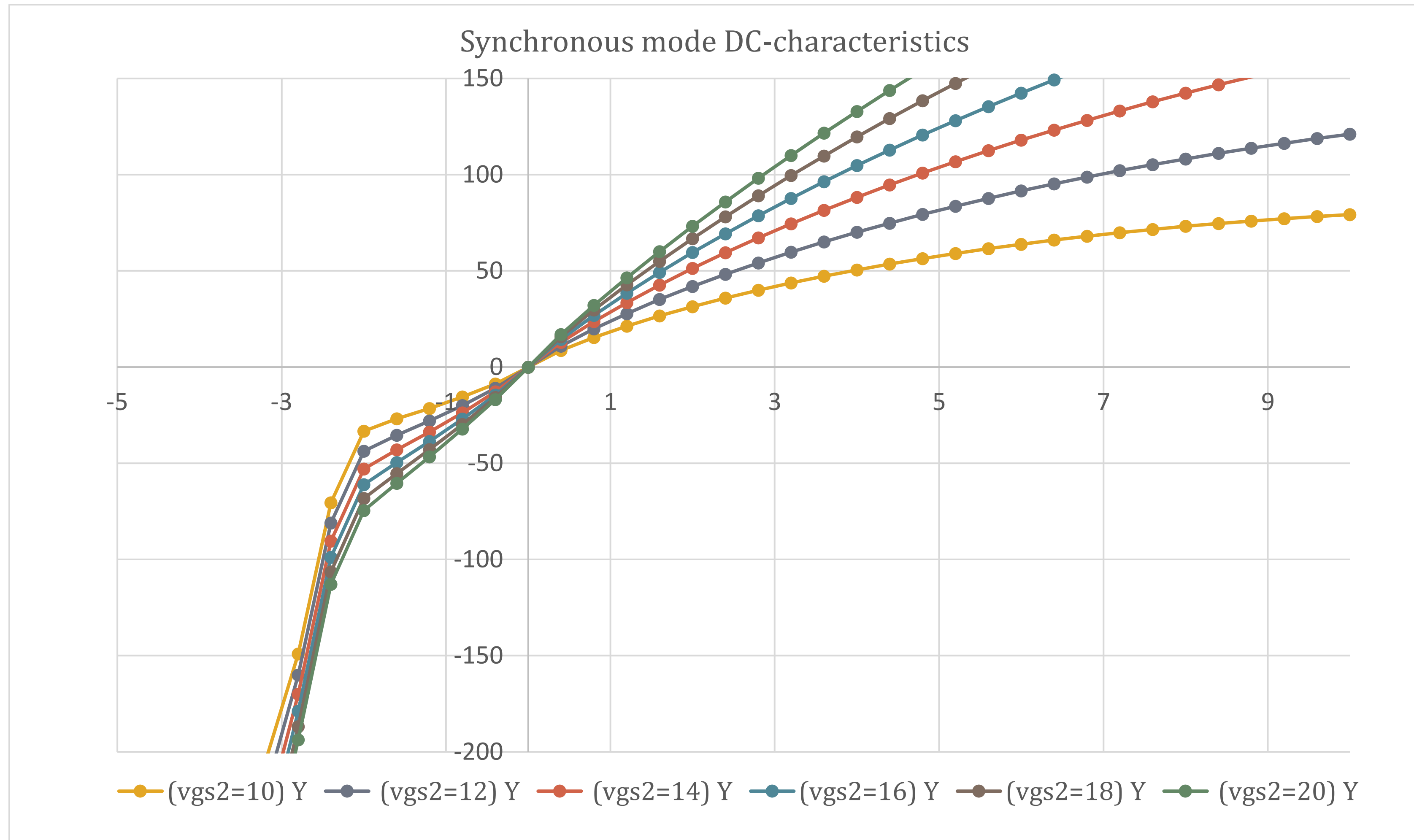


Figure 8: Synchronous mode DC-characteristics for C2M0025120D CREE device at 25°C

6. Parameter list:

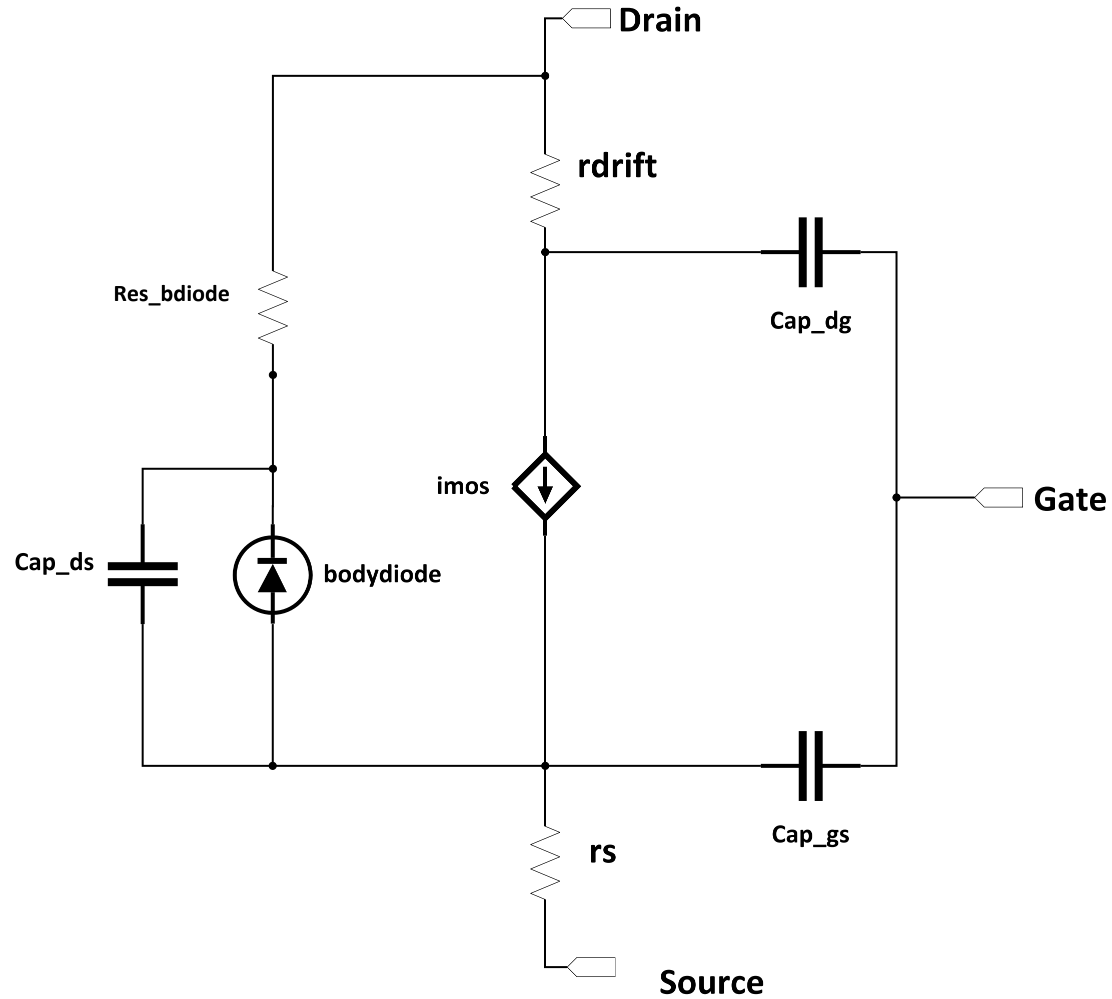
The parameters that were used to build up the PowerFET model are listed below:

Parameter name	Default value	Unit	Comment
Mtrlmod	1		Material type: "0" corresponds to Si and "1" corresponds to SiC
Syncmod	1		Mode type: "0" corresponds to synchronous operation disabled and "1" corresponds to synchronous operation enabled.
cgs	2e-9	F	Gate to source capacitance
cds	2e-9	F	Drain to source zero bias capacitance
cgd0	1e-12	F	Gate drain overlap capacitance
coxd	7e-9	F	Gate oxide capacitance
vtd	10e-3	V	Gate drain overlap depletion threshold voltage
vtdtco	0	V/K	Temp. coefficient of vtd
fc	0		Forward-bias depletion capacitance coefficient
m	440e-3		Junction grading coefficient
wb	150e-6	cm	Metallurgical drift region width
nb	1.4e15	cm^{-3}	Base doping concentration
a	0.1667	cm^2	Device active area
agd	11e-3	cm^2	Gate drain overlap active area
thetal	10e-6		Empirical parameter to model transconductance reduction low gate-source voltage
thetah	10e-6		Empirical parameter to model transconductance reduction for high gate-source voltage

thetaltexp	0		Temperature exponent for thetal
thetahtexp	0		Temperature exponent for thetah
rs	1e-3	Ω	Parasitic drain resistance
kfl	12		Transconductance parameter to scale current in triode region and low threshold voltage region
kfh	5		Transconductance parameter to scale current in triode region and high threshold voltage region
kpl	4.2		Transconductance parameter to scale current in triode and saturation region and low threshold voltage region
kph	80e-3		Transconductance parameter to scale current in triode and saturation region and high threshold voltage region
kfltexp	0		Temp. exponent for kfl
kfhtexp	0		Temp. exponent for kfh
kpltexp	0		Temp. exponent for kpl
kphtexp	0		Temp. exponent for kph
vtl	3.7	V	Low current threshold voltage
vth	32e-3	V	High current threshold voltage
vtltco	0	V/K	Temp. coefficient of vtl
vthtco	0	V/K	Temp. coefficient of vth
vbigd	0.1	V	Gate-drain neck region built-in potential
pvf	440e-3		Pinch-off voltage parameter to adjust drain-source saturation voltage
fxjbe	0.5	F/cm^2	Fraction depletion charge at gate-drain overlap edge
fxjbm	0.75	F/cm^2	Fraction depletion charge at gate-drain overlap middle
slmin	1e-9	A/V	Minimum slope for MOSFET current
id0	0	A	Leakage current at breakdown voltage
vb	1330	V	Breakdown voltage of the device
tnom	27	℃	Nominal temperature
rd	13e-3	Ω	Parasitic drain resistance
rdvd	0	Ω/V	Drain voltage coefficient of drift resistance
rdvg11	0	Ω/V	First gate voltage coefficient of drift resistance
rdvg12	1.0	Ω/V	Second gate voltage coefficient of drift resistance

rdtemp1	0	Ω/K	First temperature coefficient of rd
rdtemp2	0	Ω/K	Second temperature coefficient of rd
rdvdtemp1	0	Ω/V.K	First temperature coefficient of rdvd
rdvdtemp2	0	Ω/V.K	Second temperature coefficient of rd
kvsg1	0	1/V	Gate bias dependent first body diode parameter
kvsg2	0	1/V	Gate bias dependent second body diode parameter
nd	1.0		Emission coefficient of body diode

7. Symbolic equivalent circuit of the model:



8. Equations:

The equations that have been used in the model are given below:

Permittivity, intrinsic carrier concentration and mobility calculation for Si

$$eps = eps0 \times epsrsi$$

$$ni = \frac{3.88 \times 10^{16} \times (temperature)^{1.5}}{exp\left(\frac{7000}{temperature}\right)}$$

$$mun = \frac{5.1 \times 10^{18} + 92 \times nb^{0.91}}{(3.75 \times 10^{15} + nb^{0.91}) \times \left(\frac{300}{temperature}\right)^{2.5}}$$

Permittivity, intrinsic carrier concentration and mobility calculation for SiC

$$eps = eps0 \times epsrsic$$

$$ni = \frac{1.7 \times 10^{16} \times temperature^{1.5}}{e^{\frac{2.08 \times 10^{4}}{temperature}}}$$

$$mun = \frac{947}{\left(1 + \left(\frac{nb}{1.94 \times 10^{17}}\right)^{0.61}\right) \times \left(\frac{temperature}{300}\right)^{-2.15}}$$

Voltage definition

$$Drain\ to\ internal\ drain\ voltage, vddnr = V(res_drain)$$

$$Internal\ drain\ to\ internal\ source\ voltage, vdnrsnr = V(imos_intrinsic)$$

$$Internal\ source\ to\ source\ voltage, vsnrs = V(res_source)$$

$$gate\ to\ internal\ source\ voltage, vgsnr\ = V(cap_gs)$$

$$Gate\ to\ internal\ drain\ voltage, vgdnr = V(cap_gd)$$

$$Drain\ to\ source\ voltage, vds = vddnr + vdnrsnr + vsnrs$$

$$Internal\ drain\ to\ gate\ voltage, vdnrg = (-1) \times vgdnr$$

$$Voltage\ across\ bodydiode\ resistance, vdiodnr = V(res_bdiode)$$

$$Voltage\ across\ bodydiode, vbdiode = V(cap_ds)$$

Current calculation through parasitic resistance

$$ires_drain\ = \frac{vddnr}{rdrift}$$

$$ires_source\ = \frac{vsnrs}{rs}$$

$$ires_bdiode\ = \frac{vdiodnr}{res_bdiode}$$

Mosfet low current in triode region

$$imosl = \frac{kfl \times kpl \times \left(\begin{array}{c} (vgsnr - vtl) \times vdnrsnr - \\ \left(pvf^{yl-1} \times vdnrsnr^{yl} \times \frac{(vgsnr\ -\ vtl)^{2-yl}}{yl} \right) \end{array} \right)}{1 + thetal \times (vgsnr\ -\ vtl)}$$

Mosfet low current in saturation region

$$imosl = \frac{kpl \times (vgsnr - vtl)^2}{2 \times (1 + thetal \times (vgsnr - vtl))}$$

Mosfet high current in triode region

$$imosh = \frac{kfh \times kph \times \left(\begin{array}{c} (vgsnr - vth) \times vdnrsnr - \\ \left(pvf^{yh-1} \times vdnrsnr^{yh} \times \frac{(vgsnr - vth)^{2-yh}}{yh} \right) \end{array} \right)}{1 + thetah \times (vgsnr - vth)}$$

Mosfet high current in saturation region:

$$imosh = \frac{kph \times (vgsnr - vth)^2}{2 \times (1 + thetah \times (vgsnr - vth))}$$

Total Mosfet current:

$$imos = mode \times \left((imosl + imosh) + slmin \times vdnrsnr \right)$$

In case of synchronous rectification is enabled, mode is negative for third quadrant characteristics.

Bodydiode current:

$$tmp1 = limexp(-vbdiode/(nd \times vth))$$

$$tmp2 = limexp(-(kvsg2 \times vgsnr))$$

$$ibdiode = is_{body} \times tmp2 \times (tmp1 - 1)$$

Drain to source capacitance calculation

$$\mathrm{cdsdep} = \begin{cases} \mathrm{cds} \times \left(\dfrac{\mathrm{vbi}}{\mathrm{vbi} + \mathrm{vbdiode}}\right)^{\mathrm{m}}, & if\ vbdiode + vbi > 0 \\ cdsdep = cds\,, & elsewhere \end{cases}$$

$$qcdsj = \begin{cases} cds \times vbi^{m} \times \dfrac{(vbi + vbdiode)^{(1-m)} - vbi^{(1-m)}}{(1-m)}, & if\ vbdiode + vbi > 0 \\ qcdsj = cdsdep \times vbdiode, & elsewhere \end{cases}$$

Two-phase gate to drain capacitance calculation

$$wgdj = \begin{cases} 0, & if\ vdnrg + vtd \leq 0 \\ \sqrt{2 \times eps \times \dfrac{vdnrg + vtd}{q * nb}}, & elsewhere \end{cases}$$

$$cgd = \begin{cases} coxd, & if\ vdnrg + vtd \leq 0 \\ coxd \times \dfrac{cgdj}{coxd + cgdj}, & elsewhere \end{cases}$$

$$qcdg = \begin{cases} coxd \times vdnrg, & if\ vdnrg + vtd \le 0 \\ cgd \times vdnrg, & elsewhere \end{cases}$$

Gate to source charge, $qcgs = cgs * vgsnr$

Datasheet capacitance definitions

$$ciss = cgd + cgs$$
$$coss = cgd + cdsdep$$
$$crss = cgd$$

Temperature scaling equations

$$tdiff = temperature - tnom$$

$$tratio = \frac{temperature}{tnom}$$

$$k(temperature) = k(tnom) \times tratio^{-ktexp}$$

$$theta(temperature) = theta(tnom) \times tratio^{thetatexp}$$

$$vt(temperature) = vt(tnom) + tdiff \times vtco$$

9. People Involved

1) Mihir Mudholkar
2) Shamim Ahmed
3) Ty McNutt
4) Ramchandra Kotecha
5) Arman-Ur-Rashid
6) Mr. Tom Vrotsos
7) Prof. Alan Mantooth