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A sub-1-volt analog metal oxide memristive-based synaptic device with large conductance change for energy-efficient spike-based computing systems

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Nanoscale metal oxide memristors have potential in the development of brain-inspired computing systems that are scalable and efficient. In such systems, memristors represent the native electronic analogues of the biological synapses. In this work, we show cerium oxide based bilayer memristors that are forming-free, low-voltage (∼|0.8 V|), energy-efficient (full on/off switching at ∼8 pJ with 20 ns pulses, intermediate states switching at ∼fJ), and reliable. Furthermore, pulse measurements reveal the analog nature of the memristive device; that is, it can directly be programmed to intermediate resistance states. Leveraging this finding, we demonstrate spike-timing-dependent plasticity, a spike-based Hebbian learning rule. In those experiments, the memristor exhibits a marked change in the normalized synaptic strength (>30 times), when the pre- and post-synaptic neural spikes overlap. This demonstration is an important step towards the physical construction of high density and high connectivity neural networks. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4971188]

A memristor is a two-terminal electronic device, in which a switching layer is sandwiched between two metal electrodes.[1–4] Such devices are important for realizing spike-based hardware learning systems that are capable of processing unstructured, temporal data.[5–10] However, for memristor-based technologies to be viable, it should have a compact nanoscale footprint, operate at a voltage close to 1 V that is compatible with complementary metal oxide semiconductor (CMOS) technology, have reproducible electrical characteristics, and possess high switching speed to minimize the energy consumption.[11] Furthermore, the hardware integration of synaptic connections in advanced neural networks requires memristors with multiple resistive states.[12,13] These are challenging requirements and are difficult to implement without significant innovations.

The phenomenological principle of memristor device operation is based on the change in the physical properties of a conductive filament (associated with the presence of oxygen vacancies) by applying an electric field across the metal oxide switching layer.[14–16] The resulting motion of the oxygen vacancies alters the device resistance between low (Set) and high (Reset) states, depending on the direction and the amplitude of the electric field. So far, a variety of structures from a large set of have been studied in the literature.[4,17,18] The most important finding reveals the trade-off between the switching energy and the data retention time—that is often referred to as voltage-time dilemma.[19] This trade-off is associated with the energy barrier of the device structure. For example, devices made of metal oxides as titanium oxide (TiO_x) generally exhibit low operating voltage and compromised data retention,[20] while devices made of hafnium oxide (HfO_x) demonstrate the opposite.[21] However, the fabrication of devices with bilayer switching stacks has shown to be effective in mitigating this trade-off. In particular, the improvement in data retention was obtained by the incorporation of an ultra-thin metal oxide capping layer (for example, aluminum oxide).[22] On the other hand, the addition of a reactive capping metal (for example, titanium, hafnium, etc.) as an oxygen scavenging layer provided a pathway for reducing the operating voltage of the devices.[23,24] Despite significant advances, a sub-1 V memristive device that simultaneously affords built-in analog behavior, energy efficiency on par with a biological synapse, forming-free operation and low device-to-device variations is still elusive.

Here, we have developed a memristive-based synaptic device by engineering the material properties of an HfO_x capping layer in a bilayer structure with a cerium oxide (CeO_x) switching layer. In this structure, the combination of sub-stoichiometric structural properties of the HfO_x capping layer and its enhanced thermal resistivity at nanoscale dimensions leads to the significant improvement in switching behavior of the devices in terms of the operating voltages, device performance uniformity, reproducibility, and reliability. Furthermore, this structure yields an analog resistance state that is inherent. This key attribute enables the implementation of Hebbian learning,[25] validating the plasticity of the synaptic connection.

Our memristor consists of gold bottom electrode, HfO_x/CeO_x switching layer, and aluminum top electrode. The CeO_x layer was reactively evaporated in oxygen plasma ambient at 0.2 mTorr and an average deposition rate of ∼0.06 nm/s. The HfO_x layer was formed by plasma-assisted atomic layer deposition (PE-ALD) using water and tetrakis (dimethylamido) hafnium ($Hf(NMe_2)_4$) precursors. The film optimization involved varying a wide range of deposition conditions. The optimal HfO_x capping layer was deposited at 200 °C. The pulse width of the hafnium precursor was 0.25 s and the hold time between each pulse was 5 s. Devices were isolated using a wet etching process by first patterning the HfO_x film in the buffered oxide etch followed by removing the CeO_x layer in a mixture of hydrochloric acid, potassium hexacyanoferrate, and de-ionized water. The total thickness of the bilayer switching layer in all experiments was kept at

20 nm, while varying the thickness of the HfO_x and CeO_x layers. Fig. 1(a) conceptually illustrates the effect of the engineered HfO_x capping layer on the concentration of oxygen vacancies in the CeO_x switching layer. X-ray photoelectron spectroscopy (XPS) was performed to guide the development of the bilayer structure (see supplementary material). Fig. 1(b) shows the Hf 4f spectrum of the engineered HfO_x capping layer, revealing the sub-stoichiometric nature of the film. The data indicate the presence of Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks at 16.32 eV and 18.03 eV, respectively—which is consistent with the previous reports in the literature.[26,27] Metallic Hf was also found in the engineered HfO_x layer, evident from the peak at 15.02 eV. The chemical composition of the HfO_x was quantified using the Casa XPS software, in which x was found to be about 1.75.

Fig. 1(c) shows the Ce 3d XPS spectra of the CeO_x switching layer with and without the engineered HfO_x capping layer. In these experiments, the CeO_x and HfO_x layers were 20 nm and 0.8 nm, respectively. The thickness of the HfO_x was kept thin to allow the X-ray beam to penetrate into the underlying CeO_x layer and thus to improve the signal-to-noise ratio of the Ce 3d spectrum. The bilayer structure exhibits discernable u′ and v′ peaks, respectively, at 904 eV and 885 eV (Refs. 28–30) that are absent in the spectrum of the CeO_x layer with no HfO_x capping layer. The u′ and v′ peaks signal the reduction of the Ce^{4+} to Ce^{3+} states,[29,30] which can be translated to the formation of excess oxygen vacancies at regions near the HfO_x/CeO_x interface. This finding is consistent with the first-principle simulations of the HfO_x/CeO_x bilayer in Ref. 31. The marked increase of the oxygen vacancy concentration in the bilayer structure permits the formation of the conductive filament using a smaller electric field, thereby enabling the low-voltage operation of the bilayer structure. Fig. 1(d) shows the representative dc current-voltage characteristics of two CeO_x-based devices with and without the engineered HfO_x capping layer, demonstrating significant reduction of the Set voltage to below 0.8 V.

In a memristive device, the transition from low to high resistance states occurs as the polarity of the electric field across the device is reversed. As the reverse electric field increases, the oxygen anions in the conductive filament begin to disperse through drift and diffusion processes.[10] Considering the similar thickness of the switching layer in Fig. 1(d), the improved Reset voltage of the bilayer device may be explained by the locally enhanced diffusion of oxygen vacancies. We infer that the enhanced thermal resistivity of HfO_x at nanoscale dimensions amplifies Joule heating in the CeO_x switching layer, thereby accelerating the dispersion of oxygen anions at a lower electric field. To elucidate this concept, we performed numerical heat transfer analysis using the COMSOL simulator for two devices in Fig. 1(e) at the bias of −0.6 V. The simulation results indicate significant enhancement of Joule heating in the bilayer structure. We used the measured electrical parameters of the layers in simulation, while the thermal parameters were obtained from the literature.[28,32–36]

Low device variability is critical for implementing large neural networks with high density of memristive synaptic connections. Therefore, we statistically examined the effect of the HfO_x thickness on the important device parameters: Set, Reset, and forming voltages. In these experiments, the HfO_x thickness was varied, while keeping the total thickness

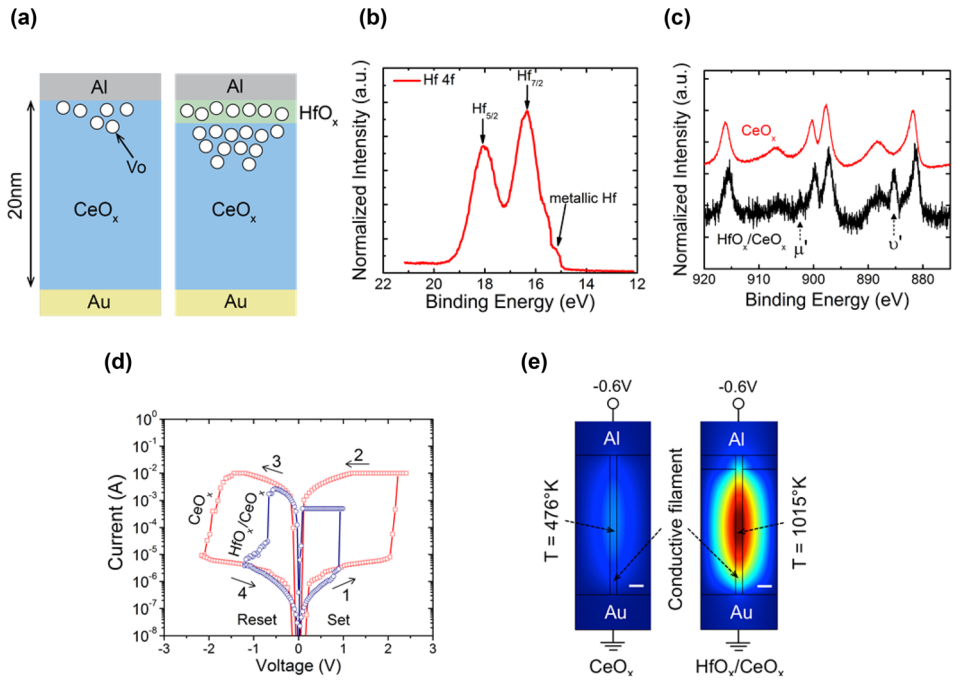

FIG. 1. Improving memristor device characteristics using an engineered sub-stoichiometric HfO_x capping layer. (a) Schematic structure of two memristors with and without the engineered HfO_x, conceptually illustrating the increase of the oxygen vacancy density in the CeO_x switching layer. This attribute of the bilayer memristor results in the forming-free operation and the reduction of the Set voltage. XPS spectra of the (b) engineered HfO_x and (c) CeO_x films with and without the HfO_x capping layer. The XPS studies indicate the increase of the oxygen vacancy concentration in the CeO_x film capped with the oxygen-deficient HfO_x layer. (d) Representative current-voltage characteristics of two memristors, indicating the sub-1 V operation of the bilayer memristive device. (e) Heat transfer simulations illustrate the enhanced Joule heating in the bilayer structure, causing the marked reduction of the Reset voltage (scale bars are 2 nm). The observed increase in Joule heating arises from the high thermal resistivity of HfO_x at nanoscale. The thickness of HfO_x is 2 nm and the total thickness is 20 nm.

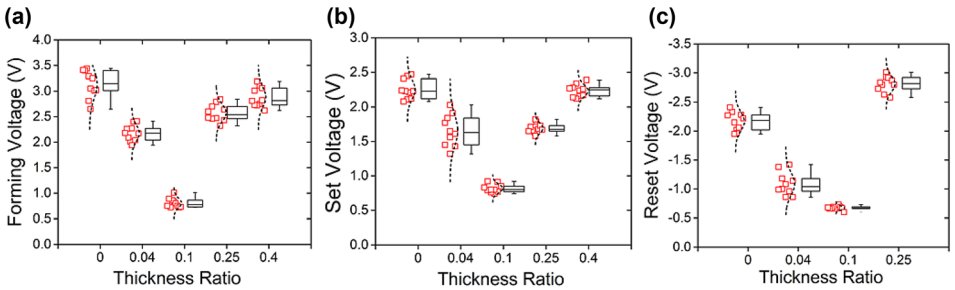

FIG. 2. Effect of HfO_x thickness ratio on the memristor device behavior. The data indicate that the optimal device characteristics, (a) forming voltage, (b) Set voltage, and (c) Reset voltage, occurs at the thickness ratio of about 0.1. Moreover, the device-to-device variation is reduced at this optimal thickness ratio. The equivalency of the forming and Set voltages at the optimal thickness ratio confirms the forming-free operation of the device. Each data point represents a device from 100-cycle average.

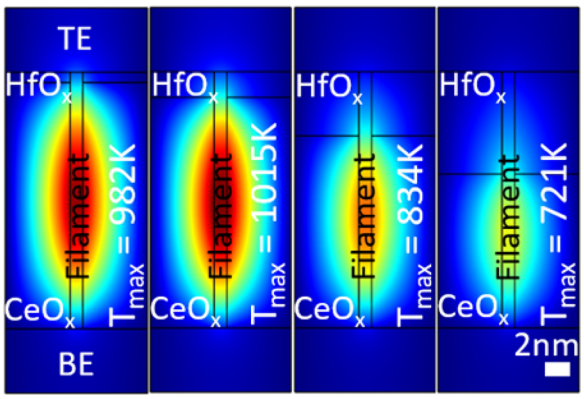

FIG. 3. Effect of HfO_x film thickness on Joule heating. Numerical heat transfer simulation results for several bilayer HfO_x/CeO_x structures with varying HfO_x to total thickness ratio at the bias voltage of −0.6 V. The total thickness of the HfO_x/CeO_x stack was kept at 20 nm. The Joule heating begins to diminish as the thickness of the HfO_x was increased, which arises from the thickness dependence of the HfO_x thermal conductivity.[36]

of the bilayer stack fixed at 20 nm. We defined the thickness ratio as the HfO_x thickness to the total thickness of the bilayer. The data in Fig. 2 indicate that the insertion of an HfO_x capping layer with the optimal thickness ratio of about 0.1 significantly improves the uniformity of the key device parameters. Interestingly, this optimal thickness ratio also coincides with the minimum operating voltages of the bilayer structure. We surmise that the HfO_x film begins to act as an independent switching layer beyond this optimal thickness ratio, resulting in a significant increase in both the device operating voltages and the device variability.

A fresh memristive device generally requires an initial formation of a conductive filament using a relatively large electric potential (known as the forming voltage) before the device can operate at normal Set and Reset voltages. Our bilayer HfO_x/CeO_x device is free from such a limitation, exhibiting forming-free behavior; i.e., the Set voltage is adequate to form the conductive filament in a fresh memristive device (see Figs. 2(a) and 2(b)). This characteristic is attributed to the efficacy of the HfO_x capping layer in creating sufficiently high concentration of excess oxygen vacancies in the CeO_x switching layer.

In Fig. 2(c), the Reset voltage begins to increase as the HfO_x film becomes thicker and the Reset voltage at the thickness ratio of 0.4 becomes significantly large and thus was not included. Fig. 3 shows the heat transfer simulations for devices with varying HfO_x/CeO_x thickness ratio, in which the total thickness of the HfO_x/CeO_x stack was 20 nm. The peak temperature value was found to be the highest when the thickness ratio was about 0.1. The simulation results suggest that capping with a sufficiently thin layer of HfO_x enhances the Joule heating, owing to the pronounced thermal resistivity of HfO_x at nanoscale. However, as the thickness of the HfO_x increases, the Joule heating begins to diminish, which is consistent with the thickness dependence of the HfO_x thermal conductivity.[36] The enhanced Joule heating effect in the optimal structure is therefore expected to enhance the diffusion of the oxygen vacancies during the Reset process, thereby reducing the Reset voltage.

The bilayer structure exhibits excellent switching reliability at the thickness ratio of 0.1, which conceivably stems from the reduced operating voltage of the device. In Fig. 4(a), the optimal memristor bilayer structure survives more than 2×10^5 cycles of programming (endurance test).

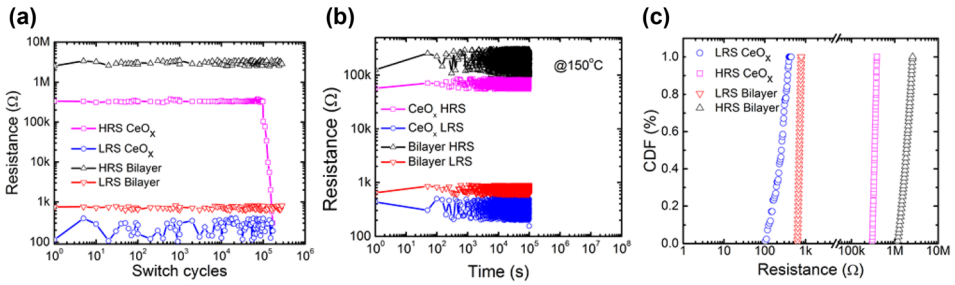

FIG. 4. Device reliability studies. (a) The endurance test results for the CeO_x and the optimal HfO_x/CeO_x devices. In addition to the improved endurance properties, the bilayer device exhibits larger HRS and LRS values compared to the device with no HfO_x. The increase in the LRS and HRS values is favorable for reducing the switching power consumption of the bilayer device. (b) The accelerated retention test for the CeO_x and the HfO_x/CeO_x devices measured at 150 °C at constant stress voltage of +0.2 V. The results indicate the projected data retention of 10 years for both devices. (c) Representative CDF plot of the cycle-to-cycle programming characteristics for two devices with and without the engineered HfO_x layer.

The accelerated retention test in Fig. 4(b) indicates the projected data retention of 10 years for the bilayer devices (see supplementary material). The cumulative distribution function (CDF) in Fig. 4(c) indicates the improved uniformity of the on-state performance between programming cycles of the same bilayer device, while the off-state characteristic of the device appears to have been degraded, perhaps due to the non-uniformity of the Joule heating effect. The bilayer device exhibits average low- and high-resistance states (LRS and HRS) of about 600 Ω and 2.8 MΩ that are larger than those of the device with no HfO_x capping layer by factors of 4 and 10, respectively. The resulting decrease of operating current is beneficial for reducing the switching power consumption during the Set and Reset operations.

One transistor and one memristor (1T-1R) is a popular approach for implementing multi-state memory function.[37] However, 1T-1R limits the memristor integration density because of area overhead by implementing transistor as well as the need for a complicated driver circuit in order to independently control each transistor. To circumvent these practical issues, the multi-state characteristic must be inherent to the two-terminal memristive device itself. Figs. 5(a) and 5(b) illustrate the pulse measurement results for a bilayer device (with the optimal 0.1 thickness ratio, $500 \times 500\,nm^2$), indicating the gradual change in the conductance of the filament between the fully on and off states. The observed resistive states are inherent to the device because no current compliance limit was used. Interestingly, the bilayer device also exhibits weak voltage-time dependence for pulses shorter than a few microseconds, which could be attributed to the dominant effect of the HfO_x capping layer on the device switching behavior. The full on/off energy consumption during Set and Reset steps was calculated to be, respectively, 8.7 and 1.6 pJ by time integral of transient voltage and current waveforms (see supplementary material Fig. S2). Considering the analog characteristic of the resistive states together with the large HRS to LRS ratio in excess of 10^3, the energy consumption for switching between the intermediate resistance states will be much smaller (about tens of fJ, assuming memory states with an increment of 100 Ω; see supplementary material Fig. S3).

The spike-based hardware learning systems have potential to be efficient and compact for processing unstructured

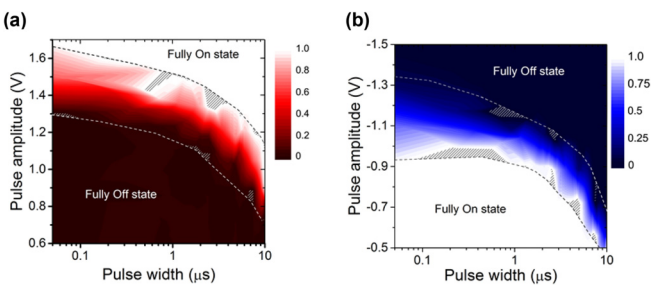

FIG. 5. Analog memory characteristic of the bilayer memristor. The normalized conductance of a bilayer memristor is plotted as a function of pulse widths and amplitudes when the device switches from (a) fully off state to fully on state and (b) fully on state to fully off state. The dashed lines are guide to the eye and the hatched regions denote unmeasured points. The data in (a) and (b) reveal the gradual change in the conductance of the device between the fully off and on states. Full on/off switching energy consumptions of ~2.6 and 2.1 pJ were calculated from the transient **c** Set and **d** Reset voltage and current waveforms, respectively.

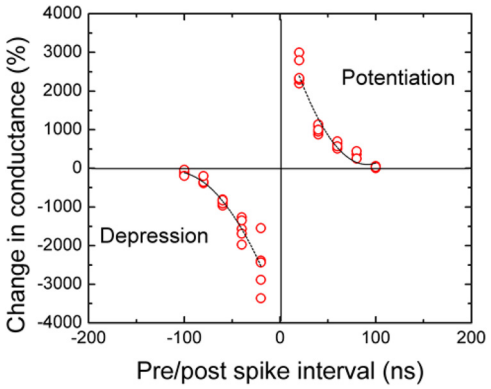

FIG. 6. Implementation of STDP learning using the HfO_x/CeO_x memristive device. (a) Schematic representation of the learning experiment. Two waveforms with identical shapes were applied to the top and bottom electrodes. In the learning experiments, the time intervals between the pre- and post-synaptic spikes were varied in order to probe the synaptic depression ($\Delta t < 0$) and potentiation ($\Delta t > 0$). The positive (negative) time difference indicates that the pre-synaptic spike occurs before (after) the post-synaptic one. (b) The plot clearly indicates the marked change in the synaptic strength as a function of different pre/post spike intervals.

data.[38] In such systems, the learning mechanism follows the spike-based form of Hebbian learning,[25] i.e., Spike-timing dependent plasticity (STDP), in which the change in the strength of the synapse depends on the time difference between the pre- and post-synaptic neural spikes. The waveforms with exponential decays were emulated with a series of square pulses (see supplementary material Figs. S4 and S5). For these experiments, we have chosen an average spike rate of about 1 MHz, which is 10^5 times faster than that of the brain. This corresponds to a time step of ~1 μs for updating the internal state of neurons and calculating the synaptic currents, assuming the neuron spiking probability of 0.01 as in the brain. Fig. 6 shows the plot of the normalized conductance change of the optimal bilayer device as a function of the time difference between the pre- and post-synaptic neural spikes. The data are fitted with the exponential decay functions, confirming an STDP behavior similar to that of a biological synapse. Moreover, the data indicate a remarkable change in the normalized conductance of the device (>30 times) when the pre- and post-synaptic spikes overlap.

In summary, we have demonstrated a bilayer HfO_x/CeO_x memristors by tailoring the structural properties of the nanoscale HfO_x capping layer. The memristive device was implemented using the CMOS-compatible materials and processes. Our device exhibits analog resistance states, sub-1 V operating voltages, high conductance change at fast nanosecond pulses, and energy efficient operation and STDP learning rule was implemented. The salient features of this bilayer structure are promising for hardware implementation of STDP-based learning systems.

See supplementary material for electrical characterization equipment, device geometry for transient test, details of XPS studies, accelerated retention test, switching cycles of intermediate states and generation of waveforms for STDP measurements.

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C.-C.H., D.S., and S.K.B conceived the experiments. C.-C.H. performed device fabrication, electrical and material characterizations, and COMSOL simulations. A.R. contributed to XPS characterizations, and Y.-F.C. contributed to device fabrication and electrical characterizations. All the authors discussed the results. D.S., C.-C.H., and S.K.B co-wrote the paper.

[1]L. O. Chua, "Memristor-the missing circuit element," IEEE Trans. Circuit Theory **18**(5), 507–519 (1971).
[2]D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature **453**(7191), 80–83 (2008).
[3]R. Waser and M. Aono, "Nanoionics-based resistive switching memories," Nat. Mater. **6**(11), 833–840 (2007).
[4]H.-S. P. Wong and S. Salahuddin, "Memory leads the way to better computing," Nat. Nanotechnol. **10**(3), 191–194 (2015).
[5]D. Kuzum, S. Yu, and H. P. Wong, "Synaptic electronics: Materials, devices and applications," Nanotechnology **24**(38), 382001 (2013).
[6]T. Masquelier, R. Guyonneau, and S. J. Thorpe, "Competitive STDP-based spike pattern learning," Neural Comput. **21**(5), 1259–1276 (2009).
[7]Y. F. Chang, B. Fowler, Y. C. Chen, F. Zhou, C. H. Pan, T. C. Chang, and J. C. Lee, "Demonstration of synaptic behaviors and resistive switching characterizations by proton exchange reactions in silicon oxide," Sci. Rep. **6**, 21268–21278 (2016).
[8]S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," Nano Lett. **10**(4), 1297–1301 (2010).
[9]M. Prezioso, F. Merrikh-Bayat, B. Hoskins, G. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," Nature **521**(7550), 61–64 (2015).
[10]J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," Nat. Nanotechnol. **8**(1), 13–24 (2013).
[11]D. Kuzum, R. G. Jeyasingh, S. Yu, and H.-S. P. Wong, "Low-energy robust neuromorphic computation using synaptic devices," IEEE Trans. Electron Devices **59**(12), 3489–3494 (2012).
[12]G. Indiveri, R. Legenstein, G. Deligeorgis, and T. Prodromakis, "Integration of nanoscale memristor synapses in neuromorphic computing architectures," Nanotechnology **24**(38), 384010 (2013).
[13]F. Zhou, Y. F. Chang, B. Fowler, K. Byun, and J. C. Lee, "Stabilization of multiple resistance levels by current-sweep in SiO_x-based resistive switching memory," Appl. Phys. Lett. **106**(6), 063508–063513 (2015).
[14]J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," Nat. Nanotechnol. **3**(7), 429–433 (2008).
[15]K. Kamiya, M. Y. Yang, S.-G. Park, B. Magyari-Köpe, Y. Nishi, M. Niwa, and K. Shiraishi, "ON-OFF switching mechanism of resistive–random–access–memories based on the formation and disruption of oxygen vacancy conducting channels," Appl. Phys. Lett. **100**(7), 073502 (2012).
[16]C.-C. Hsieh, A. Roy, A. Rai, Y.-F. Chang, and S. K. Banerjee, "Characteristics and mechanism study of cerium oxide based random access memories," Appl. Phys. Lett. **106**(17), 173108 (2015).
[17]Y. F. Chang, B. Fowler, Y. C. Chen, and J. C. Lee, "Proton exchange reactions in SiO x-based resistive switching memory: Review and insights from impedance spectroscopy," Prog. Solid State Chem. Prog. Solid State Chem. **44**(3), 75–85 (2016).
[18]D. S. Jeong, R. Thomas, R. Katiyar, J. Scott, H. Kohlstedt, A. Petraru, and C. S. Hwang, "Emerging memories: Resistive switching mechanisms and current status," Rep. Prog. Phys. **75**(7), 076502 (2012).
[19]Y. F. Chang, B. Fowler, F. Zhou, Y. C. Chen, and J. C. Lee, "Study of self-compliance behaviors and internal filament characteristics in intrinsic SiO_x-based resistive switching memory," Appl. Phys. Lett. **108**(3), 033504–033508 (2016).
[20]C. Hu, M. D. McDaniel, A. Posadas, A. A. Demkov, J. G. Ekerdt, and E. T. Yu, "Highly controllable and stable quantized conductance and resistive switching mechanism in single-crystal TiO_2 resistive memory on silicon," Nano Lett. **14**(8), 4360–4367 (2014).
[21]S. Yu, H.-Y. Chen, B. Gao, J. Kang, and H.-S. P. Wong, "HfOx-based vertical resistive switching random access memory suitable for bit-cost-effective three-dimensional cross-point architecture," ACS Nano **7**(3), 2320–2325 (2013).
[22]L. Goux, A. Fantini, G. Kar, Y.-Y. Chen, N. Jossart, R. Degraeve, S. Clima, B. Govoreanuet, G. Lorenzo, G. Pourtois *et al.*, "Ultralow sub-500 nA operating current high-performance $TiNAl_2O_3$ HfO_2 HfTiN bipolar RRAM achieved through understanding-based stack-engineering," in 2012 Symposium on VLSI Technology (VLSIT) (IEEE, 2012).
[23]Y. Y. Chen, L. Goux, S. Clima, B. Govoreanu, R. Degraeve, G. S. Kar, A. Fantini, G. Groeseneken, D. J. Wouters, and M. Jurczak, "Endurance/retention trade-off on cap 1T1R bipolar RRAM," IEEE Trans. Electron Devices. **60**(3), 1114–1121 (2013).
[24]Y. C. Chen, Y. F. Chang, X. Wu, M. Guo, B. Fowler, F. Zhou, C. H. Pan, T. C. Chang, and J. C. Lee, "Characterization of SiO_x/HfO_x bilayer resistive-switching memory devices," ECS Trans. **72**(2), 25–33 (2016).
[25]Y. Dan and M.-m. Poo, "Spike timing-dependent plasticity of neural circuits," Neuron **44**(1), 23–30 (2004).
[26]S. Ban and O. Kim, "Improvement of switching uniformity in HfOx-based resistive random access memory with a titanium film and effects of titanium on resistive switching behaviors," Jpn. J. Appl. Phys., Part 1 **53**(6S), 06JE15 (2014).
[27]W. Scopel, A. J. da Silva, W. Orellana, and A. Fazzio, "Comparative study of defect energetics in HfO_2 and SiO_2," Appl. Phys. Lett. **84**, 1492 (2004).
[28]C. Hardacre, G. M. Roe, and R. M. Lambert, "Structure, composition and thermal properties of cerium oxide films on platinum {111}," Surf. Sci. **326**(1), 1–10 (1995).
[29]T. Hasegawa, S. M. F. Shahed, Y. Sainoo, A. Beniya, N. Isomura, Y. Watanabe, and T. Komeda, "Epitaxial growth of CeO_2 (111) film on Ru (0001): Scanning tunneling microscopy (STM) and x-ray photoemission spectroscopy (XPS) study," J. Chem. Phys. **140**(4), 044711 (2014).
[30]F. ç. Larachi, J. Pierre, A. Adnot, and A. Bernis, "Ce 3d XPS study of composite $Ce_xMn_{1-x}O_{2-y}$ wet oxidation catalysts," Appl. Surf. Sci. **195**(1), 236–250 (2002).
[31]A. A. Bhatti, C.-C. Hsieh, A. Roy, L. F. Register, and S. K. Banerjee, "First-principles simulation of oxygen vacancy migration in HfO_x, CeO_x, and at their interfaces for applications in resistive random-access memories," J. Comput. Electron. **15**, 741–748 (2016).
[32]J. Guy, G. Molas, P. Blaise, C. Carabasse, M. Bernard, A. Roule, G. La Carval, V. Sousa, H. Grampeix, V. Delaye *et al.*, "Experimental and theoretical understanding of forming, SET and RESET operations in conductive bridge RAM (CBRAM) for memory stack optimization," in 2014 IEEE International Electron Devices Meeting (IEDM) (IEEE, 2014).
[33]M. Khafizov, I. W. Park, A. Chernatynskiy, L. He, J. Lin, J. J. Moore, D. Swank, T. Lillo, S. R. Philpot, A. El-Azab *et al.*, "Thermal conductivity in nanocrystalline ceria thin films," J. Am. Ceram. Soc. **97**(2), 562–569 (2014).
[34]S. Menzel, Modeling and simulation of resistive switching devices: Lehrstuhl für Werkstoffe der Elektrotechnik II und Institut für Werkstoffe der Elektrotechnik, 2013.
[35]Y. A. Volkov, L. Palatnik, and A. Pugachev, "Investigation of the thermal properties of thin aluminum films," Zh. Eksp. Teor. Fiz. **70**, 2244–2250 (1976).
[36]M. A. Panzer, M. Shandalov, J. Rowlette, Y. Oshima, Y. W. Chen, P. C. McIntyre, and K. E. Goodson, "Thermal properties of ultrathin hafnium oxide gate dielectric films," IEEE Electron Device Lett. **30**(12), 1269–1271 (2009).
[37]Y. F. Chang, B. Fowler, Y. C. Chen, Y. T. Chen, Y. Wang, F. Xue, F. Zhou, and J. C. Lee, "Intrinsic SiO_x-based unipolar resistive switching memory. I. Oxide stoichiometry effects on reversible switching and program window optimization," J. Appl. Phys. **116**(4), 043708–043718 (2014).
[38]B. Rajendran, Y. Liu, J.-S. Seo, K. Gopalakrishnan, L. Chang, D. J. Friedman, and M. B. Ritter, "Specifications of nanoscale devices and circuits for neuromorphic computational systems," IEEE Trans. Electron Devices. **60**(1), 246–253 (2013).