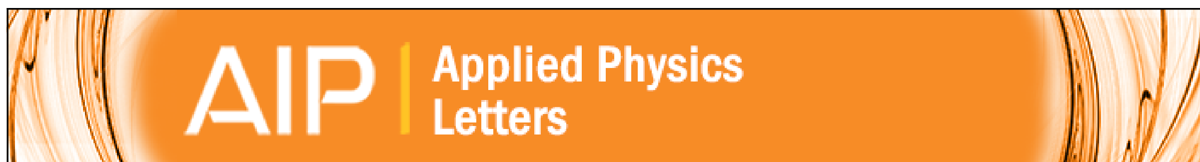

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Citation: Applied Physics Letters **101**, 103906 (2012); doi: 10.1063/1.4751339
View online: http://dx.doi.org/10.1063/1.4751339
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Characterization of thin epitaxial emitters for high-efficiency silicon heterojunction solar cells

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(Received 12 May 2012; accepted 22 August 2012; published online 6 September 2012)

We report silicon heterojunction solar cells with conversion efficiencies exceeding 21% using appropriately designed emitter structures comprised of highly doped thin epitaxial layers grown by plasma-enhanced chemical vapor deposition at temperatures close to 200 °C. We show that at a given doping concentration, there is an optimum epitaxial layer thickness, above which the conversion efficiency is limited by Auger recombination and bandgap narrowing within the epitaxial layer. In contrast, below the optimum thickness, the conversion efficiency is limited by carrier recombination at the emitter surface of the crystalline silicon substrate. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4751339]

Heterojunction (HJ) solar cells with hydrogenated amorphous Si (*a*-Si:H) contacts have reached a high conversion efficiency of 23.7% in the lab and 21.1% in production on *n*-type crystalline silicon (*c*-Si) substrates.[1] Several groups have demonstrated conversion efficiencies above 20% on *n*-type *c*-Si using this technology.[2–5] Plasma-enhanced chemical vapor deposition (PECVD) of *a*-Si:H at temperatures close to 200 °C offers the advantage of a low thermal budget as well as preserving the bulk lifetime of low-cost Si substrates. The PECVD of *a*-Si:H is also appealing in that it is an established technology in large-scale production of thin-film transistor back-planes for active-matrix displays.[6]

In typical HJ solar cells known as HJ with thin intrinsic layers (HIT), thin layers of intrinsic (i) *a*-Si:H are grown on the *c*-Si substrate to passivate the surface of *c*-Si, followed by doped *a*-Si:H layers to establish electric field at the emitter and back-surface-field junctions. The HIT structure is generally more suitable for *n*-type than *p*-type *c*-Si substrates due to a larger valence band offset compared to the conduction band offset at the *a*-Si:H/*c*-Si heterojunction.[7,8] As a result, HIT cell efficiencies achieved on *p*-type *c*-Si have been limited to 19.3%.[9] The development of high-efficiency HJ solar cells on *p*-type *c*-Si substrates would allow the usage of a wide range of *p*-type solar-grade mono-crystalline and multi-crystalline Si wafers, which are currently in widespread solar cell manufacturing. To address this issue, we proposed the HJ with engineered low-gap interlayer and thin epitaxial emitter (ELITE) cell structure and demonstrated conversion efficiencies well above 20% on *p*-type *c*-Si substrates.[8,10] In this Letter, we discuss the characterization of the thin epitaxial emitters for realizing high-efficiency ELITE cells and identify the mechanisms responsible for efficiency loss in these structures.

The schematic cross-section and equilibrium energy band diagram of the ELITE cells are illustrated in Figs. 1(a) and 1(b), respectively. At the emitter, the *i a*-Si:H layer used for surface passivation in HIT cells is replaced by a thin layer of highly doped hydrogenated *c*-Si (n^+ *c*-Si:H) grown epitaxially by PECVD at temperatures close to 200 °C. The absorption loss in the emitter is reduced by removing the *i a*-Si:H layer, resulting in a higher short circuit current, as demonstrated experimentally.[8] In addition, the presence of the n^+ *c*-Si:H layer reduces the effect of interface states and the workfunction of the transparent conductive oxide (TCO) at the emitter on the performance of the solar cell, allowing the usage of low-cost TCO materials such as aluminum-doped zinc-oxide (ZnO:Al).[8] The back-surface-field contact is formed by adding hydrogenated amorphous germanium (p^+ *a*-Ge:H) to the p^+ *a*-Si:H layer used in HIT cells. The p^+ *a*-Si:H/p^+ *a*-Ge:H/p^+ *a*-Si:H stack provides an effectively higher activated doping (due to modulation doping of p^+ *a*-Ge:H) and an effectively lower valence band offset with the *c*-Si substrate compared to the p^+ *a*-Si:H layer. As a result, efficient tunneling of holes through the potential barrier set by the valence band offset is facilitated without compromising the electric field.[8]

The epitaxial growth of *c*-Si:H is accomplished by incorporating appropriate levels of hydrogen dilution in the silane (SiH_4) precursor gas using the same PECVD reactor, which is used for *a*-Si:H growth. The substrate dependence of PECVD growth is well known, and given sufficiently high hydrogen dilution, the grown layer may vary from fully amorphous to single-crystalline depending on the substrate type.[11–13] Epitaxial growth is attributed to *in-situ* removal of weak Si-Si bonds from the growth surface by hydrogen radicals in plasma, allowing the grown layer to follow the crystalline structure of the substrate. The *c*-Si:H film may be doped *in-situ* by adding phosphine (PH_3) to the gas mixture, resulting in activated doping levels up to $2 \times 10^{20}\,cm^{-3}$ at temperatures as low as 150 °C.[13] The *c*-Si:H films grown by this technique are compressively strained due to the presence of hydrogen in the lattice, and large levels of compressive strain (over 0.5%) have been measured at hydrogen content levels above 10 at. %.[13] Accumulation of compressive strain leads to crystalline-to-amorphous phase transition after a critical thickness has been reached (Fig. 2(a)). The rough *c*-Si:H/*a*-Si:H interface resulting from the undesired *a*-Si:H growth increases carrier recombination at the interface,

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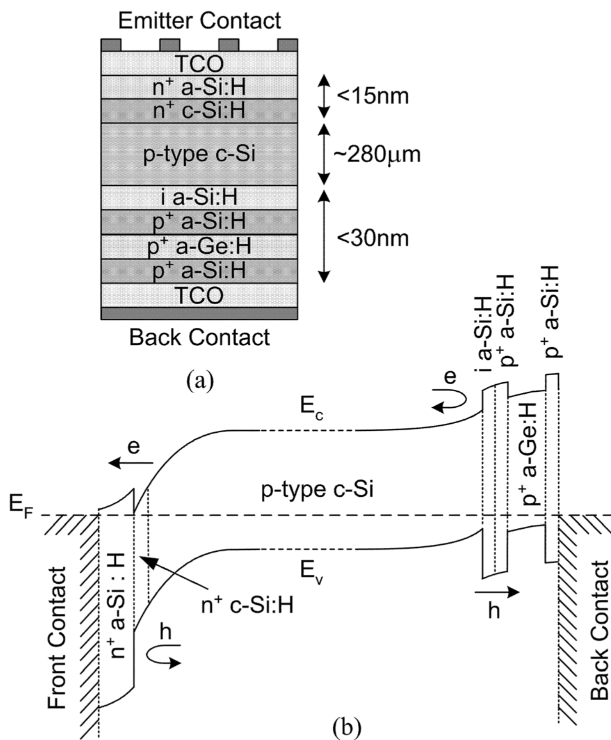
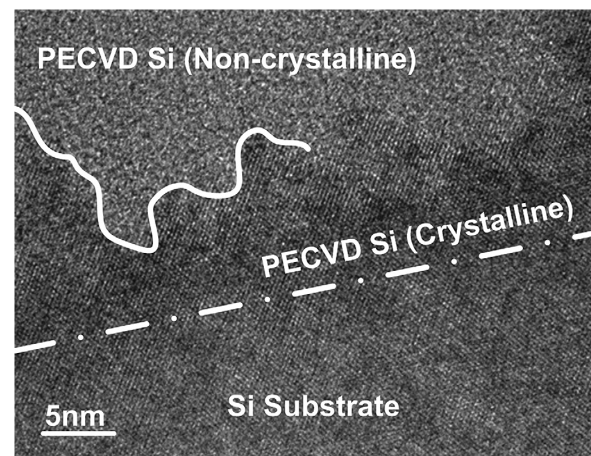


FIG. 1. (a) The schematic cross-section and (b) the schematic equilibrium energy band diagram of the heterojunction with ELITE solar cell structure.



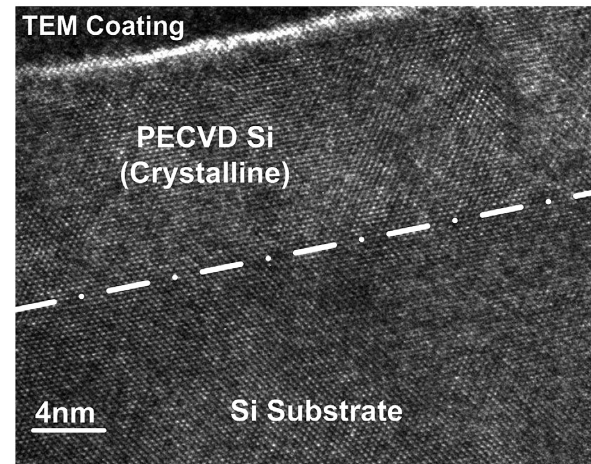


FIG. 2. Cross-sectional high-resolution transmission electron microscopy (HR-TEM) image of *c*-Si:H layers grown on *c*-Si substrates showing (a) crystalline to non-crystalline phase transition due to accumulated strain in the *c*-Si:H layer, resulting in a rough crystalline/non-crystalline transition interface, and (b) *c*-Si:H film grown at conditions, resulting in a lower accumulated strain so that the phase transition is avoided.

reducing the open circuit voltage of the cell, and must be avoided by adjusting the growth conditions (Fig. 2(b)). Similarly, in HIT cells, increased carrier recombination at rough *c*-Si:H/*a*-Si:H interfaces has been observed in the case of *a*-Si:H passivation layer growth, due to undesired *c*-Si:H growth.[3,14] In both cases, single-phase material growth is preferred over mixed-phase material growth, and the undesired growth of the opposite phase must be avoided.

To characterize the emitter structure, test cells with n^+ *c*-Si:H layer thicknesses in the range of 0–20 nm and an n^+ *a*-Si:H passivation layer thickness of 5 nm were grown on commercially available p^-/p^+ *c*-Si substrates (Fig. 3(a)). An activated donor doping density (N_D) of $\sim 5 \times 10^{19}\,\text{cm}^{-3}$ was incorporated in the n^+ *c*-Si:H layers as estimated by sheet resistance measurements on separate test samples. A total phosphorous concentration of $\sim 2.5 \times 10^{20}\,\text{cm}^{-3}$ was measured in the n^+ *c*-Si:H layers by secondary ion mass spectrometry (SIMS), indicating a doping efficiency of ~20%. The 2 μm thick p^- c-Si layer has an acceptor doping density of $\sim 5 \times 10^{15}\,\text{cm}^{-3}$ and serves as the absorption layer of the test cells. The p^+ *c*-Si carrier substrate has an acceptor doping density of $\sim 2 \times 10^{19}\,\text{cm}^{-3}$ and serves as a back-surface-field, repelling the minority electrons from the metal contact in the back. The open circuit voltage (V_{oc}) of the test cells was measured under an intensity of 1 sun using a solar simulator (Fig. 4(a)). For each of the test cells, corresponding PECVD stacks of n^+ *c*-Si:H/n^+ *a*-Si:H were grown on both sides of float-zone (FZ) p^- *c*-Si substrates having an acceptor doping density of $\sim 5 \times 10^{15}\,\text{cm}^{-3}$ and a thickness (W) of $\sim 300\mu$m (Fig. 3(b)), and the effective lifetime (τ_{eff}) of minority carriers (electrons) in the p^- *c*-Si substrate was measured by photo-conductance decay (PCD) using a Sinton WCT-120 tool (Fig. 4(b)). The bulk lifetime of minority carriers (τ_{bulk}) in the p^- *c*-Si substrates is estimated to be ~4.4 ms from PCD measurement of iodine-passivated p^- *c*-Si substrates.

The V_{oc} of the test cells improves with increasing the thickness of the n^+ *c*-Si:H layer in the 0-7.5 nm range, reaching a maximum in the 5-7.5 nm range and degrades as the n^+ *c*-Si:H layer thickness is further increased (Fig. 4(a)). In all cases, including an n^+ *c*-Si:H layer in the emitter stack results in a larger V_{oc} compared to that without an n^+ *c*-Si:H layer. Similarly, the measured τ_{eff} is improved by including the n^+ *c*-Si:H layer, indicating the improvement of surface passivation (Fig. 4(b)). This improvement is attributed to the presence of the electric field set up by the n^+ *c*-Si:H layer, which repels the minority holes from the p^- *c*-Si/n^+ *c*-Si:H and n^+ *c*-Si:H/n^+ *a*-Si:H interfaces towards the bulk of the p^- *c*-Si substrate. The sharp improvement of τ_{eff} by increasing the n^+ *c*-Si:H thickness from 0 to 5 nm may be attributed to the accumulation of hydrogen at the p^- *c*-Si/n^+ *c*-Si:H interface, as the hydrogen profile in n^+ *c*-Si:H exhibits a gradient towards the p^- *c*-Si/n$^+$ *c*-Si:H interface.[13] Hydrogen is well-known to passivate the dangling bonds at the surface of

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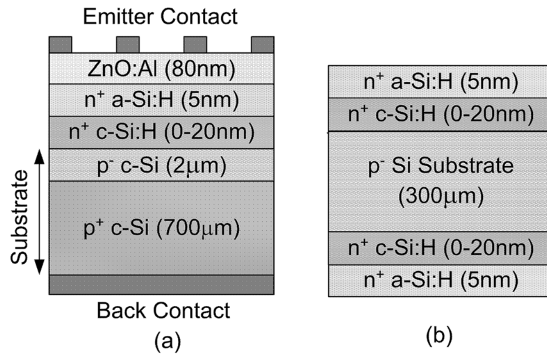
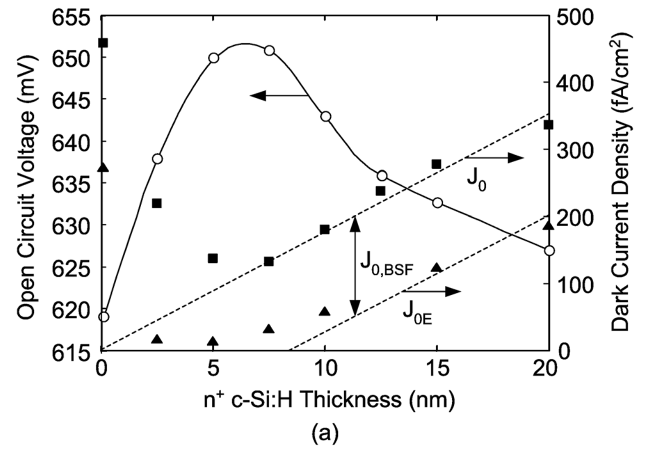


FIG. 3. Schematic cross-sections of the (a) test cells used for characterizing the n^+ doped c-Si:H/a-Si:H emitter stack and (b) test structures coated symmetrically on both sides with the same emitter stack as that of the corresponding test cells, used for μ-PCD measurements.



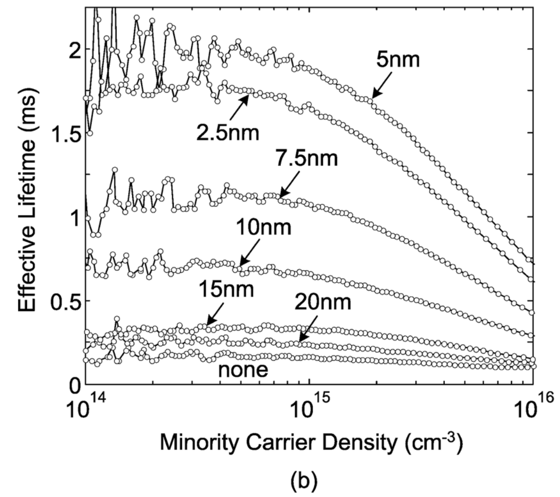


FIG. 4. (a) Open circuit voltages and dark current densities of test cells of Fig. 3(a), and the contribution of the emitter junction to the dark current density calculated from PCD measurements on test structures of Fig. 3(b); and (b) effective minority carrier lifetime versus minority carrier density from PCD measurements on test structures of Fig. 3(b).

c-Si. Using the relation $1/\tau_{eff} = 1/\tau_{bulk} + 2S_{eff}/W$, the effective surface recombination velocity (S_{eff}) of minority carriers at a density of $10^{15}\,\mathrm{cm}^{-3}$ is estimated to reduce from $\sim$100 cm/s to $\sim$4 cm/s, as the thickness of the n^+ c-Si:H layer is increased from 0 to 5 nm. The measured τ_{eff} degrades as the n^+ c-Si:H thickness is further increased, similar to the trend observed for V_{oc}.

To investigate the degradation of V_{oc} and τ_{eff} at n^+ c-Si:H thicknesses above $\sim$7.5 nm, the dark current density of the test cells (J_0) was calculated from the relation $J_0 = J_{sc} \exp(-qV_{oc}/kT)$, where J_{sc} is the short circuit current density of the cells ($\sim$11 mA/cm^2), q is the electron charge, k is the Boltzmann constant, and T is the absolute temperature. The contribution of the emitter junction to the dark current density (J_{0E}) was calculated from the relation $J_{0E} = qn_i^2 S_{eff}/(\Delta n + N_A)$ at $\Delta n = 10^{15}\,\mathrm{cm}^{-3}$, where Δn is the density of minority carriers from the PCD measurement.[15] It is observed that $J_0 > J_{0E}$ (Fig. 4(a)). The difference between J_0 and J_{0E} is due to recombination within the p^- c-Si layer and/or at the back surface and is expected to be the same for all n^+ c-Si:H thicknesses. The variation in the experimental values of $J_0 - J_{0E}$ (148 ± 36 fA/cm^2) is mainly due to the experimental inaccuracy in determining J_{0E} from the PCD measurements. Assuming negligible recombination in the depletion region, J_{0E} may be expressed as

$$J_{0E} = q\frac{D_h}{L_h}\frac{n_i^2}{N_D}\exp\frac{\Delta E_g}{kT}F_N, \tag{1}$$

where D_h and L_h are the diffusion constant and the diffusion length of minority holes in n^+ c-Si:H, respectively; n_i is the intrinsic carrier concentration in Si, ΔE_g is the bandgap narrowing in n^+ c-Si:H, and F_N is defined as[16,17]

$$F_N = \frac{S_h\cosh(W_N/L_h) + (D_h/L_h)\sinh(W_N/L_h)}{(D_h/L_h)\cosh(W_N/L_h) + S_h\sinh(W_N/L_h)}, \tag{2}$$

where W_N is the thickness of the n^+ c-Si:H layer, and S_h is the surface recombination velocity of minority holes at the n^+ c-Si:H "*surface*," i.e., at n^+ c-Si:H/n^+ a-Si:H interface. (Note that S_h and S_{eff} are different parameters, as S_{eff} represents the effective rate at which minority electrons generated in the p^- c-Si substrate are recombined at the p^- c-Si surface, including the p^- c-Si/n^+ c-Si:H interface, within the n^+ c-Si:H layer where electrons are the majority carriers, and the n^+ c-Si:H/n^+ a-Si:H interface.) If $W_N \ll L_h$, then $F_N \approx 1$, and J_{0E} becomes nearly independent of W_N. This would apply to a thick and/or highly defective n^+ c-Si:H material. If $W_N \gg L_h$, then $\sinh(W_N/L_h) \approx W_N/L_h$, $\cosh(W_N/L_h) \approx 1$, and F_N is approximated as

$$F_N \approx \frac{W_N/L_h + L_{sh}/L_h}{1 + (W_N/L_h)(L_{sh}/L_h)}, \tag{3}$$

where L_{sh} is a characteristic length defined as $L_{sh} = S_h L_h^2/D_h = S_h\tau_h$ (where τ_h is the recombination lifetime of minority holes in n^+ c-Si:H) and may be interpreted as an effective distance from the n^+ c-Si:H surface within which all minority holes existing in n^+ c-Si:H are recombined at the n^+ c-Si:H surface, rather than in the bulk of n^+ c-Si:H. If $L_{sh} \ll W_N$, then $F_N \approx W_N/L_h$ (note the original assumption of $W_N \gg L_h$ in deriving Eq. (3)), and J_{0E} becomes nearly independent of S_h, but linearly proportional to W_N, and may be expressed as

$$J_{0E} = q\frac{n_i^2}{N_D}\frac{W_N}{\tau_h}\exp\frac{\Delta E_g}{kT}. \tag{4}$$

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The linear dependence of J_0 (and J_{0E}) on the n^+ c-Si:H layer thickness observed in Fig. 4(a) implies that Eq. (4) applies to n^+ c-Si:H layers thicker than ~7.5 nm. Assuming that ΔE_g is purely a function of activated doping in n^+ c-Si:H ($\Delta E_g = \sim 85$ meV at $N_D = 5 \times 10^{19}$ cm^{-3} (Ref. 18)), a minority hole lifetime of $\tau_h \approx 100$ ps is extracted from a least square fit to J_0 (Fig. 4(b)), which corresponds to a minority hole diffusion length of $L_h \approx 200$ nm.[18,19] (J_0 was used for curve fitting rather than J_{0E}, since a relatively smaller experimental error is expected in the calculation of J_0). Assuming S_h is, to the first order, of the same magnitude as S_{eff} when n^+ c-Si:H is omitted, i.e., ~100 cm/s, L_{sh} is found to be ~0.1 nm, consistent with the assumption of $L_{sh} \ll W_N$.

To investigate the difference between J_0 and J_{0E}, test cells with 7.5 nm/5nm thick n^+ c-Si:H/n^+ a-Si:H emitter stacks and various p^- c-Si layer thicknesses in the range of 0.5-1.75 μm were prepared by thinning the p^- c-Si layer using wet etching. The measured J_{sc} and V_{oc} both decreased by reducing the thickness of the p^- c-Si layer due to lower light absorption; however, the change in the calculated J_0 was negligible. This indicates that recombination within the p^- c-Si layer is small and the difference between J_0 and J_{0E} is mainly due to the contribution of the back-surface-field to the dark current density ($J_{0,BSF}$), i.e., $J_0 = J_{0E} + J_{0,BSF}$. The value of $J_{0,BSF}$ may be estimated by rewriting Eqs. (1) and (2) for the p$^+$ c-Si region (note Eq. (2) will be equal to 1 since the p$^+$ c-Si substrate is thick). Using the parameters reported for p^+ c-Si regions,[20] it is straightforward to verify that the experimentally determined value of 148 ± 36 fA/cm^2 for $J_{0,BSF}$ is reasonable.

The values of τ_h and L_h extracted for n^+ c-Si:H are lower than that measured in conventionally doped n^+ c-Si having the same activated doping density of 5×10^{19} cm^{-3} ($\tau_h \approx 1$ ns and $L_h \approx 600$ nm[16,17]). This indicates a higher density of structural defects in n^+ c-Si:H compared to conventionally doped n^+ c-Si at the same activated doping level. The quality of the n^+ c-Si:H layer is affected by growth conditions such as plasma power density, hydrogen dilution, and dopant gas flow ratio, as well as surface cleanliness and crystalline orientation of the c-Si substrate. The open circuit voltage is the solar cell parameter which is affected most by the structural quality of n^+ c-Si:H, as discussed above in terms of minority hole lifetime. The thin epitaxial emitter structure was applied to ~280 μm thick FZ p-type c-Si substrates textured by random pyramids, and a high conversion efficiency of 21.4% ($V_{oc} = 682$ mV, $J_{sc} = 39.1$ mA/cm^2, $FF = 80.2\%$) was achieved in conjunction with an improved back-surface-field stack.[10] Low-cost ZnO:Al was sputtered at room temperature to form the top and bottom electrodes, followed by a lift-off process to form the front metal grid, resulting in a shadowing loss of ~3%. All process steps were carried out at temperatures below 200 °C. The measurements were performed on 1 cm^2 cells using an aperture area of 0.92 cm^2 to eliminate edge effects and calibrated against independently measured baseline (~20% efficiency) ELITE cells for accuracy.[8] Further optimization of the front and back PECVD stacks yielded a larger V_{oc} of 710 mV, at the cost of a slight degradation of the fill-factor (FF) to 78.6%. The total integrated J_{sc} of the optimized cells was determined to be 40.6 mA/cm^2 by external quantum efficiency measurement (with no shadowing loss from the front metal grid), corresponding to a J_{sc} of 39.3 mA/cm^2 at 3% shadowing and a conversion efficiency of 21.9%.

In summary, we discussed the characterization of highly doped thin epitaxial layers grown by PECVD for realizing high-efficiency heterojunction solar cells and reported conversion efficiencies exceeding 21% on p-type c-Si substrates. Interface recombination at the emitter surface and bulk recombination within the thin epitaxial emitter were identified as the dominant mechanisms responsible for efficiency loss depending on the thickness of the epitaxial layer.

The authors gratefully acknowledge Dr. Ghavam G. Shahidi and Dr. T-C. Chen of IBM Research for their technical guidance and managerial support. The authors are also grateful to Professor Sigurd Wagner of Princeton University for allowing the usage of his PECVD facility for this work.

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