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Electronic properties of monolayer tungsten disulfide grown by chemical vapor deposition

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We demonstrate chemical vapor deposition of large monolayer tungsten disulfide (WS_2) ($>200\ \mu\text{m}$). Photoluminescence and Raman spectroscopy provide insight into the structural and strain heterogeneity of the flakes. We observe exciton quenching at grain boundaries that originate from the nucleation site at the center of the WS_2 flakes. Temperature variable transport measurements of top-gated WS_2 transistors show an apparent metal-to-insulator transition. Variable range and thermally activated hopping mechanisms can explain the carrier transport in the insulating phase at low and intermediate temperatures. The devices exhibit room-temperature field-effect electron mobility as high as $48\ \text{cm}^2/\text{V}\cdot\text{s}$. The mobility increases with decreasing temperature and begins to saturate at below $100\ \text{K}$, possibly due to Coulomb scattering or defects. *Published by AIP Publishing.*
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Layered two-dimensional (2D) transition metal dichalcogenides (TMDs) exhibit unique properties such as the ease of energy band engineering by adjusting the number of layers or by making van der Waals heterostructures.¹ Such salient features of TMDs make them promising for a wide range of electronic and optoelectronic applications.^{2–4} However, the transformation of basic science studies into viable device technologies necessitates large-area synthesis of device-quality TMDs. Significant research is ongoing to grow monolayer (ML) TMDs using chemical vapor deposition (CVD).^{5–7} In particular, synthesis of ML- WS_2 is gaining attention due to its attractive material properties including large energy bandgap ($E_g \sim 2.0\ \text{eV}$),⁸ small effective mass ($m^* \sim 0.26m_0$),⁹ and strong spin-orbit coupling.¹⁰ However, more work is needed to study large-area synthesis of WS_2 and its electronic properties.

The high density of structural disorders including vacancies, grain boundaries (GB), and dislocations is limiting the performance of devices made of CVD TMDs. For example, the electron mobility of CVD WS_2 grown on SiO_2 has reported to be in the range of $0.01\text{--}14\ \text{cm}^2/\text{V}\cdot\text{s}$ at room temperature.^{11,12} These mobility values are substantially below the theoretical limit of $\sim 1100\ \text{cm}^2/\text{V}\cdot\text{s}$.⁹ Further, the maximum carrier mobility at low temperature is believed to be limited by long-range Coulomb scattering or short-range defects.¹³ Previous studies also reported a crossover to an insulating regime at low carrier densities for 2D TMD devices,^{14–16} possibly mediated by strong localization due to high density of structural disorder.^{17,18} Continual advancements are necessary to reduce the density of structural disorders and the resulting localized gap states in CVD TMDs.

Here, we demonstrate reproducible CVD growth of large ML- WS_2 flakes. Detailed material and device characterizations unravel the structural and electrical properties of the CVD WS_2 . The flakes exhibit optoelectronically distinct bright and dim regions. Temperature-dependent transport studies reveal a crossover from an apparent metallic phase at

high carrier densities to an insulating phase at low carrier densities. The ML- WS_2 devices show field-effect mobility of $\sim 48\ \text{cm}^2/\text{V}\cdot\text{s}$ at room temperature that is on par with the best reports for CVD molybdenum disulfide (MoS_2).^{19,20} Lastly, our transport studies suggest the dominance of optical phonon scattering in the high temperature regime, while Coulomb scattering or defects limit carrier mobility at temperatures below $100\ \text{K}$.

CVD using solid precursors is a common approach for synthesis of TMDs on SiO_2/Si substrates. To promote the CVD growth of TMDs on SiO_2 , alkali-based salt molecules are often used as seed layers.^{11,21} However, the use of such seed layers can unintentionally introduce impurities in the material (substitutionally or interstitially), thus compromising carrier transport properties due to increased impurity scattering or defects. This is an important consideration for most electronic and optoelectronic devices that require materials with reasonably high carrier mobility or long minority carrier lifetime. It is, therefore, preferable to avoid using those growth promoters. We have developed a reproducible CVD process yielding ML- WS_2 using tungsten oxide (WO_3) and sulfur (S) solid precursors without requiring a growth promoter. The CVD growth of WS_2 was performed using a custom-made setup (Figure S1 in [supplementary material](#)) at $950\ \text{C}$ on p^+ silicon substrates with $285\ \text{nm}$ thermally grown SiO_2 . The optimal quantities of WO_3 and S precursors are about $20\ \text{mg}$ and $100\ \text{mg}$. The growth was done at atmospheric pressure in nitrogen ambient ($10\ \text{sccm}$) for $3\ \text{min}$. The key growth parameters were optimized to obtain large ML- WS_2 triangles in excess of $\sim 200\ \mu\text{m}$ (Figure S2 in [supplementary material](#)). The monolayer thickness of CVD WS_2 was verified using atomic force microscopy (AFM), photoluminescence (PL) measurement, and Raman spectroscopy (Figure S2 in [supplementary material](#)). The AFM step-height profile measured at the edge of triangles was found to be $\sim 0.8\ \text{nm}$. The PL spectrum exhibits a strong peak intensity at $\sim 1.97\ \text{eV}$. The Raman spectrum shows the separation of $65\ \text{cm}^{-1}$ between the in-plane E_{2g} and the out-of-plane A_{1g} vibration modes. Overall, these measurements confirmed the successful growth of ML- WS_2 .

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Layered TMDs exhibit strong photoemission properties at monolayer thickness due to their direct energy bandgap and also strong many-body effects, including the formation of bound electron-hole pairs.^{22–25} Therefore, PL measurements are widely used for studying the physical properties of ML-TMDs. Recent PL studies of CVD WS₂ have shown distinct bright and dim regions in the edge and inner regions of the flakes. Although the physical origin of this phenomenon is a subject of study, the strong emission from the edge region has been attributed to the formation of higher-order excitonic states including negative trions and biexcitons.²⁶ Further, the low-temperature PL spectra of the dim PL regions reveal the presence of defect-bound excitons,²⁶ suggesting the higher density of structural disorder in those dim regions. To examine the photoemission properties of our CVD WS₂, we performed high-resolution PL measurements, shown in Figure 1(a). Two interesting observations can be made in our nano-PL studies. First, the PL map of the ML-WS₂ flakes shows local exciton quenching at GBs that originate from the center of the flake. From the geometric angles, we surmise that these GBs originate from the nucleation region of the flakes. Similar GBs were recently observed in CVD ML-MoS₂ using nano-PL imaging and have shown to be sulfur-deficient through nano-Auger spectroscopy.²⁷ Second, the spatial location of the bright and dim regions in our flakes is different from the previous reports.^{26,28} Three distinct regions are visible: (i) a bright inner region, (ii) an intermediate dim region, and (iii) a bright narrow band at the outer edge. In our subsequent discussions, we use the terms “bright” and “dim” to refer to these distinct regions. Figure 1(b) illustrates the PL peak position map. We observe that the PL peak energies in the intermediate dim region show red shift relative to the bright regions. The linewidth of the

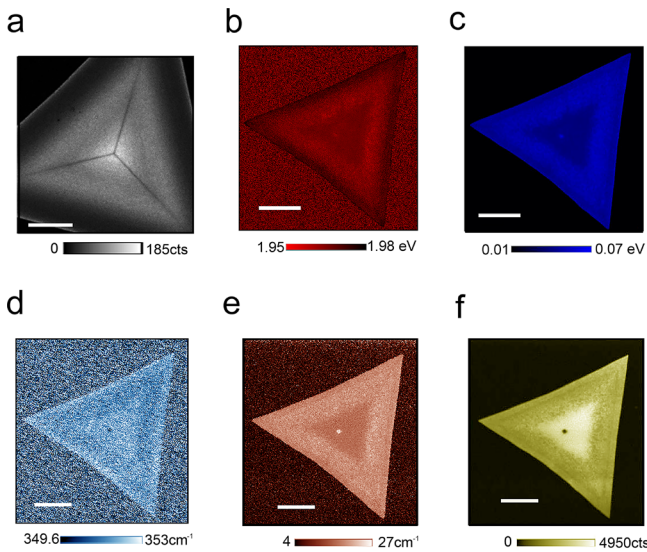


FIG. 1. Heterogeneity of structure and strain in CVD WS₂. (a) Map of the PL intensity reveals optoelectronically distinct bright and dim regions (scale bar is 20 μm). We observe exciton quenching at GBs that are emanating from the center of the flakes. The maps of PL peak (b) position and (c) linewidth illustrate the structural heterogeneity of the dim and bright regions. (d) Variation of the in-plane E_{2g} Raman peak indicates the heterogeneity of the strain. The map of (e) linewidth and (f) intensity of the E_{2g} peaks suggest higher structural disorder in the intermediate regions with dim PL intensities (scale bars are 40 μm in (b)–(f)).

PL peaks in the bright region is ~ 40 meV, confirming the good crystalline quality of the film. The linewidth in the dim region is broader (Figure 1(c)), possibly due to the existence of additional defect-bound excitons at lower energies.²⁶ From the PL studies, we expect the dim region to be plagued with higher structural defects compared to the bright regions.

Raman spectroscopy was performed to further examine the heterogeneity of the structure and strain in CVD WS₂ films. Previous studies have shown the presence of local tensile strain in CVD ML-MoS₂.²⁹ The residual strain in CVD WS₂ is discernible from the variations of the in-plane E_{2g} peak position in Figure 1(d). The residual strain is possibly compressive, arising at the cooling stage of the growth process due to the mismatch in the coefficients of thermal expansion $\Delta\alpha = \alpha_{\text{Si}} - \alpha_{\text{WS}_2}$.³⁰ We deduced the type of the residual thermal stress from the sign of the $\Delta T \cdot \Delta\alpha$ product, where $\Delta\alpha$ is positive and ΔT at the cooling stage is negative. The maps of the E_{2g} peak linewidth and intensity in Figures 1(e) and 1(f) illustrate the striking difference in the structural properties of the dim and bright regions. The lower intensity and wider linewidth of the E_{2g} peaks in the intermediate dim region suggest its higher structural disorder than the bright regions.

We fabricated top-gated Hall-bar field-effect transistors (FETs) to study the key electronic properties of the CVD WS₂ including density of localized gap states and scattering mechanisms limiting carrier transport. Figure 2(a) illustrates the schematic of the ML-WS₂ device. Devices were fabricated on the original SiO₂/Si growth substrates. The metal electrodes were formed through electron beam evaporation of Ti/Au (10 nm/40 nm). The gate dielectric was formed through

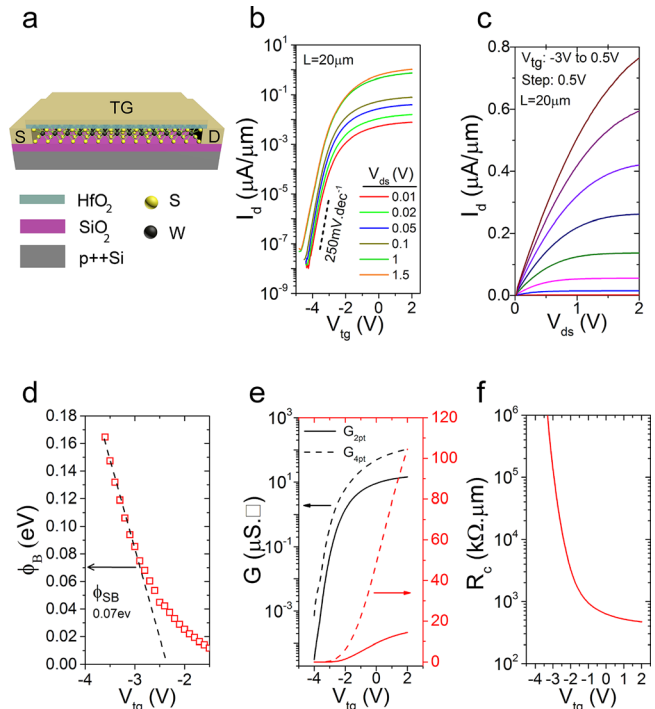


FIG. 2. Electrical characteristics of WS₂ FETs. (a) Schematic structure of top-gated WS₂ FETs. Room-temperature (b) transfer and (c) output characteristics of a device fabricated in the bright region of a flake. (d) The Schottky barrier at the source/drain is ~ 70 meV. (e) Significant difference between the G_{2pt} and G_{4pt} reveals the large parasitic series resistance at the contacts. (f) The specific contact resistance approaches to ~ 500 kΩ μm at high carrier densities.

atomic layer deposition (ALD) of hafnium oxide (HfO_2) at 200°C . Figure 2(b) illustrates the room-temperature transfer characteristics of a device fabricated in the bright region of a ML- WS_2 flake. The device exhibits a subthreshold swing of ~ 250 mV/dec and ON/OFF ratio of $> 10^5$ at the drain bias of 10 mV. The corresponding output characteristic of the device is shown in Figure 2(c), illustrating linear characteristics at small drain bias and saturation at higher drain voltages. Figure 2(d) shows the Schottky barrier at the source/drain contacts that is about 70 meV (details described in the Supplementary information).³¹ The relatively large barrier height significantly increases the parasitic series resistance at the contacts, evident from the noticeable difference between the measured two-point (G_{2pt}) and four-point (G_{4pt}) conductance values (Figure 2(e)). The G_{4pt} represents the intrinsic conductance of the channel, while the G_{2pt} includes the effect of the contact resistances from the source/drain regions. The specific contact resistance (R_c) of the device normalized to the contact width (W) was calculated using the following expression:

$$R_c = \frac{W}{2} \left(\frac{1}{G_{2pt}} - \frac{1}{G_{4pt}} \right).$$

The specific contact resistance of the device (Figure 2(f)) asymptotically approaches $500 \text{ k}\Omega \mu\text{m}$ at $V_g = 3 \text{ V}$. Further improvement of the contact resistance can be achieved using low-work function metal electrodes,³¹ graphene interlayer,^{32–34} phase engineering,¹⁹ or chemical and electrostatic doping.^{20,35,36}

Next, we turn our attention to examine the trap states in the energy bandgap that originate from structural disorders in the ML- WS_2 film as well as its interface with top high- k and bottom SiO_2 dielectrics. These localized gap states can give rise to an apparent metal-insulator transition (MIT) due to strong localization at low carrier densities¹⁸ and degradation of carrier transport due to excessive charge scattering.³⁷

To quantify the density of the trap states in the energy bandgap of ML- WS_2 , we performed capacitance-voltage (C-V) and ac-conductance measurements.³⁸ Figure 3(a) illustrates the measured capacitance as a function of frequency for different gate bias voltages. The existence of a double-hump feature in the capacitance-frequency curves suggests the presence of two or more types of trap states with different time constants.³⁷ Assuming two different types of trap states, the equivalent device model in Figure 3(b) was used for extracting the density (D_{it}) and the corresponding time constant (τ_{it}) of the localized gap states from the C-V data. In this model, C_{it} and R_{it} represent the corresponding capacitance and resistance of the traps given by $C_{it} = q \cdot D_{it}$ and $R_{it} = \tau_{it} / C_{it}$, where q is the elementary charge. Further, the notations “M” and “B” correspond to the mid-gap and band-edge traps. The equivalent device model was used to fit the data in Figure 3(a) (solid lines), and subsequently extract the density of traps and their time constant at a given gate voltage, shown in Figure 3(c). The details of the calculations are given in [supplementary material](#).

The ac conductance method provides an additional way to probe the density and time constant of traps from C-V measurements.³⁸ The extracted ac conductance (G_p) was

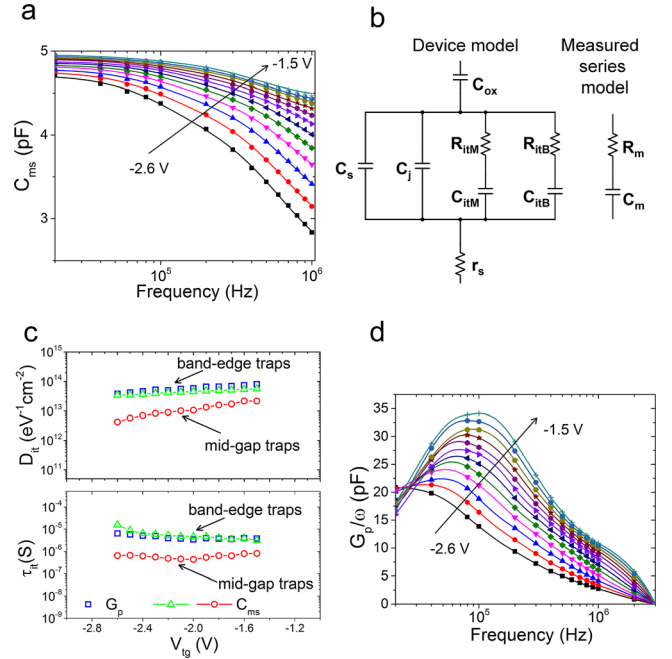


FIG. 3. Quantification of localized gap states. (a) Capacitance as a function of frequency measured at different gate voltages. (b) Electrical device model that was used for extracting the density and time constant of the traps from the measured series model. Two types of traps (mid-gap and band-edge) were assumed to fit the capacitance-frequency curves, solid lines in (a). (c) Density and time constant of the traps extracted from the equivalent device model and the ac-conductance in (d).

calculated from the measured series model in Figure 3(b). The plot in Figure 3(d) shows the G_p/ω as a function of frequency, in which ω is the angular frequency. The noticeably high density of band-edge traps dominates the ac conductance, thereby making this method infeasible for probing the mid-gap traps. The density and time constant of the band-edge traps at different gate voltages were calculated using the following relations:³⁸ $D_{itB} = \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{peak}$ and $\tau_{it} = \frac{1.98}{2\pi f_0}$, where $(G_p/\omega)_{peak}$ is the maximum of the G_p/ω curve at frequency f_0 . The extracted trap density and their corresponding time constants are included in Figure 3(c), consistent with the values extracted for the band-edge traps using the equivalent circuit model. Next, temperature-dependent measurements were made to examine the effect of these localized gap states on the electronic properties of the CVD WS_2 devices.

Figure 4(a) shows the corresponding four-point conductance of the device in Figure 2, measured at different temperatures. Several interesting observations can be made from the data. The measurements reveal the weak dependence of subthreshold swing on temperature. From the principle of FET device operation, the carrier diffusion is the dominant transport mechanism in the subthreshold regime. The resulting diffusion current depends on the Boltzmann distribution of charge carriers in the source region, thereby exhibiting an exponential dependence on temperature.³⁹ The weak dependence of subthreshold swing on temperature has previously been observed in other TMD FETs.^{37,40} This phenomenon has been attributed to the distribution of local band tail states with an energy width significantly larger than the thermal energy kT .³⁷

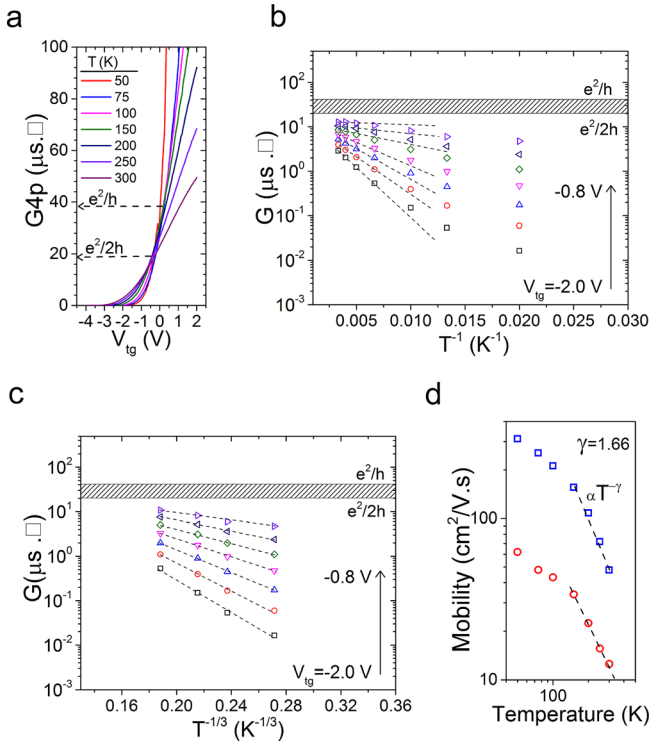


FIG. 4. Temperature-dependent measurements of conductivity. (a) A crossover from an apparent metallic phase at high carrier densities to an insulating phase at low carrier densities is happening at conductivity range of $e^2/2h$ to e^2/h . The semi-logarithmic plots of conductivity of the insulating phase as a function of (b) T^{-1} , and (c) $T^{-1/3}$, suggesting thermally activated hopping and VRH transport mechanisms in intermediate and low temperature regimes, respectively. (d) Variation of μ_{4pt} as a function of temperature, indicating the dominance of optical phonons at high temperatures. At low temperatures, the μ_{4pt} is limited by Coulomb scattering or defects.

The temperature-dependent measurement of the intrinsic channel conductance (i.e., G_{4pt}) in Figure 4(a) exhibits two distinct regimes. At gate voltages above -0.8 V, the conductance monotonically increases with decreasing temperature and begins to deviate from this trend at the gate voltages below -0.8 V. This crossover is attributed to an apparent MIT with presumably a weakly localized regime at high carrier densities (i.e., an apparent metallic phase) and a strongly localized regime at low carrier densities (i.e., an insulating phase). The observation of an apparent MIT in our ML- WS_2 devices is consistent with the previous reports on 2D semiconductors including TMD-based devices with high disorder.^{14,15,18,41} The crossover between these two regimes occurs at conductivity values between $e^2/2h$ and e^2/h , a signature of MIT in 2D systems.¹⁸

To better understand the origin of MIT in our devices, the logarithmic intrinsic conductivity of the channel (i.e., $\log(G_{4pt})$) was plotted as a function of $1/T$ and $(1/T)^{1/3}$, where T is the temperature. The plots are shown in Figures 4(b) and 4(c). From the data in Figure 4(b), the intrinsic channel conductivity exhibits an Arrhenius-type activated behavior at intermediate temperatures for gate voltages below -0.8 V. At lower temperatures, however, the conductivity

can possibly be explained by the variable range hopping (VRH) transport via localized states (Figure 4(c)), where the conductivity follows the relation⁴² $G_{4pt} \propto \exp\left(-\frac{T_1}{T}\right)^{1/3}$. While strong localization at low carrier densities is likely to be responsible for the observed insulating phase in our ML- WS_2 devices, the classical percolation model can also explain the crossover phenomenon.^{17,43}

Lastly, we study the scattering mechanisms limiting the carrier transport in ML- WS_2 devices. Figure 4(d) shows the variations of the field-effect four-point mobility (μ_{4pt}) as a function of temperature for two FETs fabricated in the inner bright and intermediate dim regions of the same flake. The intrinsic field-effect mobility was calculated using the following expression:

$$\mu_{4pt} = \frac{1}{C_{tg}} \frac{L}{W} \frac{dG_{4pt}}{dV_g},$$

where L and C_{tg} are the channel length of the device and the measured capacitance of the HfO_2 gate dielectric, respectively. In our measurements, the back gate was connected to the ground to avoid the capacitive coupling between the top and bottom electrodes.⁴⁴ The FET located in the bright region exhibits a high room-temperature field-effect mobility of ~ 48 $cm^2/V.s$. We have noticed that devices located in the intermediate dim region of the flakes show smaller field-effect mobility than those in the bright region. Nonetheless, the μ_{4pt} of the ML- WS_2 devices follows similar temperature-dependent behavior. In particular, at high temperature range ($T \geq 100$ K), μ_{4pt} follows a power-law temperature dependence ($\propto T^{-\gamma}$) with $\gamma \sim 1.66$, indicating the dominance of optical phonon scattering in these devices.^{13,45} Dielectric engineering can diminish the scattering by the homopolar optical phonons.^{14,46} At lower temperatures, phonon scattering decreases and consequently the exponent γ becomes smaller (~ 0.6). In this temperature regime, μ_{4pt} is possibly limited by long-range Coulomb impurities or short-range structural disorders.⁴⁶

In conclusion, we have demonstrated chemical vapor deposition (CVD) of large monolayer WS_2 on SiO_2 using WO_3 and S solid precursors. The photoluminescence (PL) results revealed grain boundaries that are emanating from the center of WS_2 flakes. These grain boundaries are surmised to be S-deficient. The nano-PL studies also showed the existence of distinct bright and dim regions in CVD WS_2 flakes. The bright region in the inner part of the flake exhibits higher mobility than the intermediate dim regions. The temperature-dependent measurements of the Hall-bar FETs revealed an apparent metal-insulator transition. The crossover phenomenon is likely to stem from defect-mediated strong localization. Finally, our results indicate the dominance of optical phonon scatterings in the high temperature regime ($T \geq 100$ K), while Coulomb scattering or defects limit transport at low temperatures.

See [supplementary material](#) for additional details of the material synthesis and further characterization results of the monolayer CVD film and the transistors.

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