NANO LETTERS

Letter

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Extremely Flexible Nanoscale Ultrathin Body Silicon Integrated Circuits on Plastic

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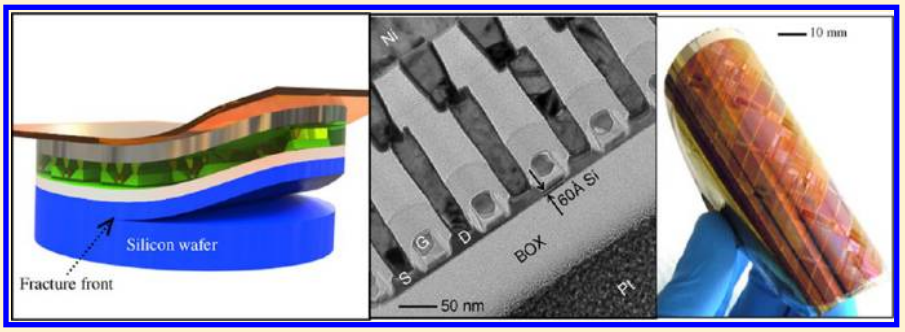
Supporting Information



ABSTRACT: In recent years, flexible devices based on nanoscale materials and structures have begun to emerge, exploiting semiconductor nanowires, graphene, and carbon nanotubes. This is primarily to circumvent the existing shortcomings of the conventional flexible electronics based on organic and amorphous semiconductors. The aim of this new class of flexible nanoelectronics is to attain high-performance devices with increased packing density. However, highly integrated flexible circuits with nanoscale transistors have not yet been demonstrated. Here, we show nanoscale flexible circuits on 60 Å thick silicon, including functional ring oscillators and memory cells. The 100-stage ring oscillators exhibit the stage delay of ~16 ps at a power supply voltage of 0.9 V, the best reported for any flexible circuits to date. The mechanical flexibility is achieved by employing the controlled spalling technology, enabling the large-area transfer of the ultrathin body silicon devices to a plastic substrate at room temperature. These results provide a simple and cost-effective pathway to enable ultralight flexible nanoelectronics with unprecedented level of system complexity based on mainstream silicon technology.

KEYWORDS: *Flexible electronics, integrated circuits, thin-film transistors, mechanical flexibility, ultrathin body silicon*

Thin-film electronic materials have been extensively studied for realizing a wide range of mechanically flexible electronic devices such as light-emitting diodes,[1] thin-film transistors,[2,3] photovoltaic solar cells,[4,5] and sensors.[6,7] So far, the mainstream flexible electronics have been based on thin-film organic[8,10] and amorphous[11,12] semiconductors that allow direct device fabrication on a flexible substrate at relatively low temperatures (≤300 °C). The salient feature of this processing scheme is the ability to achieve very large-area flexible electronics at a relatively low processing cost. However, the inherently defective and highly disordered crystalline structure in such materials severely limits the overall device performance and reliability when the device dimensions are scaled down.

Alternatively, nanomaterials such as nanowires[13,14] and carbon nanotubes[15,16] have been exploited for realizing high-performance flexible nanoelectronics, owing to their nanoscale dimensions and superb carrier transport properties. Despite the remarkable advances in understanding the physical properties of such materials and the promising demonstration of flexible devices, implementation of highly integrated circuits using these materials still encounters numerous practical challenges.

The ability to realize sophisticated system-on-chip (SoC) integrated circuits with an unprecedented level of functionality in a cost-effective manner has been the hallmark of the silicon microelectronics. However, silicon integrated circuits are conventionally fabricated on thick mechanically rigid substrates. One straightforward approach to render fully fabricated silicon chips mechanically flexible is through the chemical and/or mechanical removal of the wafer using polishing methods[17] or deep reactive ion etch such as a smart skin process.[18] Some of the drawbacks to this approach include the long times and specialized equipment required to remove the bulk Si wafer. To overcome the constraints of the polishing approaches, several clever layer transfer methods have been demonstrated including assembly of small-size thin-film inorganic semiconductor structures and devices,[19,20] epitaxial layer transfer (ELTRAN),[21] and its variants.[22] In particular, the small-size thin-film inorganic devices are generally obtained utilizing epitaxial layer lift-off (ELO) processes.[23,24] The ELO method works based on the selective lateral removal of an embedded sacrificial layer between the substrate and the semiconductor structure. The slow lateral etch rate of the sacrificial layer and difficulties

Received: November 21, 2012
Revised: December 8, 2012
Published: December 18, 2012

   dx.doi.org/10.1021/nl304310x | *Nano Lett.* 2013, 13, 315–320

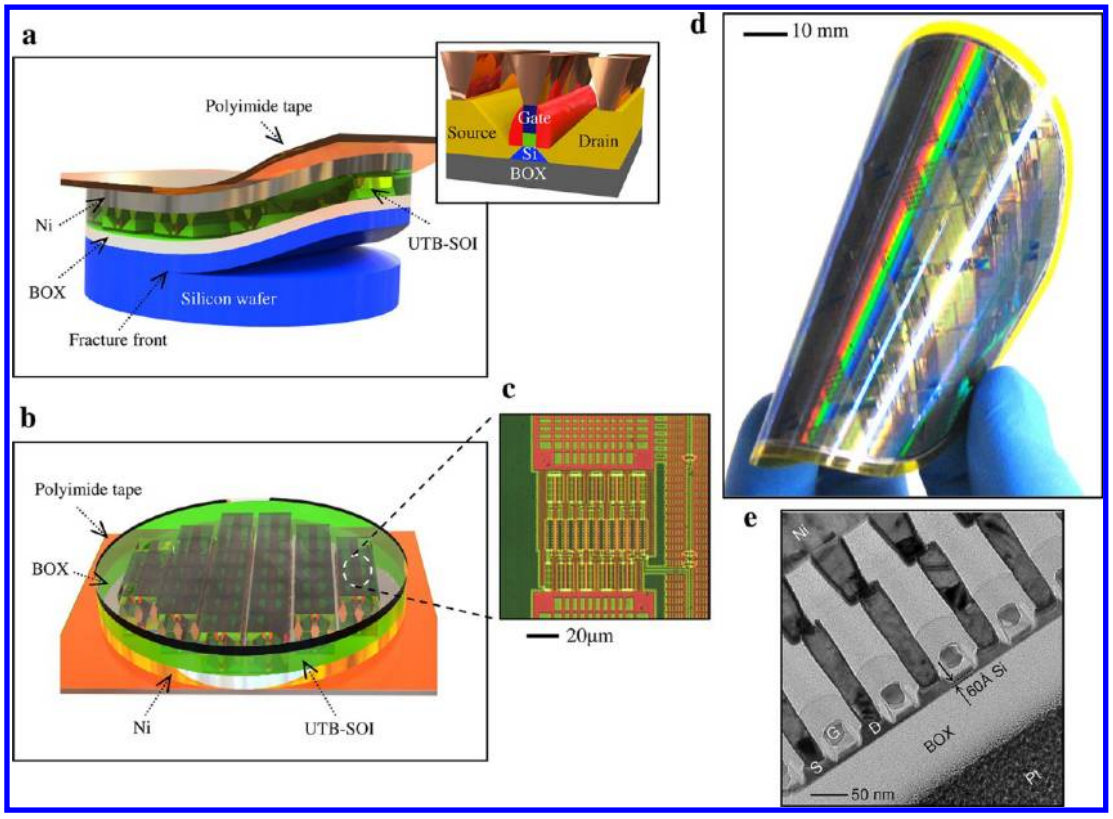


Figure 1. Flexible nanoscale fully depleted transistors and integrated circuits enabled by the controlled spalling technology. (a) Schematic illustration of the controlled spalling process used for removing the prefabricated devices and circuits from the rigid silicon handle wafer. The inset schematically shows the device architecture for the UTB transistors with raised source/drain regions. (b) The post-spalling process involving the selective removal of the residual Si. (c) Optical microscope image of a 100-stage RO from the backside of the circuit through the BOX. (d) Photograph of a 100 mm UTB-SOI flexible circuit. (e) Representative cross-sectional TEM image of nanoscale ultrathin n- FETs, confirming the structural integrity of the flexible devices.

in handling the free-standing thin film semiconductor particularly during the release process restrict the use of ELO when large-size wafers are used. In the case of ELTRAN process, a rather sophisticated process is used to create a cavity underneath the silicon active layer.[21] This tends to further complicate the integration process as the built-up stress during device fabrication and interconnect process can potentially lead to premature failure of the silicon cantilevers. Although the above examples represent major advances in demonstrating high-performance flexible electronics, they call for sophisticated equipment and engineered substrates. Furthermore, the demonstration of extremely bendable ultralight integrated circuits with deeply scaled transistors is still missing in the literature.

Ultrathin body silicon on insulator (UTB-SOI) devices with a body thickness (T_{si}) of 60 Å were chosen in this work because of the unique device properties that originate from the ultrathin channel. The ultrathin body of the silicon channel allows aggressive scaling of the channel length into sub-30 nm range without incurring the deleterious short channel effects because of the excellent gate control.[25] The fabrication process for the complementary metal−oxide semiconductor (CMOS) integrated circuits on rigid (001) UTB-SOI substrates have been described previously.[26] The flexible p- and n-type field-effect transistors (p- and n-FETs) reported here have a gate length of <30 nm with a contacted gate pitch of 100 nm. To realize high-performance flexible circuits, the controlled spalling technique was applied to the rigid and fully fabricated circuits consisting of the ultrathin body silicon transistors and the metal interconnect levels. Figure 1 schematically illustrates the fabrication process, highlighting the key processing details. The controlled spalling process[27,28] was performed at room temperature to remove the top ∼10−15 μm of the substrate, comprising of the prefabricated devices and circuits, from a selected region of a 300 mm wafer. To perform the controlled spalling process, a tensile Ni stressor layer with a stress level of 485 MPa was deposited using dc magnetron sputtering at the base pressure of 1×10^{-6} Torr at room temperature to a thickness of 5.5 μm. The intrinsic stress and the thickness of the stressor layer were chosen to satisfy the conditions in accordance with the previously published models.[28,29] A thin polyimide tape was then applied onto the surface to mechanically guide a single spalling-mode fracture across the wafer in a controllable manner (Figure 1a). The fracture was initiated using the stress discontinuity at one edge of the wafer at room temperature.[27] Because the fracture occurred in the substrate roughly 10 μm below the BOX layer, it is desirable to remove the excess silicon layer underneath the BOX to maximize the flexibility of the final circuit. The selective chemical removal of the residual silicon was performed in tetramethylammonium hydroxide (TMAH) solution, illustrated in Figure 1b. After this step, the device and circuit layouts are revealed from the backside, owing to the optically transparent thin BOX and silicon layers. The optical image in Figure 1c shows the circuit layout for a 100-stage ring oscillators (ROs) from the backside through the BOX. The photograph of the

dx.doi.org/10.1021/nl304310x | Nano Lett. 2013, 13, 315−320

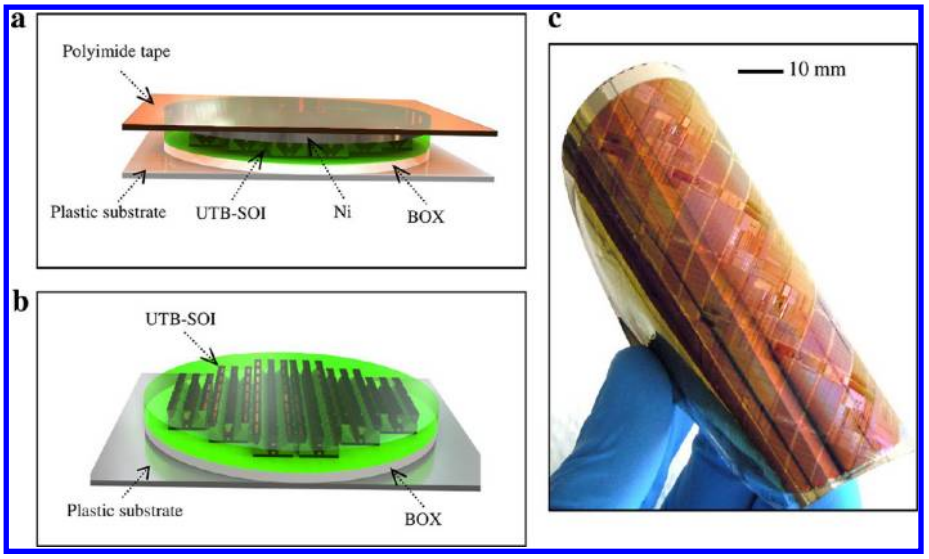


Figure 2. Strategy for producing extremely flexible integrated circuits. (a) Transfer of the thin-film sample in Figure 1d onto another flexible substrate. (b) Removal of the polyimide tape and the relatively thick Ni layer. (c) Photograph of a 100 mm flexible UTB-SOI circuit prepared using this strategy, illustrating the high level of the mechanical flexibility of the circuits.

flexible ultrathin silicon integrated circuits is shown in Figure 1d. Cross-sectional transmission electron microscopy (TEM) was subsequently performed to examine the structural properties of the flexible devices. The TEM image in Figure 1e shows the architecture and physical dimensions of a representative flexible nanoscale transistor, sandwiched between the Ni stressor and the BOX layers. Furthermore, the TEM studies confirmed the structural integrity of the devices, while no discernible crystalline defect was found in the silicon channel as a result of the layer transfer process.

To implement mechanically flexible circuits employing the controlled spalling technology, we identified two possible approaches. The first approach simply utilizes the combination of the Ni film and the tape as the flexible surrogate substrate, as described earlier. This approach is particularly easy to implement, though it offers a limited degree of mechanical flexibility, because of very large Young's modulus of Ni (~200 GPa). This implementation calls for an additional design consideration to allow the possibility of electrical access to the chip from the backside by forming contact pads through the BOX layer. Another approach, which results in improved flexibility, involves the transfer of the spalled film onto another flexible substrate followed by the removal of the polyimide tape and the Ni stressor layer, schematically illustrated in Figure 2a,b. Figure 2c shows the photograph of a flexible circuit after the completion of the second transfer process, revealing the original contact pads on the surface of the chip following the selective removal of the stressor layer.

The extremely thin nature of the fabricated flexible circuits makes the electrical measurement and consequently the assessment of the device properties challenging. When initial electrical measurements were made on the flexible sample in Figure 2c, the local plastic deformation of the device pads was observed because of the exerted pressure by the probe tips (see the Supporting Information, Figure S1). Comparison of the electrical characteristics of the same devices measured before and after the layer transfer process indicated significant degradation of the p-FET performance, while the n-FET device characteristics appear to have remained nearly unchanged, shown in Figure 3 (see the Supporting Information

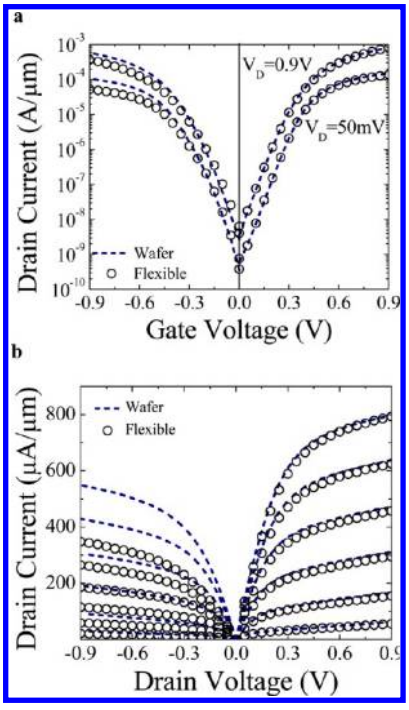


Figure 3. Representative electrical characteristics of n- and p-FETs with a channel length of 20 nm on the flexible sample shown in Figure 2c. (a) Transfer and (b) output characteristics of the same devices were measured before and after the layer transfer process, indicating significant degradation of the on current for p-FETs, while n-FET device characteristics appeared to be unchanged.

for the full analysis of the flexible devices). To verify that the source of p-FET degradation was due to the influence of the probe pressure, the flexible circuit in Figure 1d was rigidly bonded onto a silicon handle wafer using conductive epoxy (Ablebond 2030 SC) at 80 °C. The Ni layer and the tape were then removed to expose the device pads for electrical measurements.

To examine fully the possible effect of the controlled spalling process on the characteristics of the flexible integrated circuits,

dx.doi.org/10.1021/nl304310x | Nano Lett. 2013, 13, 315–320

hundreds of devices including n- and p-FETs, ROs, and static random access memory (SRAM) cells were measured. The comparison of the performance data before and after the layer transfer for both the n- and p-FETs is shown in Figure 4. The

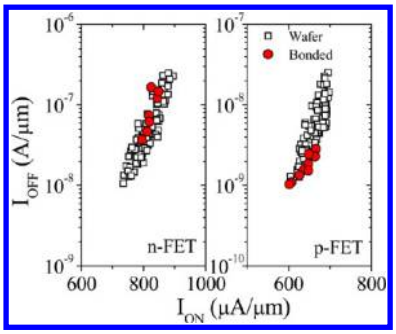


Figure 4. Comparison of the n- and p-FET device performance before and after the layer transfer. The equivalency of the device performance was confirmed by bonding the flexible sample in Figure 1d rigidly onto a silicon handle wafer prior to electrical measurements, eliminating the detrimental influence of the probe pressure on the electrical characteristic of the flexible devices.

off- and on-state currents were extracted from the transfer characteristics of the transistors measured at a drain bias of 0.9 V. As is evident from the data, the performance of the transistors appears to be unchanged. The slight difference in the device performance can be explained by the observed threshold voltage shift (V_{th}) to the negative direction (~30 mV) for both the n- and p-FETs compared to their original characteristics. The origin of the V_{th} shift is unknown, though it could conceivably be attributed to the introduction of some positively fixed charges during the bonding process, particularly because no change in V_{th} was observed for the flexible devices shown in Figure 3. Owing to the intrinsic biaxial tensile stress of the Ni layer used for the controlled spalling process, the thin-film semiconductor will be under residual biaxial compressive stress as a result of the stress sharing. The residual compressive stress in the semiconductor did not appear to impact the electrical properties of the devices. The average compressive strain in the ultrathin silicon was simply measured from the displacement of the alignment marks on the thin-film samples relative to their original spacing before the layer transfer (see Supporting Information, Figure S5). The average compressive strain was found to be nearly the same (~0.15−0.18%) for both the flexible and the bonded samples.

An SRAM cell is the integral element of SoC integrated circuits. The inset in Figure 5a shows the circuit diagram of an SRAM cell that is composed of six transistors (6T-SRAM). The excellent subthreshold characteristics in conjunction with the lack of random dopant fluctuations for the UTB transistors, owing to their undoped ultrathin channel, allow reliable operation of the SRAMs at small power supply voltages (V_{dd}). Accordingly, this feature makes the UTB SRAMs suitable for applications that benefit from ultra low-power integrated circuits. The butterfly curves for a flexible SRAM cell with an area of 0.136 μm^2 are shown in Figure 5a, illustrating the functionality of the memory cell with a good symmetry down to V_{dd} of 0.6 V. Another example of a deeply scaled flexible integrated circuit with a higher level of integration complexity involved the demonstration of functional 100-stage ROs with fanout of 3. The schematic of the circuit and the SEM image of the layout that was taken from the backside through the BOX

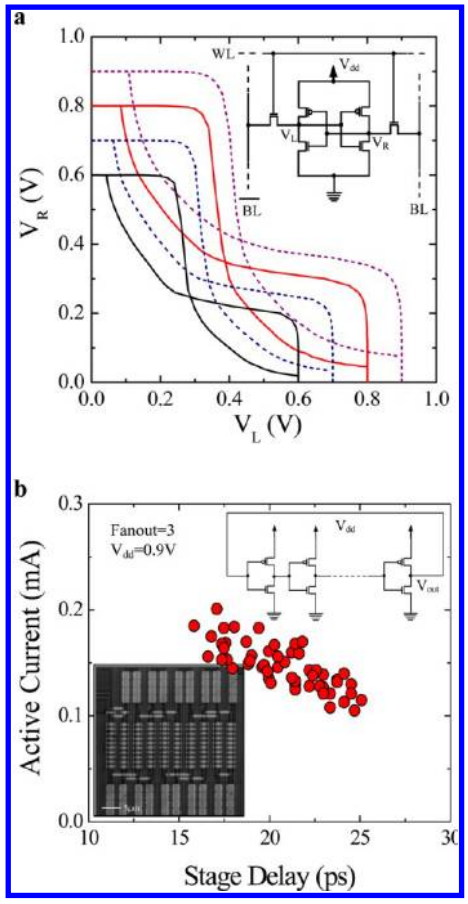


Figure 5. Ultradense high-performance flexible memory and ring oscillator circuits. (a) The representative butterfly curves for a flexible SRAM, showing good symmetry down to V_{dd} of 0.6 V. The inset shows the schematic illustration of a 6T-SRAM cell. (b) Stage delay characteristics of the flexible ring oscillators, indicating a record stage delay of ~16 ps. The top and bottom insets illustrate the circuit diagram of a multistage ring oscillator and the SEM image of a flexible 100-stage ring oscillator taken from the backside of the sample through the BOX, respectively.

are shown in the top and bottom insets in Figure 5b, respectively. The plot in Figure 5b shows the measured stage delay characteristics for a large number of flexible ROs on the flexible sample, exhibiting a stage delay as low as 16 ps at V_{dd} = 0.9 V, the best reported delay for any flexible circuit.

Bending stability is an important factor when considering the suitability of a technology for applications in flexible electronics. Bending tests were performed using circular cylinders with different radii of curvature (R) from 6.3 to 15.8 mm, shown in Figure 6a. Figure 6b shows the transfer characteristics of an n-FET under different tensile bending conditions, exhibiting slight V_{th} shift to smaller values (ΔV_{th} = 35 mV at R = 6.3 mm). In these experiments, the bending was performed along the direction of the current flow in the [110] channel direction. The level of the bending tensile strain, ε_b, for the flexible devices was estimated to be ~0.95% at R = 6.3 mm using the following expression:

$$\varepsilon_b = \frac{t}{2R}$$

where R is the bending radius and t is the total thickness of the flexible sample including the tape and the thin-film semiconductor. The observed shift in V_{th} of the n-FET device is

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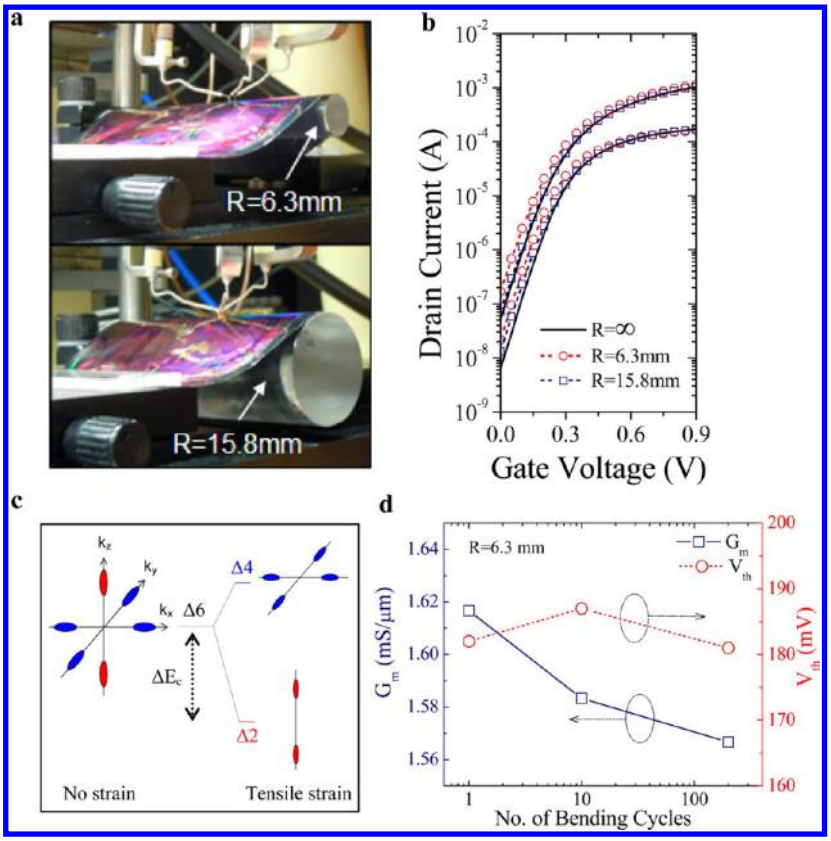

Figure 6. Bending stability of the flexible circuits. (a) Photograph of a flexible circuit under tensile bending tests at two different radii of curvature. (b) Transfer characteristics of an n-FET with a channel length of 20 nm under different bending conditions. (c) The bending tensile strain causes the 6-fold symmetry of the silicon conduction band to break, resulting in a shift in the threshold voltage of the n-FETs. (d) No noticeable change in device properties was observed during the repeated bending test at R = 6.3 mm.

attributed to the strain-induced change in the silicon conduction band by breaking the 6-fold symmetry,[30,31] depicted in Figure 6c. Furthermore, bending endurance of the n-FETs was successfully demonstrated up to 200 cycles at R = 6.3 mm without any noticeable change in device characteristics, shown in Figure 6d.

The present study demonstrated nanoscale highly integrated flexible circuits on 60 Å thick silicon. This outcome was achieved by exploiting the controlled spalling technology as a simple and cost-effective solution for implementing high-performance flexible integrated circuits. The unique attributes of the ultrathin body silicon technology in conjunction with the simplicity of the controlled spalling technique can create new possibilities for the silicon-based flexible nanoelectronics, particularly in applications demanding a staggering level of functionality. The controlled spalling process has been previously applied to entire 300 mm wafers,[28] as well as selected areas of the surface as in the present study. Nevertheless, for some flexible electronics applications consisting of various subsystems including circuits, energy harvesters, transceivers, and sensors, the integrated circuits are not required at full coverage, because of system design considerations and cost implications. The fact that controlled spalling is able to remove layers of arbitrary size and shape allows one to design the circuits and subsystems at the wafer scale and selectively remove them by selected deposition of the stressor layer on these regions. This notable feature of our approach can potentially eliminate the need for subsequent handling and transfer of small chips to a foreign substrate using costly pick-and-place equipments.

■ ASSOCIATED CONTENT

Supporting Information

Effect of probe tips on flexible devices, method of calculating residual strain in transferred layers, Figures S1–S5. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The UTB-SOI devices used in this work were fabricated at Albany Nanotech and IBM East Fishkill facilities. The authors wish to gratefully acknowledge A. Khakifirooz for helpful discussions, K. Cheng for providing the UTB-SOI device wafers, K. Fogel and P. Lauro for their help with the controlled spalling process, and J. A. Ott for the TEM studies. The UTB-SOI wafers used in this study are from the early stage of the UTB-SOI technology development and do not represent the best devices. All authors have equally contributed to this work.

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