# Fast and slow transient charging in various III-V field-effect transistors with atomic-layer-deposited-Al2O3 gate dielectric

Michael E. Ramón, Tarik Akyol, Davood Shahrjerdi, Chadwin D. Young, Julian Cheng, Leonard F. Register, and Sanjay K. Banerjee

Citation: Applied Physics Letters **102**, 022104 (2013); doi: 10.1063/1.4776678
View online: http://dx.doi.org/10.1063/1.4776678
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/102/2?ver=pdfcov
Published by the AIP Publishing

# Fast and slow transient charging in various III-V field-effect transistors with atomic-layer-deposited-$Al_2O_3$ gate dielectric

Michael E. Ramón,[1,a)] Tarik Akyol,[1] Davood Shahrjerdi,[2] Chadwin D. Young,[3] Julian Cheng,[1] Leonard F. Register,[1] and Sanjay K. Banerjee[1]
[1]*Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78758, USA*
[2]*IBM T.J. Watson Research Center, 1101 Kitchawan Road, Route 134, Yorktown Heights, New York 10598, USA*
[3]*Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, Texas 75080, USA*

(Received 8 October 2012; accepted 31 December 2012; published online 16 January 2013)

We report measurement of fast transient charging effects (FTCE) in enhancement-mode n-channel GaAs, InP, and $In_{0.53}Ga_{0.47}As$ field-effect transistors (FETs) using $Al_2O_3$ as the gate dielectric. The FTCE data reveal superior drive current and enhanced threshold voltage stability for $In_{0.53}Ga_{0.47}As$ FETs. We further report charge pumping measurements for $In_{0.53}Ga_{0.47}As$ transistors, revealing that the majority of interface traps are donor traps, as well as an increased trap density within the $Al_2O_3$ bulk. Such data, together with FTCE data, reveal that drain current degradation observed during pulsed *I-V* measurements is predominantly due to slow oxide traps, underscoring their significance within III-V/high-$\kappa$ metal-oxide-semiconductor FETs. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4776678]

High mobility III-V substrates have continued to attract great interest as replacement channel materials to meet the performance demands beyond the limits of silicon (Si) complementary metal-oxide-semiconductor (CMOS) technology. Progress has been made on enhancement-mode III-V MOS field-effect transistors (MOSFETs), including MOSFETs on GaAs,[1,2] InP,[3,4] and InGaAs[5,6] utilizing various high-$\kappa$ dielectrics such as $Al_2O_3$,[2,5] $HfO_2$,[1,3,5] HfAlO,[5] stacked $HfAlO_x/HfO_2$,[4] and stacked $HfO_2/AlN$,[6] among others. However, the high trap density which typically characterizes high-$\kappa$ dielectrics and the III-V/high-$\kappa$ dielectric interface remains a challenge for future III-V substrate integration. In particular, the transient charging of fast interface traps present at III-V/high-$\kappa$ dielectric interface, as well as the charging of slow, near-interface oxide traps can cause mobility degradation, threshold voltage ($V_t$) instability, and reduced transistor reliability.[7,8] To better understand III-V device performance, it is important to characterize the impact of charge traps within the gate stack of III-V MOSFETs as well as at the III-V/dielectric interface. In this work, a pulsed I-V measurement technique[7–11] is used to assess the impact of fast transient charging effects (FTCE), wherein substrate-injected electrons become trapped in pre-existing defects within the high-$\kappa$ dielectric,[8] on GaAs, InP, and $In_{0.53}Ga_{0.47}As$ MOS transistors with $Al_2O_3$ gate dielectric deposited by atomic layer deposition (ALD). Moreover, the pulsed *I-V* technique is used to provide insight into the impact of slow, near-interface oxide traps by employing variable, long pulse widths (PWs). $In_{0.53}Ga_{0.47}As$ FETs are found to show high drive current as compared to GaAs and InP FETs, as reported elsewhere,[5,6] and are found to be least impacted by FTCE. To better understand the nature of trapping in the III-V/high-$\kappa$ system, the charge pumping (CP) technique[12] was also used to directly measure the trap recombination current and accurately determine the interfacial trap density ($D_{it}$) in the $In_{0.53}Ga_{0.47}As$ MOSFETs. The charge pumping technique has been recently used to extract $D_{it}$ in III-V/high-$\kappa$ systems[13,14] and is further used here to shed light on the FTCE data. For example, utilizing a frequency-dependent charge pumping technique,[15,16] the trap density within the $Al_2O_3$ dielectric has also been profiled, providing further understanding into the contribution of slow traps away from the III-V/high-$\kappa$ interface. Further, the present charge pumping analysis was used to extract the energy distribution of $D_{it}$ within the bandgap.

GaAs-based transistors were fabricated on (100) undoped semi-insulating substrates, which were initially cleaned in a 1% HF solution to remove surface oxides, followed by a 20% $(NH_4)_2S$ dip surface passivation treatment, which has been previously demonstrated to effectively improve the GaAs substrate/high-$\kappa$ gate dielectric interface.[2,17] After the surface treatment, the GaAs wafers were immediately transferred into an ALD reactor, where $Al_2O_3$ was grown using trimethyl aluminum (TMA) as the metallic precursor and $H_2O$ as the oxidant. Selective removal of GaAs native oxides using TMA precursor has been reported previously,[18] and helps eliminate the need for an elaborate *in situ* clean. Physical vapor deposited (PVD) TaN was used as the gate electrode and the source/drain ohmic contacts were formed by e-beam evaporation and lift-off of AuGe/Ni/Au. The complete GaAs MOSFET process flow has been previously described.[2] Semi-insulating (100) InP substrates were used for InP MOSFET fabrication, and molecular beam epitaxy (MBE)-grown p-type $In_{0.53}Ga_{0.47}As$ on highly doped p-type InP substrates were used for $In_{0.53}Ga_{0.47}As$ MOSFET fabrication using a similar process flow as described above. All devices were fabricated using a ring-FET geometry with an annular gate, useful for simplifying the device isolation process.[6]

a)Electronic mail: michael.ramon@utexas.edu.

 

Figure 1(a) depicts a schematic illustration of the pulsed *I-V* measurement setup used to study FTCE in our high-$\kappa$ III-V MOS transistors. To illustrate the impact of FTCE, Figure 1(b) shows a pulsed *I-V* measurement [rise time ($t_r$) = fall time ($t_f$) = 10 $\mu$s, $PW = 100\ \mu$s] on a GaAs transistor, where the difference in the forward and reverse $I_d$-$V_g$ sweeps is a result of transient charge trapping, and is a direct cause of threshold voltage ($V_t$) instability.[8,10] Comparing the forward pulsed $I_d$-$V_g$ sweep to the DC sweep illustrates the underestimation of the drive current due to trapping occurring during the DC measurement. While transient charging may still occur for pulses in the $\mu$s-range,[8] the pulsed $I_d$-$V_g$ sweep is closer to being "trap-free." Figure 1(c) illustrates the drive current degradation as a function of time corresponding to the pulsed $I_d$-$V_g$ sweep of Figure 1(b). The reduction in drive current is caused by the increasing $V_t$ due to charge trapping within the high-$\kappa$ during the pulse charging time, where the charging time is defined as the sum of the rise time ($t_r$) and the *PW*.[8,10] The FTCE phenomenon has also been observed for Si-based transistors with high-$\kappa$ gate dielectrics.[7]

When studying pulsed current data, it is preferable to use $I_d$-time sweeps (Figure 1(c)) as opposed to $I_d$-$V_g$ sweeps (Figure 1(b)) because of artifacts that can be present in $I_d$-$V_g$ data,[8,10,19] such as variable values of $V_t$ shift observed at different values of drain current, resulting from forward/reverse $I_d$-$V_g$ traces that are not parallel to one another. Thus, to compare the impact of FTCE across various III-V/$Al_2O_3$ devices, $I_d$-time sweeps for (a) GaAs, (b) InP, and (c) $In_{0.53}Ga_{0.47}As$ MOSFETs (W/L = 600 $\mu$m/5 $\mu$m) as a function of *PW* are presented (Figure 2). For each substrate type, four different pulse widths were used (5 ms, 10 ms, 50 ms, 100 ms), while holding the rise time and fall time constant (0.1 $\mu$s). A superior drive current for $In_{0.53}Ga_{0.47}As$-based devices is observed, and has been reported elsewhere.[5,6] The initial rapid decrease in drain current with time is due to fast traps, while the continued decay with time is due to the ability of slower near-interface oxide traps to respond for increased charging times.[20] For a maximum charging time of ~100 ms, $In_{0.53}Ga_{0.47}As$, GaAs, and InP MOSFETs each experience a drain current degradation of ~18%, ~25%, and ~42%, respectively, indicative of increased $V_t$ instability of GaAs and InP devices as compared to their $In_{0.53}Ga_{0.47}As$ counterparts. In light of the higher drive current of $In_{0.53}Ga_{0.47}As$, its more forgiving nature with regards to Fermi-level pinning,[5] and the present results showing less susceptibility to FTCE, it is worthwhile to probe further into the nature of traps in the $In_{0.53}Ga_{0.47}As/Al_2O_3$ system.

Toward that end, the 2-level CP technique[12–16,21–23] was used to accurately determine $D_{it}$ in the $In_{0.53}Ga_{0.47}As$ MOSFETs, as well as the trap density within the $Al_2O_3$ dielectric and the energy distribution of $D_{it}$ within the bandgap. GaAs and InP-based devices, which have semi-insulating substrates, did not allow for similar probing of the trap recombination current. The charge pumping measurements were performed by keeping the source, drain, and substrate grounded while ramping the base level ($V_{base}$) from −2 V to 0 V of a constant amplitude ($V_a = 2$ V) gate pulse. In order to avoid the impact of bulk traps,[13] high frequency (1 MHz) charge pumping current ($I_{cp}$) versus $V_{base}$, with fixed rise and fall times (100 ns) was used (not shown) to compute the mean $D_{it}$[12,23]

$$\frac{I_{cp}}{f} = 2q\overline{D_{it}}AkT\left\{\ln\sqrt{t_r t_f} + \ln\left(\frac{|V_{fb} - V_t|}{|V_a|}\upsilon_{th} n_i \sqrt{\sigma_n \sigma_p}\right)\right\}, \tag{1}$$

where $f$ is the measurement frequency, $q$ is the electron charge, $\overline{D_{it}}$ is the mean interfacial trap density, $A$ is the device area (W*L = 600 $\mu$m*5 $\mu$m), $kT$ is the product of the Boltzmann constant and temperature (0.0259 eV), $t_r$ and $t_f$ are the pulse rise and fall times (100 ns), $V_{fb}$ and $V_t$ are the flatband and threshold voltages and $|V_{fb} - V_t| \sim 1.5$ V as estimated from Figure 3, $\upsilon_{th}$ is the thermal velocity ($1 \times 10^7$ cm/s), $n_i$ is the intrinsic carrier concentration ($1 \times 10^{12}$ cm$^{-3}$), and $\sigma_n$ and $\sigma_p$ are the electron and hole capture cross sections, respectively. By performing a linear fit of the $I_{CP}/f$ vs. $\ln(t_r t_f)^{1/2}$ curve while keeping $t_r$ fixed (not shown),[23] the electron capture cross section ($\sigma_n$) is extracted to be $\sim 1.52 \times 10^{-13}$ cm$^2$. Similarly, from a linear fit of the $I_{CP}/f$ vs. $\ln(t_r t_f)^{1/2}$ curve while keeping $t_f$ fixed (not shown), the hole capture cross section ($\sigma_p$) is found to be $\sim 6.34 \times 10^{-15}$ cm$^2$. The mean capture cross section can then be extracted as $\sqrt{\sigma_n \sigma_p} \sim 3.11 \times 10^{-14}$ cm$^2$. For a peak measured $I_{cp}$ value of 11.63 $\mu$A, the mean $D_{it}$ is thus found to be $1.24 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$, which is comparable to previously reported values.[14,15] Moreover, the interface traps in InGaAs devices are predominantly donor traps which reside in the upper half of the bandgap, as will be discussed below, and thus they do not affect the on-state performance of InGaAs transistors.[14]

Figure 3(a) shows a strong influence of varying fall time on $I_{cp}$ while keeping the rise time fixed at 100 ns (~53% $I_{cp}$

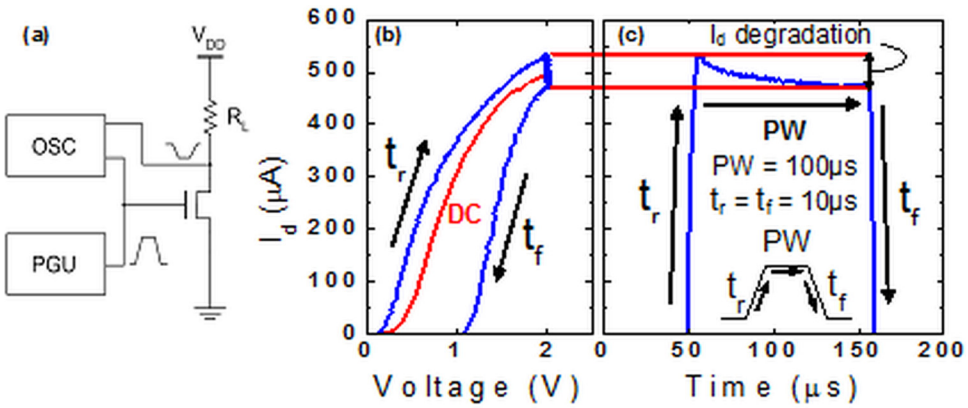


FIG. 1. (a) Schematic illustration of the pulsed *I-V* measurement setup used to study FTCE in our high-$\kappa$ III-V MOS transistors. (b) Pulsed *I-V* measurement [rise time ($t_r$) = fall time ($t_f$) = 10 $\mu$s, $PW = 100\ \mu$s] on a GaAs transistor, illustrating the impact of FTCE. (c) Drive current degradation as a function of time corresponding to the pulsed $I_d$-$V_g$ sweep shown in (b).

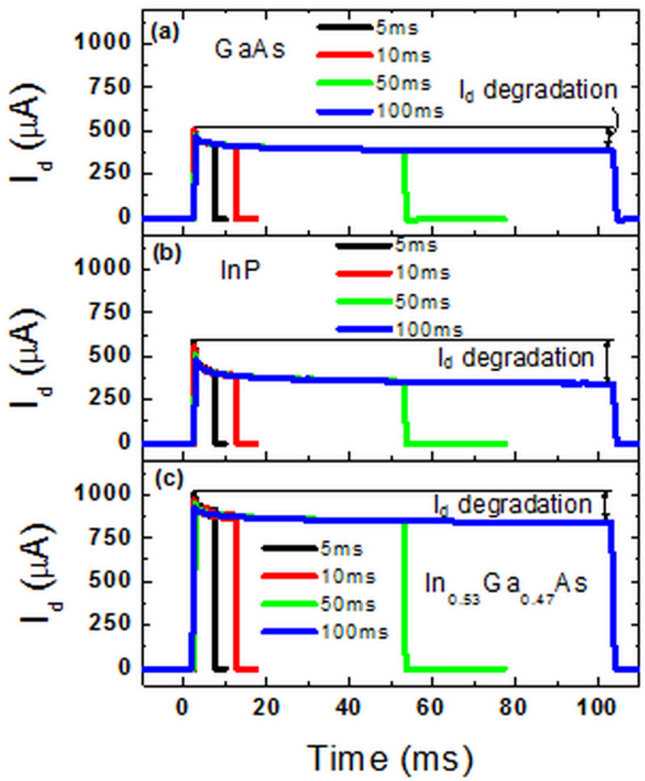


FIG. 2. $I_d$-time sweeps for (a) GaAs, (b) InP, and (c) $In_{0.53}Ga_{0.47}As$ MOSFETs (W/L = 600 $\mu$m/5 $\mu$m) as a function of *PW*. For each substrate type, four different pulse widths were used (5 ms, 10 ms, 50 ms, 100 ms), while holding the rise time and fall time constant (0.1 $\mu$s).

degradation), and Figure 3(b) shows a weak influence of varying rise times on $I_{cp}$ while keeping the fall time fixed at 100 ns (~11% $I_{cp}$ degradation). These results, together with the much larger electron capture cross section, indicate that the majority of interface traps in InGaAs are in fact donor traps, residing in the upper half of the bandgap.[21,23] The larger electron capture cross section also underscores that donor traps above midgap are more effective trapping centers than acceptor traps in the lower half of the bandgap, as expected since the trapping time constant is inversely proportional to the capture cross section.[12] It should be noted that while the on-state drive current and threshold voltage are unaffected for the case of donor traps, they do have a detrimental impact on off-state performance, including subthreshold slope (SS), ON/OFF current ratio, and drain-induced barrier lowering.[14,15] The $In_{0.53}Ga_{0.47}As$ devices used for the present charge pumping study exhibited an ON/OFF current ratio of ~$10^4$ and a SS of ~150 mV/dec, as extracted from the device transfer curve (not shown). Previously presented $In_{0.53}Ga_{0.47}As$ devices having comparable ON/OFF current ratio and SS also exhibited similar values of $D_{it}$.[6]

To probe the slow, near-interface oxide traps in the $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSFETs, a frequency dependent charge pumping technique[15,16] was used. Figure 4(a) shows the charge pumped per cycle ($Q_{cp} = I_{cp}/f$) versus frequency. As shown, the charge pumped per cycle increases with decreasing frequency, as there is more time for electrons to tunnel into traps deeper into the $Al_2O_3$ bulk. Without near-interface oxide traps, $Q_{cp}$ remains constant.[12] Such behavior is consistent with other reports[15] and with what is known regarding the high trap density of high-$\kappa$ dielectrics in general.[8] The profile of the bulk trap density ($N_{ot}$) away from the $In_{0.53}Ga_{0.47}As/Al_2O_3$ interface and into the $Al_2O_3$ is shown in Figure 4(b), and was extracted using the data of Figure 4(a) and the following equations:[22]

$$N_{ot}(x_{\min}) = -\frac{1}{q\lambda_{e,h}A\Delta E}\frac{dQ_{cp}}{d\ln f}, \tag{2}$$

$$x_{\min} = \min(x_e, x_h) = \min(-\lambda_e \ln\{c_n(0)/[\ln(0.5)2f]\}, -\lambda_h \ln\{c_p(0)/[\ln(0.5)2f]\}), \tag{3}$$

$$c_n(0) = n_s\sigma_n(0)\upsilon_{th}, \tag{4}$$

$$c_p(0) = p_s\sigma_p(0)\upsilon_{th}, \tag{5}$$

where $x_{min}$ is the oxide depth which corresponds to the carrier type which limits recombination, $\lambda_e$ and $\lambda_h$ are the electron and hole tunnel attenuation coefficients, $\Delta E$ is the bandgap energy scanned, $c_n$ and $c_p$ are the capture rates

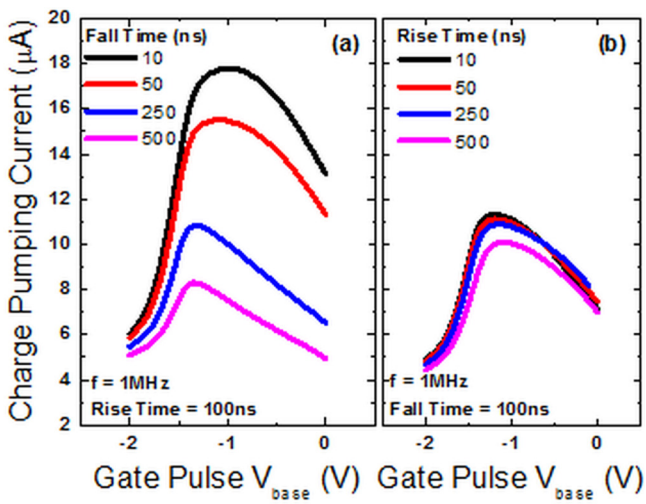


FIG. 3. (a) Strong dependence of $I_{cp}$ with varying fall time, while rise time is fixed at 100 ns (~53% $I_{cp}$ degradation). (b) Weak dependence of $I_{cp}$ with varying rise time while keeping fall time fixed at 100 ns (~11% $I_{cp}$ degradation). $f$ = 1 MHz for all measurements.

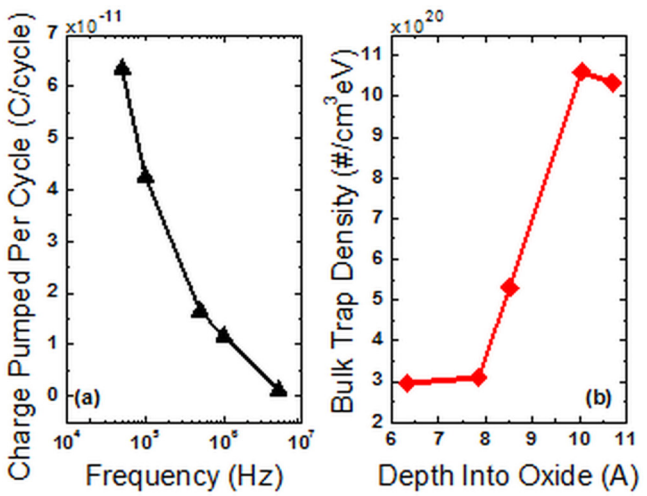


FIG. 4. (a) Charge pumped per cycle ($Q_{cp} = I_{cp}/f$) versus frequency. (b) Profile of bulk trap density ($N_{ot}$) in $Al_2O_3$, extracted using the data shown in (a).

for electrons and holes, and $n_s$ and $p_s$ are the electron and hole surface carrier concentrations when the device is alternately driven into either inversion or accumulation by the gate pulse. For the present calculations, values of $\lambda_e = \lambda_h = 0.95$ Å for the InGaAs/$Al_2O_3$ system,[15] $\Delta E = 0.48$ eV which is a weighted average of the energy window scanned by the frequency-dependent CP measurement,[15] $\sigma_n = 1.52 \times 10^{-13}$ cm$^2$, and $\sigma_p = 6.34 \times 10^{-15}$ cm$^2$ were used. Using basic semiconductor equations,[24] the known $In_{0.53}Ga_{0.47}As$ p-type doping concentration ($N_A = 8.5 \times 10^{16}$ cm$^{-3}$), an $In_{0.53}Ga_{0.47}As$ intrinsic carrier concentration of $n_i = 1 \times 10^{12}$ cm$^{-3}$,[25] and assuming that the device is driven into strong inversion when the gate pulse is high and into accumulation when the gate pulse is low, we estimate that $n_s = 8.53 \times 10^{16}$ cm$^{-3}$ and $p_s \sim N_A = 8.5 \times 10^{16}$ cm$^{-3}$. The pulse rise/fall times were fixed at 100 ns, and the pulse amplitude ($V_a$) was set to 2 V. The bulk trap density is found to be $\sim 3 \times 10^{20}$ cm$^{-3}$ eV$^{-1}$ near the interface and increases away from the $In_{0.53}Ga_{0.47}As/Al_2O_3$ interface, exhibiting a peak concentration of $\sim 1.05 \times 10^{21}$ cm$^{-3}$ eV$^{-1}$ approximately 10 Å into the oxide. While these values are high, they are within the expected range for deposited high-$\kappa$ gate dielectrics.[15] Furthermore, the increased trap density observed within the $Al_2O_3$ dielectric supports the idea that the drain current degradation with increasing pulse width time, as shown in the FTCE data of Figure 2, is predominantly due to slower traps within the oxide responding to increased charging times.

The energy distribution of $D_{it}$ within the $In_{0.53}Ga_{0.47}As$ bandgap (Figure 5) was also found by using the data of Figure 3, in accordance with the following relations:[12,23]

$$E_{em,e} - E_i = -kT \ln\left( \upsilon_{th} n_i \sigma_n \frac{|V_{fb} - V_t|}{|V_a|} t_f + e^{(E_i - E_{f,inv})/kT} \right), \quad (6)$$

$$E_{em,h} - E_i = +kT \ln\left( \upsilon_{th} n_i \sigma_p \frac{|V_{fb} - V_t|}{|V_a|} t_r + e^{(-E_i + E_{f,acc})/kT} \right), \quad (7)$$

$$D_{it}(E_2) = -\frac{t_f}{qAkTf} \frac{dI_{cp}}{dt_f} \quad \text{(rise time constant)}, \quad (8)$$

$$D_{it}(E_1) = -\frac{t_r}{qAkTf} \frac{dI_{cp}}{dt_r} \quad \text{(fall time constant)}, \quad (9)$$

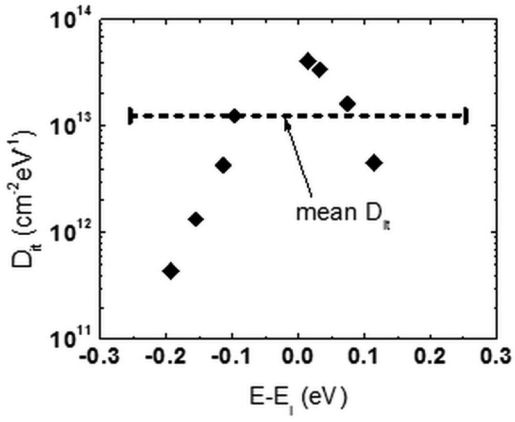


FIG. 5. Energy distribution of $D_{it}$ within the $In_{0.53}Ga_{0.47}As$ bandgap, extracted using the data shown in Figure 3.

where $E_{em,e}$ and $E_{em,h}$ are the energies of the onset of electron and hole emission, respectively. The mean $D_{it}$ ($1.24 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$) is overlaid for reference. As shown, the distribution of $D_{it}$ values in the upper half of the bandgap is approximately an order of magnitude higher than in the lower half of the bandgap, and the density of interface traps peaks at $\sim 4 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$ just above midgap. The $D_{it}$ values reported here are comparable to values reported elsewhere for InGaAs-based devices,[6,13–15] and underscore the previous interpretation of the data shown in Figure 3 that the majority of interface traps in the present $In_{0.53}Ga_{0.47}As$ MOSFETs are in the upper half of the bandgap.

In conclusion, the pulsed $I_d$-$V_g$ technique was used to assess the impact of FTCE in various III-V/$Al_2O_3$ MOSFETs, including GaAs, InP, and $In_{0.53}Ga_{0.47}As$. $In_{0.53}Ga_{0.47}As$-based devices exhibited the highest drive current and showed the least susceptibility to FTCE. The charge pumping technique was also used to measure the mean $D_{it}$, profile the trap density within the $Al_2O_3$ dielectric, and extract the energy distribution of $D_{it}$ within the $In_{0.53}Ga_{0.47}As$ bandgap. Charge pumping results indicated that the majority of interface traps in $In_{0.53}Ga_{0.47}As$ are donor-type traps which reside in the upper half of the bandgap. Further, the increased trap density observed within the $Al_2O_3$ dielectric supports the fact that the drain current degradation with increasing pulse width time, as observed for the pulsed $I_d$-$V_g$ measurements, is predominantly due to slower traps within the oxide which are able to respond at increased charging times and underscores the significant contribution of slow traps for III-V/high-$\kappa$ MOSFETs.

This was supported by the SWAN Emerging Technology Fund of the State of Texas.

[1]I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Self-aligned n- and p-channel GaAs MOSFETs on undoped and p-type substrates using $HfO_2$ and silicon interface passivation layer," Tech. Dig. - Int. Electron Devices Meet. **2006**, 829–832.
[2]D. Shahrjerdi, T. Akyol, M. Ramon, D. I. Garcia-Gutierrez, E. Tutuc, and S. K. Banerjee, "Self-aligned inversion-type enhancement-mode GaAs metal-oxide semiconductor field-effect transistor with $Al_2O_3$ gate dielectric," Appl. Phys. Lett. **92**, 203505 (2008).
[3]Y. Z. Wang, Y. T. Chen, H. Zhao, F. Xue, F. Zhou, and J. C. Lee, "Impact of $SF_6$ plasma treatment on performance of TaN-$HfO_2$-InP metal-oxide-semiconductor field-effect transistor," Appl. Phys. Lett. **98**, 043506 (2011).
[4]H. Zhao, D. Shahrjerdi, F. Zhu, H.-S. Kim, I. Ok, M. H. Zhang, J. H. Yum, S. K. Banerjee, and J. C. Lee, "Inversion-type indium phosphide metal-oxide-semiconductor field-effect transistors with equivalent oxide thickness of 12 angstrom using stacked HfAlO(x)/HfO(2) gate dielectric," Appl. Phys. Lett. **92**, 253506 (2008).
[5]Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High-performance sub-micron inversion-type enhancement-mode InGaAs MOSFET with ALD $Al_2O_3$, $HfO_2$, and HfAlO as gate dielectrics," Tech. Dig. - Int. Electron Devices Meet. **2007**, 637–640.
[6]D. Shahrjerdi, T. Rotter, G. Balakrishnan, D. Huffaker, E. Tutuc, and S. K. Banerjee, "Fabrication of self-aligned enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs with TaN/$HfO_2$/AlN gate stack," IEEE Electron Device Lett. **29**, 557–560 (2008).
[7]C. D. Young, P. Zeitzoff, G. A. Brown, G. Bersuker, B. H. Lee, and J. R. Hauser, "Intrinsic mobility evaluation of high-k gate dielectric transistors using pulsed Id-Vg," IEEE Electron Device Lett. **26**, 586–589 (2005).
[8]C. D. Young, D. Heh, A. Neugroschel, R. Choi, B. H. Lee, and G. Bersuker, "Electrical characterization and analysis techniques for the high-k era," Microelectron. Reliab. **47**, 479–488 (2007).

[9]B. H. Lee, C. D. Young, R. Choi, J. H. Sim, G. Bersuker, C. Y. Kang, R. Harris, G. A. Brown, K. Matthews, S. C. Song, N. Moumen, J. Barnett, P. Lysaght, K. S. Choi, H. C. Wen, C. Huffman, H. Alshareef, P. Majhi, S. Gopalan, J. Peterson, P. Kirsh, H.-J. Li, J. Gutt, M. Gardner, H. R. Huff, P. Zeitzoff, R. W. Murto, L. Larson, and C. Ramiller, "Intrinsic characteristics of high-k devices and implications of fast transient charging effects (FTCE)," Tech. Dig. - Int. Electron Devices Meet. **2004**, 859–862.
[10]G. Bersuker, P. Zeitzoff, J. H. Sim, B. H. Lee, R. Choi, G. Brown, and C. D. Young, "Mobility evaluation in transistors with charge-trapping gate dielectrics," Appl. Phys. Lett. **87**, 042905 (2005).
[11]A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the $V_T$ instability in $SiO_2/HfO_2$ gate dielectrics," in *IEEE 41st Annual IRPS Technical Digest* (2003), pp. 41–45.
[12]G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," IEEE Trans. Electron Devices **31**, 42–53 (1984).
[13]H. C. Chiu, L. T. Tung, Y. H. Chang, Y. J. Lee, C. C. Chang, J. Kwo, and M. Hong, "Achieving a low interfacial density of states in atomic layer deposited $Al_2O_3$ on $In_{0.53}Ga_{0.47}As$," Appl. Phys. Lett. **93**, 202903 (2008).
[14]W. Wang, J. Deng, J. C. M. Hwang, Y. Xuan, Y. Wu, and P. D. Ye, "Charge-pumping characterization of interface traps in $Al_2O_3$/$In_{0.75}Ga_{0.25}As$ metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett. **96**, 072102 (2010).
[15]D. Varghese, Y. Xuan, Y. Q. Wu, T. Shen, P. D. Ye, and M. A. Alam, "Multi-probe interface characterization of $In_{0.65}Ga_{0.35}As/Al_2O_3$ MOSFET," Tech. Dig. - Int. Electron Devices Meet. **2008**, 379–382.
[16]D. Heh, C. D. Young, G. A. Brown, P. Y. Hung, A. Diebold, and G. Bersuker, "Spatial distributions of trapping centers in $HfO_2/SiO_2$ gate stacks," Appl. Phys. Lett. **88**, 152907 (2006).
[17]D. Shahrjerdi, D. I. Garcia-Gutierrez, E. Tutuc, and S. K. Banerjee, "Chemical and physical interface studies of the atomic-layer-deposited $Al_2O_3$ on GaAs substrates," Appl. Phys. Lett. **92**, 223501 (2008).
[18]M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, "$HfO_2$ and $Al_2O_3$ gate dielectrics on GaAs grown by atomic layer deposition," Appl. Phys. Lett. **86**, 152904 (2005).
[19]D. Heh, C. D. Young, R. Choi, and G. Bersuker, "Extraction of the threshold-voltage shift by the single-pulse technique," IEEE Electron Device Lett. **28**, 734–736 (2007).
[20]D. Shahrjerdi, J. Nah, B. Hekmatshoar, T. Akyol, M. Ramon, E. Tutuc, and S. K. Banerjee, "Hall mobility measurements in enhancement-mode GaAs field-effect transistors with $Al_2O_3$ gate dielectric," Appl. Phys. Lett. **97**, 213506 (2010).
[21]T. Aichinger and M. Nelhiebel, "Advanced energetic and lateral sensitive charge pumping profiling methods for MOSFET device characterization—analytical discussion and case studies," IEEE Trans. Device Mater. Reliab. **8**, 509–518 (2008).
[22]Y. Maneglia and D. Bauza, "Extraction of slow oxide trap concentration profiles in metal-oxide-semiconductor transistors using the charge pumping method," J. Appl. Phys. **79**, 4187–4192 (1996).
[23]J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, and J. S. Suehle, "Energy distribution of interface traps in high-K gated MOSFETs," Dig. Tech. Pap. - Symp. VLSI Technol. **2003**, 161–162.
[24]B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th ed. (Pearson Education, New Jersey, 2006).
[25]C. Carmody, H. H. Tan, and C. Jagadish, "Electrical isolation of n- and p-$In_{0.53}Ga_{0.47}As$ epilayers using ion irradiation," J. Appl. Phys. **94**, 6616–6620 (2003).