ECS Journal of Solid State
Science and Technology

The Electrochemical Society
Advancing solid state & electrochemical science & technology

OPEN ACCESS

Highly Non-linear and Reliable Amorphous Silicon Based Back-to-Back Schottky Diode as Selector Device for Large Scale RRAM Arrays

To cite this article: Cheng-Chih Hsieh *et al* 2017 *ECS J. Solid State Sci. Technol.* **6** N143

View the article online for updates and enhancements.

This content was downloaded from IP address 216.165.95.84 on 29/08/2020 at 16:35

Highly Non-linear and Reliable Amorphous Silicon Based Back-to-Back Schottky Diode as Selector Device for Large Scale RRAM Arrays

Cheng-Chih Hsieh,[a] Yao-Feng Chang,[a,*,z] Ying-Chen Chen,[a,*] Davood Shahrjerdi,[b] and Sanjay K. Banerjee[a,]**

[a]*Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, USA*
[b]*Department of Electrical and Computer Engineering, New York University, Brooklyn, New York 11201, USA*

In this work, we present silicon process compatible, stable and reliable (>10^8 cycles), high non-linearity ratio at a half-read voltage (>5×10^5), high speed (<60 ns), and low operating voltage (<3V) back-to-back Schottky diodes. Materials choice of electrode, the thickness of semiconductor layer and doping level are investigated by numerical simulation, experiments and current-voltage equations to give a general design consideration when back-to-back Schottky diodes are used as selector device for Resistive Random Access Memory (RRAM) arrays.
© The Author(s) 2017. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution Non-Commercial No Derivatives 4.0 License (CC BY-NC-ND, http://creativecommons.org/licenses/by-nc-nd/4.0/), which permits non-commercial reuse, distribution, and reproduction in any medium, provided the original work is not changed in any way and is properly cited. For permission for commercial reuse, please email: oa@electrochem.org. [DOI: 10.1149/2.0041709jss]
All rights reserved.

Manuscript submitted April 27, 2017; revised manuscript received July 31, 2017. Published August 10, 2017.

Resistive Random Access Memory (RRAM) is an emerging technology for future non-volatile memories (NVMs) because of fast write and read speed, low operating voltage, excellent scalability, and very high density ($4F^2$) if using crossbar array architecture with the potential for three-dimensional integration. RRAM can be the essential building block for neuromorphic computing and in-memory process.[1–9] However, the RRAM crossbar arrays usually suffer from leakage current due to undesired sneak paths when selecting RRAM cells. As array size increases, more sneak paths can form in arrays thus it deteriorates read margin required to distinguish high and low resistance states. This needs to be addressed before moving on to any application as well as to large-scale RRAM arrays.[10,11] Non-linear (NL) devices which can provide very low current series through unselected cells while pass enough current to selected cells are highly desirable for realizing large scale RRAM arrays. This structure is usually called as one-selector-one-resistor (1S1R).[12–17] Compared to another structure, one-transistor-one-resistor (1T1R),[18] the benefit of 1S1R over 1T1R is that there is no area overhead for universal leakage-current-limiting devices, and making RRAM capable of building memory arrays with higher density than flash memory. Besides, the NL device must be Back-End-Of-Line (BEOL) compatible because most RRAM processes are currently integrated into BEOL. In this paper, we present highly NL, fast, robust, low operating voltage, sufficient current density, good scalability, and simple fabrication processes with symmetric back-to-back Schottky diodes by metal-semiconductor-metal (MSM) structure. We also discuss impacts of material choices and device geometry on the performance of MSM diode by numerical simulation, Schottky diode current characteristics, and experimental results.

Simulation and Experiments

We performed simulations of Sentaurus to evaluate the feasibility of MSM diode as selector device for future RRAM crossbar arrays. It is interested in investigating the correlation between performance metrics of selector device and physical properties of MSM diode. In the simulation setup, we chose metal work function to match experimental values of Schottky barrier height values reported in the literature which means we take Fermi-level pinning into account. We assume the dominant current transport mechanism in this ultra-thin MSM diode to be thermionic emission, recombination, and tunneling. The doping concentration is assumed to be n-type doped (10^{13} cm^{-3}). DC characteristics in Fig. 1a with different thickness for Schottky barrier height of 0.66 eV, which is close to experimental values of titanium of silicon barrier.[19,20] The results show that a thickness dependence of current density and NL ratio. The definition of NL ratio in this paper follows half-read scheme which is widely used in many memory systems. The NL ratio is defined as the current density ratio of 1 MA/cm^2 and the current at half of voltage where current density reaches 1 MA/cm^2. As the thickness increases, the NL ratio decreases (Fig. 1a). This is probably because the voltage region where current grows exponentially is shifted by higher resistance in the diode, and higher series resistance in the thicker film also affects effective voltage drop in diode at the higher current region. This makes I-V characteristics of thicker diodes deviate from the ideal exponential curve at a lower current level as compared to thinner diodes, thus NL ratio in the thicker film is lower. The relation between Schottky barrier height and current density in Fig. 1b agrees well with simple Schottky diode model. In our simulation, we found out the high doping concentration adversely affects NL ratio. This is intuitive since CMOS technology has been using highly doped source and drain to achieve ohmic contact, which contradicts with our purpose to reach high NL ratio. Note that the effect of Schottky barrier height in current characteristics of MSM diode is similar to a simple Schottky diode: a higher Schottky barrier height results in lower current density near zero bias (discuss later). One important design consideration of selector device is to have both high NL ratio at low voltage region and high current density at high voltage region. Hence, based on the above simulation results, the desired MSM diode should have a thin thickness of semiconductor layer (less than 14 nm), low doping concentration and appropriate Schottky barrier height to give decent current density while keeping good NL ratio.

After optimizing the design by numerical simulation, devices were fabricated on an n-type Si (111) substrate with 300 nm plasma-enhanced chemical vapor deposition (PECVD) grown silicon dioxide on the top as an isolation layer. 80 nm bottom electrode (BE) was formed by electron beam evaporation at 273 K. 10 nm to 20 nm semiconductor layer was deposited on the top of BE by PECVD at 250 °C without ex-situ annealing.The growth condition and parameters are referred to Moravej et al.,[21] to aim to grow nanoscale hydrogenated amorphous silicon thin film. Then 80 nm top electrode (TE) was formed by electron beam evaporation of titanium at 273 K. Devices were patterned as crossbar with variant device perimeters from 300 nm to 10 μm by electron beam lithography. Electric measurements were taken by Agilent Semiconductor Parameter Analyzer B1500 and Lakeshore CRX-VF Probe Station. Pulse measurement was carried out by Agilent B1525 Pulse Generator Unit. Devices were measured by

*Electrochemical Society Student Member.
**Electrochemical Society Member.
[z]E-mail: yfchang@utexas.edu

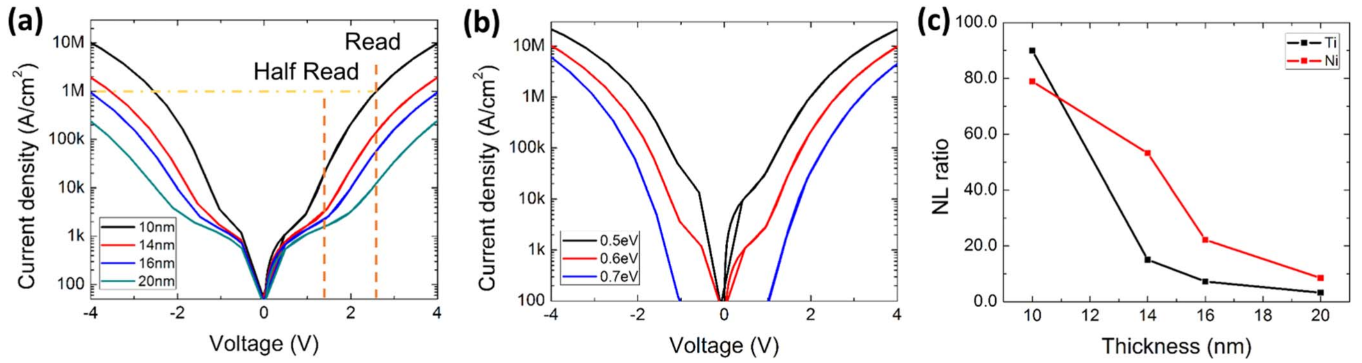

Figure 1. (a) DC I-V characteristics from two-dimensional numerical simulation by Sentaurus from Synopsys Inc. Two orange dash lines represent voltage values calculated for NL ratio. The choice of 1 MA/cm^2 is based on matching the current density of RRAM devices. (b) I-V characteristics of Schottky barrier height dependence. Note that non-linear step size of simulation caused I-V curves to show having a small hysteresis at low bias during positive polarity sweep, which is an artifact. (c) NL ratio extracted from Figs. 1a, 1b.

applying a voltage to the TE while the BE is grounded. The equivalent circuit diagram in Fig. 2a illustrates series resistance in MSM diode. The design of the crossbar is targeted to minimize impacts on parasitic components when doing pulse measurements. It can be seen in Fig. 2b metal lines are tapered to reduce parasitic capacitance. The overlap area of BE and TE defines the area of MSM diode.

Results and Discussion

Fig. 3a compares experimental DC I-V characteristics of Ti−aSi−Ti for different thickness of silicon layer. The effect of series resistance in 20 nm amorphous Si MSM diode can be observed in the region highlighted by dashed circle. Ti−aSi−Ti has higher current density than Ni−aSi−Ni at the same thickness of amorphous silicon in Fig. 3b, which implies amorphous silicon is unintentionally doped with n-type impurities. For n-type silicon, nickel tends to pin closer to the valence band of silicon while titanium is pinned at midgap. Thus we observe lower current density in Ni−aSi−Ni. NL ratio in Fig. 3c agrees well with Fig. 1c, which also indicates series resistance plays an important role when designing high current density selector. The inset of Fig. 3c shows linear scale plot of current density. It is obvious that there is asymmetry of current density between each polarity for titanium and nickel MSM diodes. Amorphous silicon and electrodes weren't deposited in the same instrument or same vacuum environment. So this causes inevitable interface difference between two Schottky diodes. To extract Schottky diode parameters from I-V characteristics of MSM diode, we need to start with simple Schottky diode current characteristics and combine with some assumptions to derive an insightful current equation for MSM diode device. Later we will point out when ideality factor larger than 1, MSM diode also demonstrates asymmetric I-V curve. Overall, experimental results are in good agreement with simulation prediction except for lower current density, probably because in simulation some materials-related parameters such as effective mass, recombination coefficients, and the bandgap is not a very accurately known for amorphous silicon.

To understand current-voltage characteristics of MSM diode and fundamental parameters such as Schottky barrier height and ideality factor, we have performed the fitting procedure on experimental I-V curves. The band diagram in Fig. 2a indicates that MSM diode can be considered to be back-to-back Schottky diodes. The current-voltage equation of a simple Schottky diode is in the following form:

$$J = J_S \exp\left(\frac{qV}{\eta kT}\right) \quad [1]$$

J_s is reverse saturation current of Schottky diode:

$$J_s = A * T^2 \exp\left(\frac{q\phi_b^0}{kT}\right) \quad [2]$$

where A is Richardson constant, T is temperature and k is Boltzmann constant. The voltage drops in two Schottky diodes are V_1 and V_2 the voltage across MSM diode is $V_{MSM} = V_1 + V_2$. We can also write $J_1 = -J_2$ from current continuity. Based on these two conditions we can write the current-voltage equation as in Nouchi and Nagano et al.:[22,23]

$$J_{MSM} = \frac{2J_{S1}J_{S2}\sinh\left(\frac{qV_{MSM}}{2\eta kT}\right)}{J_{S1}\exp\left(\frac{qV_{MSM}}{2\eta kT}\right) + J_{S2}\exp\left(\frac{-qV_{MSM}}{2\eta kT}\right)} \quad [3]$$

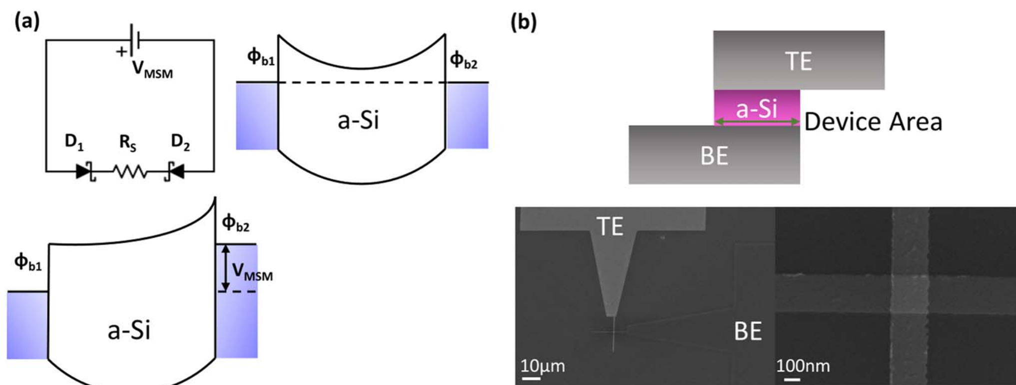

Figure 2. (a) shows band diagrams at equilibrium and forward bias on D1. The equivalent circuit diagram was shown at forwarding bias on D1. Series resistance is labeled as R_S.ϕ_{b1} and ϕ_{b2} represents Schottky barrier height at D1 and D2. Fig. 2b shows cartoon illustration of cross-sectional view of the device. The green arrow indicates the effective area of the device.

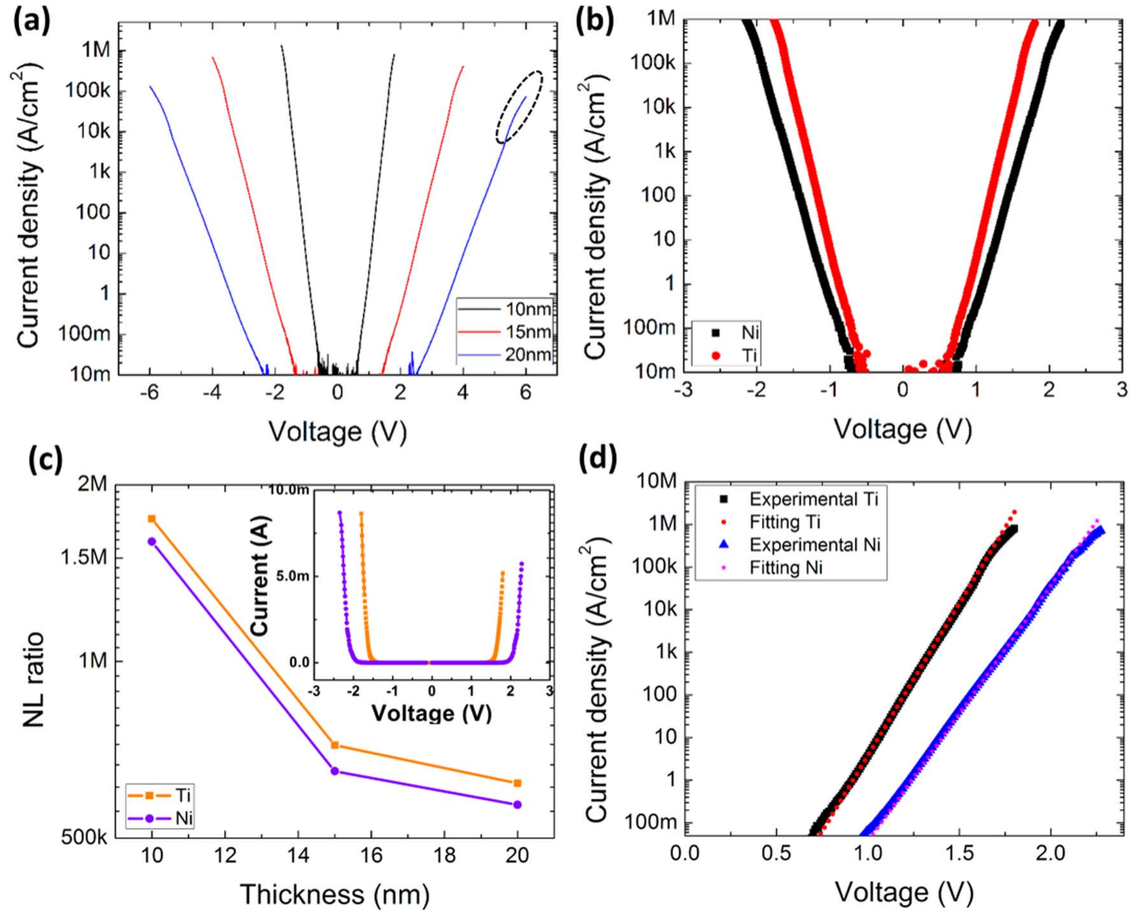

Figure 3. (a) shows a semilog plot of I-V characteristics of different thickness Ti−aSi−Ti diodes. The dashed circle is where series resistance effect becomes prominent. (b) shows I-V characteristics of Ti−aSi−Ti and Ni−aSi−Ni with 10 nm amorphous silicon. (c) compares NL ratio between Ti−aSi−Ti and Ni−aSi−Ni at different thickness. The inset of (c) is linear scale I-V characteristics of (b). (d) shows I-V curve fitting by using Eq. 7 fits well at intermediate bias where series resistance effect was low and thermionic emission is dominant.

The equation above can be further simplified if Schottky barrier height of diode 1 and diode 2 are symmetric:

$$J_{MSM} = J_S \tanh\left(\frac{qV_{MSM}}{2\eta kT}\right) \quad [4]$$

However, the current obtained from 4 reaches saturation at very low bias; this is contradicting to reported experimental results[24,25] and our experimental data. Note that 4 doesn't consider image-force lowering. Image-force lowering is based on image charges in metal layer induced by charges in semiconductor layer near the metal-semiconductor interface. Image charges establish an electric field along the metal-semiconductor interface and Schottky barrier height becomes voltage dependent:

$$\phi_{b1}(V_1) = \phi_{b1}^0 + qV_1\left(1 - \frac{1}{\eta}\right) \quad [5]$$

$$\phi_{b2}(V_2) = \phi_{b2}^0 + qV_2\left(1 - \frac{1}{\eta}\right) \quad [6]$$

where ϕ_b^0 is Schottky barrier height under zero bias and η is ideality factor. Assuming voltage drop in MSM diode is mostly on diode 2 since diode 1 is forward bias in Fig. 2a, we have $V_{MSM} \approx V_2$. We also assume 5 equals to 6 because of symmetric MSM structure, then we can rewrite 1:

$$J = J_S \sinh\left(\frac{qV_{MSM}}{2kT}\right)\exp\left(\frac{qV_{MSM}}{2kT}\right)\exp\left(\frac{-qV_{MSM}}{\eta kT}\right) \quad [7]$$

With Eq. 7 we can evaluate Schottky barrier height and ideality factor in MSM diodes and discuss the impacts on performance matrices of selector device. Fig. 3d shows fitting by 7 on 10 nm Ti−aSi−Ti and Ni−aSi−Ni MSM diode. The Schottky barrier height between titanium and amorphous silicon extracted by curve fitting with Eq. 7 is ≈0.79 eV, and the Schottky barrier height between nickel and amorphous silicon is about 0.86 eV. Note that the bandgap of hydrogenated amorphous silicon is around 1.6–1.8 eV. Titanium is usually pinned at midgap at silicon interface and nickel is usually pinned closer to the valence band of silicon, so the barrier height values extracted from Fig. 3d is what we expect. The ideality factor extracted from Fig. 3d are 1.18 and 1.36 for titanium and nickel respectively. Eq. 7 implies that non-ideal ideality factor can be attributed to unequal current density in MSM diode. The magnitude of the current density difference between each polarity is sensitive to ideality factor. As mentioned in the previous section, two Schottky diodes might have slightly different silicon interfaces. This might cause slightly different Schottky barrier height and thus contribute to asymmetric I-V characteristics. Although there is asymmetric current density for the same voltage when applying different polarity, the ratio of current density asymmetry is less than one order, as seen in Fig. 3c. The voltage difference to reach 1 MA/cm^2 is only 0.1 V for different voltage polarity for both Ti−aSi−Ti and Ni−aSi−Ni MSM diode. This will not impact the operation of selector device, but the effect of non-ideal MSM diode and interface properties should be taken into account when applying the selector device in RRAM arrays.

We performed transient analysis to test the speed of Ti−aSi−Ti device. We did impedance matching for the source to ensure the actual

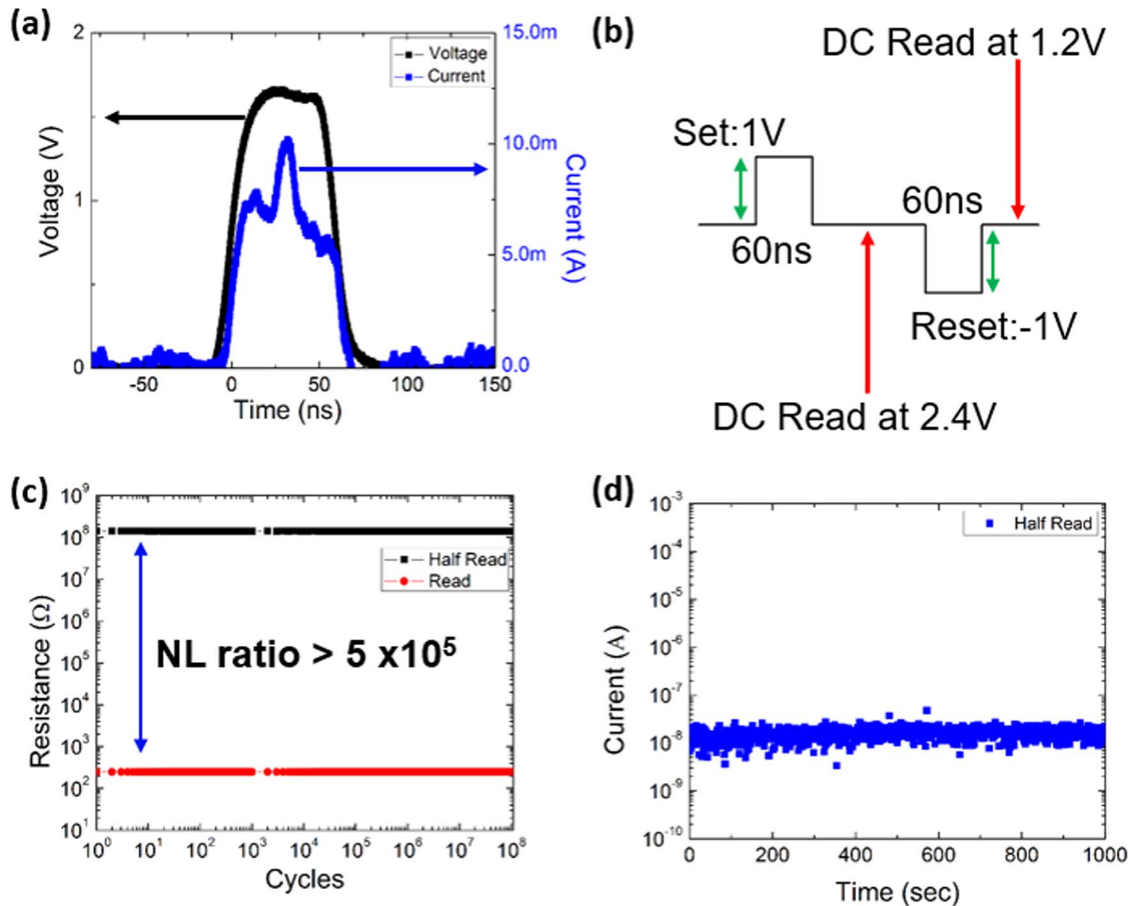

Figure 4. (a) shows the transient current response of DUT. black curve and arrow is input pulse generated by the source and blue curve and arrow are the current response of MSM diode. The device dimension is 300 nm × 300 nm crossbar. (b) Test scheme of cycle test. (c) shows cycle test of 10^8 cycles. (d) shows DC stress test at 0.9 V for 1000 seconds.

voltage drop in the device under test (DUT) was correct, and further normalized the current scale measured at oscilloscope (because input channel impedance was 50 ohm but the impedance through DUT was a few thousand ohm). It can be seen that in Fig. 4a MSM diode can response to 60 ns pulse without any notable delay or distortion of the signal. The current overshoot was only 25% higher than the mean current level during pulses. The result of the transient analysis is reasonable because the dominant current transport in MSM diode is thermionic emission. This makes MSM diode favorable over pn junction diode which is based on minority carrier injection. MSM diode also shows excellent reliability as potential selector device. Fig. 4b illustrates cycle test scheme of MSM diode. This is very similar to the test scheme of RRAM device since selector devices need to be integrated with RRAM cells. After each set or reset pulse, DC read at reading voltage or half read voltage was performed to record the value of resistance. Fig. 4c shows MSM diodes survived after 10^8 cycles without any notable degradation. Besides, MSM diodes demonstrated very good DC stress test, as seen in Fig. 4d at a half-read voltage over 10^3 seconds. These test results validate that our MSM diode is very robust and a suitable candidate for selector device.

Conclusions

In summary, a fast, reliable, high NL ratio, a low operating voltage with large current density MSM diode based selector device is presented in this paper. The current-voltage characteristics of symmetric MSM diode are also derived from extracting Schottky barrier height between metal and amorphous silicon and ideality factor. The current density asymmetry at a given voltage between each polarity is due to non-ideal MSM diode and different interface properties at each diode. The performance of MSM diodes could be improved if we use a narrower bandgap semiconductor or choose lower Schottky barrier height metal, but one needs to consider the fabrication feasibility and reliability of selector device. Here, we present an idea of designing MSM diode to meet requirements for selector device.

Acknowledgment

This work was supported by National Science Foundation (NSF), National Nanotechnologies Coordinated Infrastructure (NNCI), and Nanomanufacturing Systems for Mobile Computing and Mobile Energy Technologies (NASCENT).

References

1. D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, *Nature*, **453**, 80 (2008).
2. J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, *Nat. Nanotechnol.*, **3**, 429 (2008).
3. Y.-F. Chang, B. Fowler, Y.-C. Chen, F. Zhou, C.-H. Pan, T.-C. Chang, and J. C. Lee, *Sci. Rep.*, **6**, 21268 (2016).
4. D. Kuzum, S. Yu, and H.-S. P. Wong, *Nanotechnology*, **24**, 382001 (2013).
5. G. Indiveri, B. Linares-Barranco, R. Legenstein, G. Deligeorgis, and T. Prodromakis, *Nanotechnology*, **24**, 384010 (2013).
6. Y. F. Chang, F. Zhou, B. W. Fowler, Y. C. Chen, C. C. Hsieh, L. Guckert, E. E. Swartzlander, and J. C. Lee, *IEEE Transactions on Electron Devices*, **64**, 2977 (2017).

7. C. C. Hsieh, A. Roy, Y. F. Chang, D. Shahrjerdi, and S. K. Banerjee, *Applied Physics Letters*, **109**, 223501 (2016).
8. K. C. Chang, T. C. Chang, T. M. Tsai, R. Zhang, Y. C. Hung, Y. E. Syu, Y. F. Chang, M. C. Chen, T. J. Chu, H. L. Chen, C. H. Pan, C. C. Shih, J. C. Zheng, and S. M. Sze, *Nanoscale Research Letters*, **10**, 120 (2015).
9. C.-C. Hsieh, A. Roy, A. Rai, Y.-F. Chang, and S. K. Banerjee, *Appl. Phys. Lett.*, **106**, 173108 (2015).
10. C. Y. Lin, P. H. Chen, T. C. Chang, K. C. Chang, S. Zhang, T. M. Tsai, C. H. Pan, M. C. Chen, Y. T. Su, Y. T. Tseng, Y. F. Chang, Y. C. Chen, H. Huang, and S. M. Sze, *Nanoscale*, **9**, 8586 (2017).
11. S. Kim, Y. F. Chang, M. H. Kim, S. Bang, T. H. Kim, Y. C. Chen, J. H. Lee, and B. G. Park, *Phys. Chem. Chem. Phys.*, **19**, 18988 (2017).
12. Y. Deng, P. Huang, B. Chen, X. Yang, B. Gao, J. Wang, L. Zeng, G. Du, J. Kang, and X. Liu, *IEEE Trans. Electron Devices*, **60**, 719 (2013).
13. J. Zhou, K.-H. Kim, and W. Lu, *Electron Devices, IEEE Trans*, **61**, 1369 (2014).
14. M. Q. Guo, Y. C. Chen, C. Y. Lin, Y. F. Chang, B. Fowler, Q. Q. Li, J. Lee, and Y. G. Zhao, *Applied Physics Letters*, **110**, 233504 (2017).
15. L. Ji, Y. F. Chang, B. Fowler, Y. C. Chen, T. M. Tsai, K. C. Chang, M. C. Chen, T. C. Chang, S. M. Sze, E. T. Yu, and J. C. Lee, *Nano letters*, **14**, 813 (2013).
16. C. Y. Lin, Y. C. Chen, M. Guo, C. H. Pan, F. Y. Jin, Y. T. Tseng, C. C. Hsieh, X. Wu, M. C. Chen, Y. F. Chang, F. Zhou, B. Fowler, K. C. Chang, T. M. Tsai, T. C. Chang, Y. Zhao, S. M. Sze, S. Banerjee, and J. C. Lee, 2017 *International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 1, (2017).
17. L. Zhang, A. Redolfi, C. Adelmann, S. Clima, I. P. Radu, Y. Y. Chen, D. J. Wouters, G. Groeseneken, M. Jurczak, and B. Govoreanu, *IEEE Electron Device Lett*, **35**, 199 (2014).
18. Y. Y. Chen, L. Goux, S. Clima, B. Govoreanu, R. Degraeve, G. S. Kar, A. Fantini, G. Groeseneken, D. J. Wouters, and M. Jurczak, *IEEE Transactions on Electron Devices*, **60**, 1114 (2013).
19. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, *ECS Transactions*, **33**, 3 (2010).
20. C. A. Dimitriadis, S. Logothetidis, and I. Alexandrou, *Appl. Phys. Lett.*, **502**, 502 (1995).
21. M. Moravej, S. E. Babayan, G. R. Nowling, X. Yang, and R. F. Hicks, *Plasma Sources Sci. Technol.*, **13**, 8 (2004).
22. R. Nouchi, *J. Appl. Phys.*, **116**, 184505 (2014).
23. T. Nagano, M. Tsutsui, R. Nouchi, N. Kawasaki, Y. Ohta, Y. Kubozono, N. Takahashi, and A. Fujiwara, *J. Phys. Chem. C*, **111**, 7211 (2007).
24. D. Bozyigit, W. M. M. Lin, N. Yazdani, O. Yarema, and V. Wood, *Nat. Commun.*, **6**, 6180 (2015).
25. P. R. Berger, *IEEE Potentials*, **15**, 25 (1996).