# Kerf-Less Removal of Si, Ge, and III–V Layers by Controlled Spalling to Enable Low-Cost PV Technologies

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***Abstract*—Kerf-less removal of surface layers of photovoltaic materials including silicon, germanium, and III–Vs is demonstrated by controlled spalling technology. The method is extremely simple, versatile, and applicable to a wide range of substrates. Controlled spalling technology requires a stressor layer, such as Ni, to be deposited on the surface of a brittle material, and the controlled removal of a continuous surface layer could be performed at a predetermined depth by manipulating the thickness and stress of the Ni layer. Because the entire process is at room temperature, this technique can be applied to kerf-free ingot dicing, removal of preformed p-n junctions or epitaxial layers, or even completed devices. We successfully demonstrate kerf-free ingot dicing, as well as the removal of III–V single-junction epitaxial layers from a Ge substrate. Solar cells formed on the spalled and transferred single-junction layers showed similar characteristics to nonspalled (bulk) cells, indicating that the quality of the epitaxial layers is not compromised as a result of spalling.**

***Index Terms*—Flexible photovoltaic (PV), kerf-free, layer transfer, substrate reuse.**

## I. Introduction

THE field of photovoltaics (PV) is primarily concerned with maximizing the conversion efficiency of photon energy into electrical energy under the constraint of minimum cost. Therefore, the main driving forces for innovation in PV involve increasing the efficiency of the solar cell device (or system), decreasing materials costs, or decreasing processing costs. The current cost reduction roadmap aims at achieving \$1/W for installed systems by 2017. Additionally, the industry is expanding its application space by integrating flexible solar cells into architectural materials, portable devices, or other nonstandard solar panel applications. The efficiency of state-of-the-art solar cells for such applications is far from optimum.

In this paper, we describe a novel and elegant method which allows kerf-free layer removal of single-crystal Si, Ge, and III–Vs with or without additional epitaxial structures such as those used for high-efficiency solar cells. The method can be extended to any brittle material and applied to commercially available crystalline wafers or ingots of any size or shape without requiring ion implantation or specialized epitaxy layers [1]. The thickness of the removed layer can be controlled from hundreds of angstroms to tens of micrometers by this technique. We have successfully demonstrated kerf-free layer removal from up to 300-mm-diameter Si wafers. We believe that the layer removal method described here not only has the potential to reduce significantly the cost of conventional PV technologies but will permit fabrication of novel, high-efficiency, flexible PV materials and devices as well. The method exploits a unique fracture mode in brittle materials referred to as substrate spalling; the fracture is controlled by applying constraints on the crack propagation.

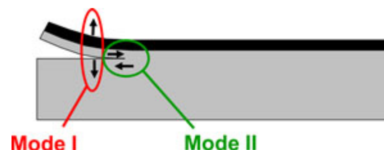


Fig. 1. Spalling mode fracture of a substrate due to the presence of a tensile layer. In addition to the opening mode stress (mode I) acting on the crack tip, a shear field (mode II) is created as the tensile surface layer contracts.

## II. Spalling Mode Fracture

The most familiar form of fracture in a brittle substrate is cracking through the entire thickness leading to wafer breakage. However, under the specific condition of a tensile strained film on the surface of a brittle substrate, fracture can propagate downward to a certain depth below the film/substrate interface and, then, travel parallel to the interface. This fracture propagation parallel with the film/substrate interface results in the removal of the upper surface of the brittle substrate, provided the film adhesion is sufficiently strong. Fig. 1 shows a drawing of the basic fracture mode referred to as substrate spalling. Although this phenomenon has been known for a long time, the fracture mechanics analysis of substrate spalling was not developed until the late 1980s [2]–[4]. The basic physical mechanism underlying spalling mode fracture lies in the fact that in the presence of a surface film under residual tension, the stress field at a crack tip (see Fig. 1) is composed of both mode I (pure opening stress) and mode II (shear stress) components. The nature of fracture in brittle solids is such that the crack path tends to follow a trajectory where the shear component is minimized [5]. If the

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surface stressor layer is compressive, the crack will be deflected upward and lead to film cracking, if it is tensile the crack tip is deflected downward into the substrate. Therefore, the equilibrium crack depth will be at a position below the film/substrate interface where the mode II stress is zero. The crack trajectory is stable within the substrate because the nonzero shear fields above and below the equilibrium crack depth are corrective. An excellent review of mixed mode fracture is given by Hutchinson and Suo [6].

Although spalling has historically been studied as a failure mode, recent work by Dross *et al*. [7] demonstrated successful removal of a 40-$\mu$m-thick Si layer from a 300-$\mu$m-thick starting substrate by surface spalling. In that work, thick screen-printed metal (Al and Ag) pastes were applied to the surface of the substrate and annealed at 900 °C. Upon cooling, the coefficient of thermal expansion (CTE) mismatch between the metal layers and the Si substrate was the source of tensile stress and ultimately led to spalling of the Si surface.

## III. Controlled Spalling Technology

The main drawbacks to the aforementioned approach are the high-temperature steps, which are required to create the necessary stress, and the occurrence of spontaneous fracture upon cooling. Both of these conditions create severe restrictions on the usefulness of layer transfer by substrate spalling. The high temperature prohibits layer spalling of prefabricated devices, and the spontaneous fracture limits the ability to integrate the transferred layers with other substrates in a controllable manner. To make layer transfer by spalling as general and useful as possible, we engineered tensile stress into the as-deposited metal stressor layer, enabling the entire spalling process to be performed at near room temperature. In addition, by controlling the stress level, the appropriate film thickness can be chosen to simultaneously control the fracture depth as well as inhibit spontaneous fracture of the metal/substrate combination. We can, therefore, apply a separate flexible adhesion layer to the metal surface and mechanically assist spalling of the metal/substrate layers in a controllable manner. By creating a well-defined fracture initiation region and propagating a single fracture front across the surface in a controlled manner, we have demonstrated routine, large-area, crack-free layer transfer from a variety of substrates. Fig. 2 shows a schematic illustration of the controlled spalling process which enables low-temperature layer transfer and a simplified film-handling scheme. Although many different materials can be used as the stressor, Ni was used in this study because it is inexpensively deposited, and the stress can be well controlled.

The first step to enable controlled spalling is to deposit a stressor layer with a well-controlled thickness and stress at or near room temperature. This can be accomplished using a variety of methods, but physical vapor deposition by sputtering and electroplating are the most common. It is well known that sputter-deposited hard metal films are usually in a stressed state [8]. The magnitude and sign (compressive or tensile) depend on the atomic mass of the film material as well as processing conditions. We have been able to control tensile stress in Ni layers

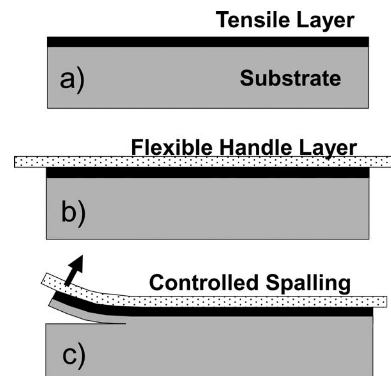


Fig. 2. Controlled spalling process. (a) Stress and thickness conditions are chosen that render the system metastable (or stable) against spontaneous fracture. (b) Handle layer is then applied and used to propagate (c) surface fracture controllably.

over a range of approximately 200 to 800 MPa using dc magnetron sputtering with approximately 5% variation in stress over the target life. Likewise, electroplated Ni films can be deposited using a wide range of chemistries and conditions to produce residual stress ranging from stress free to greater than 1-GPa tensile stress [9]. Interestingly, most electroplating research is aimed at either reducing stress or improving luster, usually at the expense of film toughness. Controlled spalling provides a unique application of electroplating whereby well-controlled (and high) residual stress and film toughness are of primary importance. Controlled spalling can be performed directly after layer deposition with no need for subsequent heat treatment or preparation.

The critical film stress and thickness combination required to fracture a given substrate at a desired depth is computed following the procedure outlined in [3], which has been coded into a stand-alone software application for convenience. Deposition of a film with the proper critical conditions does not, however, generally lead to substrate spalling. The reason for this is because the conditions are computed assuming a pre-existing crack, whereas the physical conditions that lead to spontaneous (self-initiated) spalling are different. Controlled spalling exploits this metastability of fracture. Therefore, the film thickness and stress are deposited in such a manner that renders the substrate stable against spontaneous fracture but permits spalling after the handle layer (usually a thin tape) is applied and a crack is introduced at one edge of the wafer.

One convenient method for introducing a crack is to provide an abrupt discontinuity at the edge of the stressor layer. When the additional force from the handle layer is applied to this stress discontinuity, a crack is introduced into the surface of the film/substrate boundary and initiates fracture. Fig. 3 shows a scanning electron microscopic (SEM) cross-section image of fracture initiation at the edge of a 4-in Ge substrate with III–V heteroepitaxial surface layers. A sputtered Ni layer (6 $\mu$m) was used in this example which led to a spalling depth of approximately 17 $\mu$m. Over a 4-in wafer using SEM imaging at various locations, the thickness variation of the spalled layer is typically $\sim$1 $\mu$m. We believe this can be further reduced by optimizing the mechanical constraints during spalling. Alternatively,

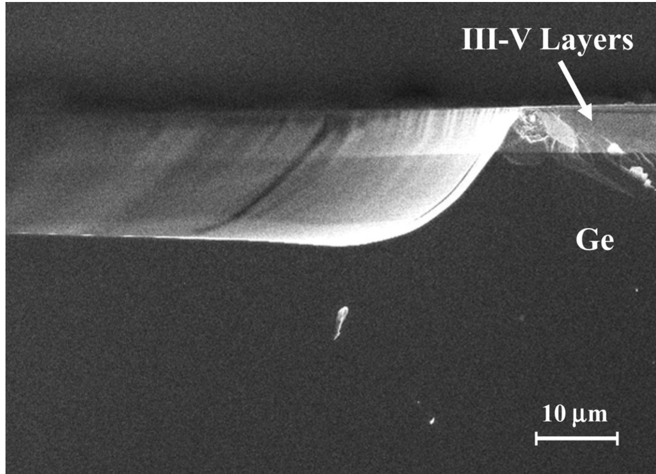


Fig. 3. Cross-section SEM image of the crack initiation region in a 4-in Ge substrate with epitaxial III–V surface layers. The fracture depth is approximately 17 $\mu$m.

precise depth control can be achieved by using epitaxial layers with a lower fracture toughness ($K_{1C}$) than the surrounding material. We have demonstrated controlled spalling with depth control that is limited only by the epitaxial layer thickness variation, which is typically in the range of a few nanometers.

## IV. Defect Analysis of Spalled Layers

The handle layer plays an interesting role in the controlled spalling process; it promotes pure spalling mode fracture while suppressing parasitic modes of fracture (such as channel mode fracture). It does this by preventing the formation of multiple fracture fronts, which lead to high roughness, surface artifacts, and even film cracking. Because the spalled film/substrate combination forms a stressed bilayer, the semiconductor is capable of cracking if it is mishandled. Therefore, the handle layer also provides a convenient way to manipulate the thin semiconductor layer without introducing cracks.

Due to the well-developed techniques for studying defects in Si, the impact of spalling on crystal quality can be readily observed by using a combination of Secco defect etching [10] in conjunction with differential interference contrast (DIC) optical microscopy on spalled Si layers. Fig. 4 shows a composite DIC microscope image after Secco etching the fractured surface of a spalled Si ⟨1 0 0⟩ layer. In the left image [see Fig. 4(a)], two intersecting cracks can be seen that formed near the edge of the film due to mishandling. In Fig. 4(b), a typical DIC image after defect etching shows the absence of any crystalline defects (dislocations or cracks). The lines in the image are thickness variation as the crack front oscillates about the equilibrium fracture depth and the amplitude is typically less than 100 nm, as measured by profilometry.

The absence of dislocations is anticipated as they are not able to form in Si at room temperature except under unique loading conditions [11]. The presence of an atomically sharp crack tip at room temperature assures that the response of the Si will be dominated by pure brittle fracture during spalling.

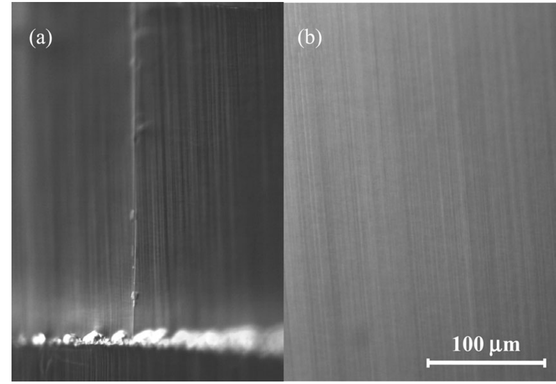


Fig. 4. Optical DIC micrographs of spalled Si ⟨1 0 0⟩ surfaces after defect etching. (a) Two intersecting cracks can be seen and resulted from film mishandling. (b) Typical region of a spalled surface is shown, indicating the absence of etch pits or cracks. The faint parallel lines are due to the crack depth oscillation about equilibrium and are typically less than 100 nm.

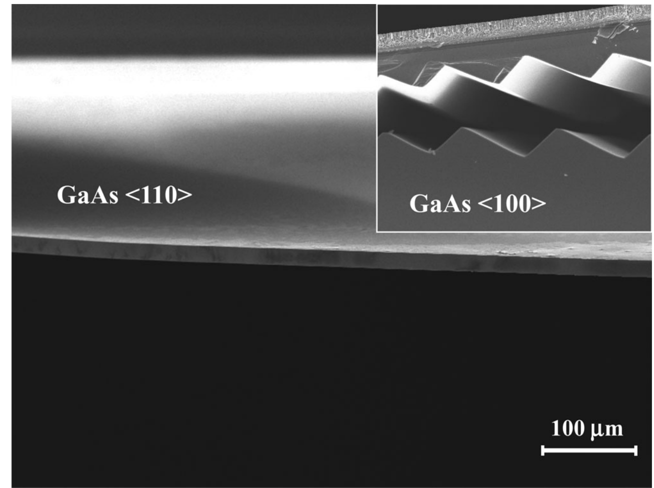


Fig. 5. Cross-section SEM image of a 15-$\mu$m-thick uniformly spalled GaAs ⟨1 1 0⟩ layer (Ni removed). The inset shows a spalled ⟨1 0 0⟩ GaAs layer (∼6-$\mu$m Ni intact), illustrating the unstable fracture in that system.

This also indicates another possible drawback to CTE-originated spalling; the brittle-to-ductile transition temperature (for Si) is around 450 °C, and dislocations are more likely to form at those temperatures.

## V. Kerf-Free Ingot Spalling

One of the most direct methods to improve the cost of PV materials is to minimize the waste associated with wafer sawing losses. Direct electroplating of stressed Ni onto ingots of Si, Ge, and GaAs was performed, and kerf-free removal of thin substrates was successfully demonstrated.

The effect of the crystal orientation on controlled spalling is small for the elemental semiconductors such as Si and Ge, and we have spalled all major orientations with similar results. The polar nature of the bonding in GaAs, however, makes spalling of the ⟨1 0 0⟩ GaAs crystals difficult. Fig. 5 shows a cross-section SEM image of a ⟨1 1 0⟩ GaAs layer which shows stable fracture parallel to the surface, compared with the unstable fracture in

Fig. 6. Demonstration of layer transfer of GaAs ⟨1 1 0⟩ directly from a 2-in ingot by controlled spalling using electroplated Ni.

Fig. 7. Five-micrometer thick GaAs single-junction epitaxial layer removed from a 4-in Ge substrate and bonded to a thin steel disk using conductive epoxy. The handling layer and the Ni have been removed. The reflection from the ceiling can be seen on the wafer surface.

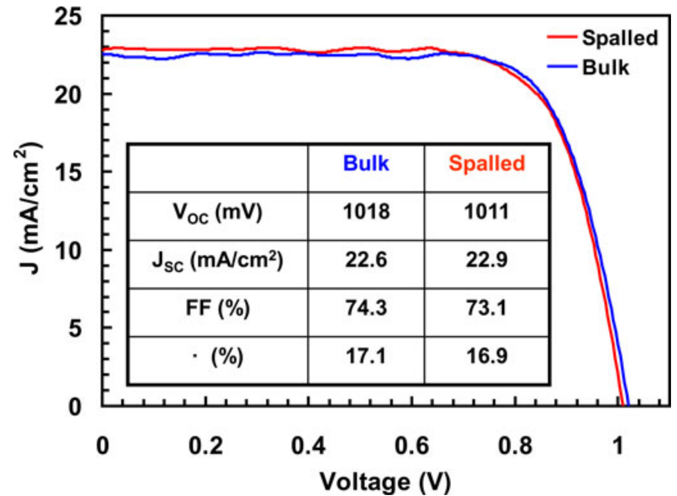


Fig. 8. 1 sun *J–V* characteristics of the fabricated bulk and thin-film PV cells.

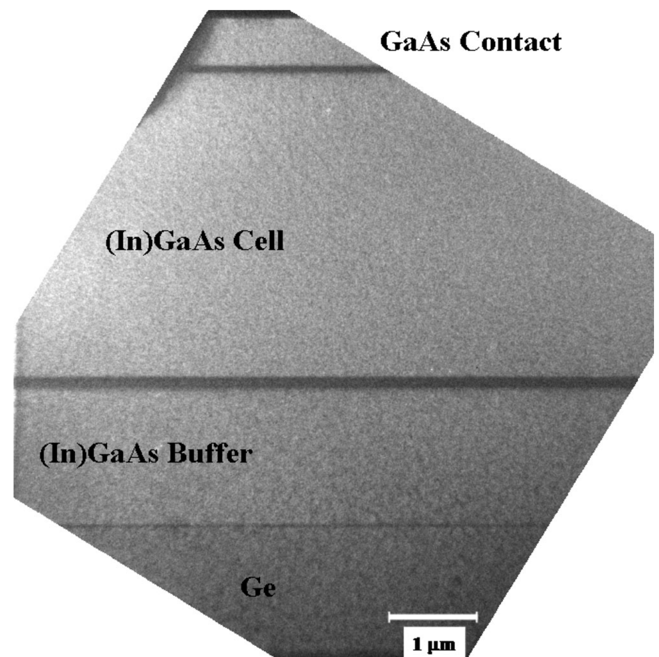


Fig. 9. Cross-section TEM image of the spalled single-junction III–V layers shown in Fig. 7 after bonding and cell fabrication. There were no defects observed in the TEM sample.

the ⟨1 0 0⟩ orientation (inset). Ni was used to spall both layers, but has been removed from the GaAs ⟨1 1 0⟩ surface.

Fig. 6 shows a 20-$\mu$m-thick ⟨1 1 0⟩ GaAs layer transferred from a 2-in ingot to a plastic handling layer using controlled spalling. The ingot was manually polished to remove saw damage leaving some polishing artifacts that can be seen near the center of the spalled layer. The smooth as-spalled ⟨1 1 0⟩ surface allowed the process to be repeated up to five times without the need for repolishing the ingot surface. The accumulation of fracture depth variations arising from nonconstant spalling velocity (start/stop defects) can be seen on the ingot surface after multiple transfers and can be minimized with automation. The extreme simplicity of the technique and the low cost and reusability of the plating solution makes kerf-free ingot slicing by controlled spalling a very promising technology.

## VI. Substrate Reuse and Flexible Photovoltaics

A significant fraction of the cost of high-efficiency solar cells is due to the expense of the starting substrate. The highest efficiency III–V-based solar cells have only limited terrestrial application due to this high expense. By using controlled spalling, we successfully removed III–V single-junction layers grown on thin 4-in Ge substrates by metal–organic chemical vapor deposition (MOCVD). The entirety of the surface was removed as a continuous sheet, and a thin Ti/Al bilayer (20 nm/100 nm) was evaporated onto the as-fractured Ge surface. The layer was, then, bonded to a thin stainless steel disk using conductive epoxy in order to process and test devices. After bonding, both the handling and Ni stressor layers were removed (see Fig. 7). Cells (1 cm$^2$) were fabricated on both bulk and thin-film (spalled) materials using a shadow mask (15% shadowing) process for the evaporation of the Pd/Ge/Au front contact grid, followed by the deposition of the ZnS/$MgF_2$ antireflective coating. The current density–voltage (*J–V*) characteristics of the single-junction cells were measured under a simulated 1.5AM solar spectrum at 1 sun intensity, as shown in Fig. 8. The conversion efficiency values of the spalled III–V single-junction PV cells were measured to be ~17%, which were similar to those formed on bulk substrates (see the inset in Fig. 8) indicating that the material quality is not affected by the spalling process. A cross-section

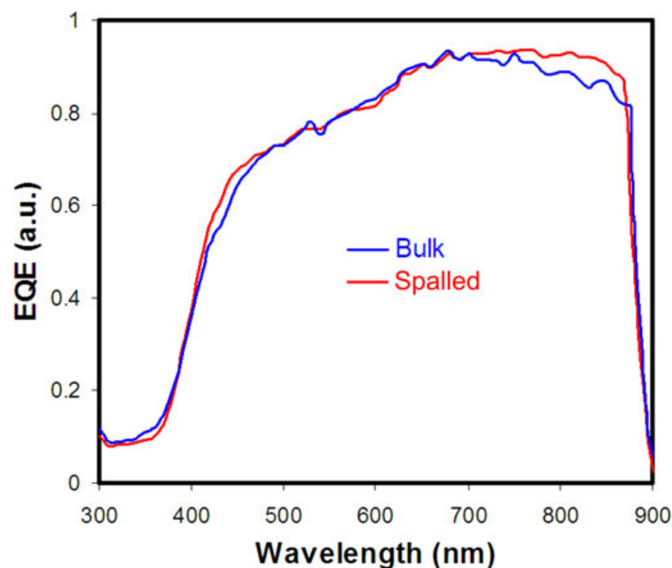


Fig. 10. Comparison of EQE from the spalled and bulk single-junction solar cells.

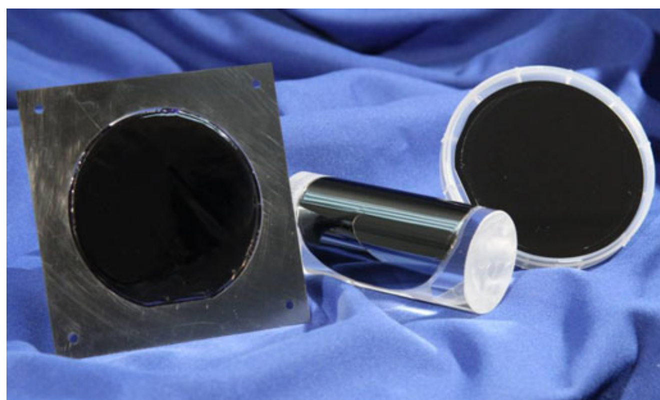

Fig. 11. (Left to right) Twenty-micrometer-thick Si on plastic mounted in a handling frame, 8-$\mu$m-thick III–V multijunction layers on tape and mounted on a cylinder, and the bulk Si substrate from which the 20-$\mu$m-thick layer was removed.

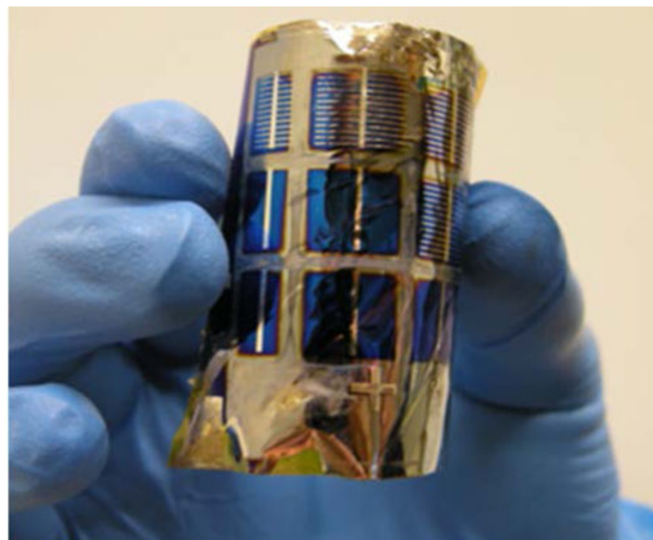

Fig. 12. Flexible solar cells fabricated on a 3-$\mu$m-thick single crystal Si formed by controlled spalling.

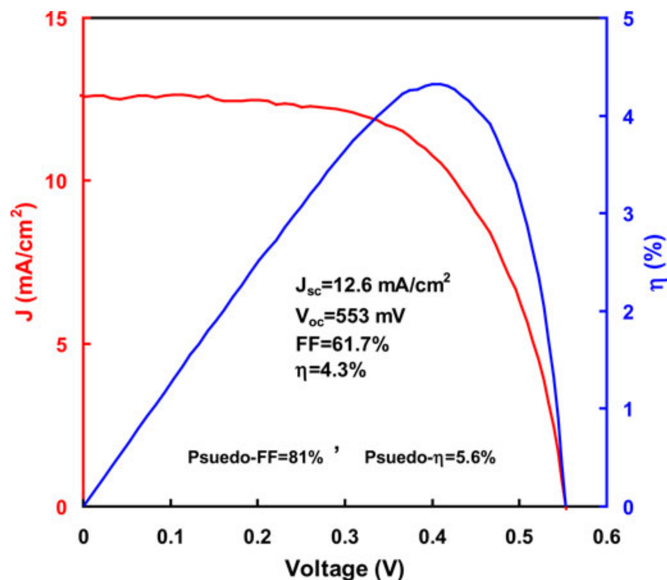


Fig. 13. One-sun *J–V* characteristics of the 1-cm$^2$ solar cells formed on the 3-$\mu$m-thick spalled Si layers shown in Fig. 12.

TEM image of the spalled and processed single-junction cell is shown in Fig. 9. No crystalline defects were found in the TEM sample volume. The modest efficiency of these single-junction cells was due to high absorption in the thick window layer and nonoptimized low-temperature Ohmic contacts. All devices fabricated were functional with a reasonable distribution in efficiency (highest-to-lowest $\sim$30% variation). Despite the variations in cell efficiency due to postprocessing, the external quantum efficiency (EQE) of all bulk and spalled devices was the same within measurement error suggesting that the intrinsic material parameters (minority carrier lifetime, surface recombination properties) are unchanged after spalling. A comparison of EQE data from a typical bulk and spalled cell is shown in Fig. 10. The advantages enabled by this layer transfer approach include the ability to change the cost structure of III–V PV materials by reusing the starting substrate, as well as enabling flexible high-efficiency products. Although layer transfer of III–V layers has been demonstrated using epitaxial liftoff [1], controlled spalling is much simpler, independent of area, and does not require the use of specialized etch layers.

For multiple reuse of the original substrate, it is desirable to start with a thicker substrate so that repolishing of the substrate after spalling can be accomplished. Alternatively, epitaxial layers can be used either as preferential fracture layers or etch-back layers to reclaim the original surface while minimizing substrate material loss.

In addition to the single-junction III–V structure, multijunction epitaxial layers have been successfully released from a 4-in Ge substrate. Fig. 11 shows examples of 20-$\mu$m-thick Si $\langle 1\,0\,0 \rangle$ on tape mounted to a stainless steel handling frame, flexible GaAs multijunction layers on tape, and bulk Si substrate after layer removal.

In another application of controlled spalling, flexible heterojunction solar cells (1 $cm^2$) were fabricated on a $\sim$3-$\mu$m single-crystal Si layer that was released from an Si wafer, which is shown in Fig. 12. In this example, the Ni stressor layer and the handling tape remained on the spalled layer to serve as the back electrical contact and support medium, respectively. The resulting *J–V* characteristics are shown in Fig. 13, and these are consistent with simulations assuming a 3-$\mu$m-thick Si layer with a rear surface recombination velocity of $\sim 10^4$ cm/s.

Although the spalled layers in our current experiments are initially in residual compression, by judicious choice of bonding temperatures and substrates, the final strained state of the spalled semiconductor layer can be engineered to be tensile, compressive, or zero. This may be an important consideration, especially for devices requiring thermal cycling.

## VII. Conclusion

Controlled spalling technology is introduced as an extremely simple, versatile, and low-cost method for removing surface layers of brittle substrates. By tailoring the thickness and stress in Ni layers deposited on a range of semiconductor materials, the controlled removal of a continuous surface layer could be performed at a predetermined depth in the substrate. Because the entire process is at room temperature, this technique can be applied to kerf-free ingot dicing, removal of preformed p-n junctions or epitaxial layers, or even completed devices. We successfully demonstrated kerf-free ingot dicing, as well as the removal of III–V single-junction epitaxial layers from a Ge substrate. Solar cells formed on the spalled and transferred single-junction layers showed similar characteristics to nonspalled (bulk) cells, indicating that the quality of the epitaxial layers is not compromised as a result of spalling.

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