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Mechanically flexible nanoscale silicon integrated circuits powered by photovoltaic energy harvesters

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ABSTRACT

In this work, we demonstrate mechanically flexible extremely thin silicon on insulator (ETSOI) ring oscillators with a stage delay of ~16 ps at a power supply voltage of 0.9 V. Extensive electrical analyses of the flexible ETSOI devices reveal the unchanged properties of the devices during the layer transfer process. Furthermore, we discuss the use of flexible silicon and gallium arsenide photovoltaic energy harvesters for powering flexible ETSOI ring oscillators under different illumination conditions. Our results illustrate innovative pathways for the implementation of optically powered flexible ETSOI technology in future flexible hybrid electronics.

1. Introduction

Flexile hybrid electronics is a new class of technology, wherein thin electronic components mounted on flexible substrates can conform to non-planar surfaces. This new class of electronics is enabled through innovative layer transfer processes that aim to (i) reduce the thickness of the conventional electronic devices and (ii) transfer the ensuing thin electronics onto a flexible substrate, while maintaining the original performance of the devices.

Internet-of-Things (IoT) is emerging as the next wave in Information Technology. The ability to cost-effectively manufacture complex system-on-chip (SoC) silicon integrated circuits that contain a staggering number of nanoscale transistors has enabled a slew of new portable devices that are integral building block of IoT. In addition to those devices, new flexible hybrid electronic systems are envisioned to become an integral part of IoT, due to their possible wide-ranging applications from health monitoring to consumer electronic gadgets [1–5]. Therefore, considering the existing silicon manufacturing infrastructures, the use of silicon technology is appealing to achieve high-performance flexible integrated sensors and circuits with a high level of miniaturization. The success of this new class of electronics, however, depends on the development of enabling disruptive technologies that yield high-speed low-power devices that are mechanically flexible. In this paper, we discuss flexible complementary metal-oxide semiconductor (CMOS) integrated circuits that are fabricated on extremely thin silicon on insulator (ETSOI) substrate as a viable candidate for future flexible hybrid electronic systems.

The ultra-thin body of the silicon channel in ETSOI devices allows aggressive scaling of the channel length into sub-20 nm range without incurring the detrimental short channel effects. In addition, excellent subthreshold characteristics, lack of random dopant fluctuations, and the ability to lower the threshold voltage by applying a wide range of forward body bias (FBB) in ETSOI transistors, allows significant reduction of power supply voltage (V_{DD}) not accessible to other CMOS technologies [6–8]. This enabling feature opens up an opportunity for developing new paradigms in design of ultra low-power integrated circuits using the ETSOI technology [9].

On the other hand, current technological challenges in downscaling of electrochemical batteries have limited the longevity and form factor of the batteries. Therefore, there is a strong demand for energy-autonomous integrated sensors and circuits utilizing energy harvesting schemes to replace or supplement the on-chip batteries [10–15]. There have been numerous reports of energy harvesting from various energy sources such as mechanical, optical and thermal energy as well as near- and far-field RF power. Notably, a survey of various energy harvesters indicates that high-efficiency photovoltaic solar cells produce the highest output power per unit area among the existing energy harvesters [16,17]. This attribute of photovoltaic energy harvesters therefore

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makes them attractive for applications where the size is a critical factor.

A number of factors play a key role in determining an appropriate strategy for the integration of photovoltaic energy harvesters in flexible hybrid electronics. Examples of those factors include cost, level of mechanical flexibility of the system, output voltage and output power of the energy harvester. One relatively straightforward approach is to monolithically integrate silicon photovoltaic devices by forming p–n junctions in the silicon substrate using compatible CMOS fabrication processes [10]. Considering the relatively large size of a photovoltaic device compared with that of a CMOS circuit, the cost considerations might prohibit the monolithic integration of p–n junction solar cells in the active silicon layer where the CMOS circuit is fabricated. Compared to bulk CMOS technologies, this approach could however be more favorable for an SOI technology, in which the p–n junction solar cells can be formed in the silicon handle substrate under the buried oxide (BOX) layer. This particular configuration will therefore relax the size requirements of the photovoltaic device since it no longer consumes the silicon active region. However, one practical design consideration is to account for an unintentional back bias of the CMOS devices above the BOX layer by the 'buried' photovoltaic device. In particular, this effect will be more pronounced in case of SOI technologies utilizing the ultra-thin BOX feature for FBB. Alternatively, one can devise a flexible hybrid electronic system, in which the flexible photovoltaic device is fabricated separately. In this approach, the flexible energy harvester will be connected to other flexible constituents of the flexible hybrid system, such as sensors and integrated circuits, later in the process when these components are being assembled on a main flexible substrate. This approach offers two main advantages over the monolithic integration method. These advantages namely are: (i) the heterogeneous integration of high-efficiency photovoltaic energy harvesters that are made of dissimilar materials such as compound semiconductors and (ii) the implementation of photovoltaic device architectures with adjustable output voltage by connecting the solar cell devices in series.

In this paper we first discuss the fabrication and electrical properties of flexible ETSOI devices and circuits. Then, we describe the performance of our flexible ETSOI circuits powered by flexible silicon and gallium arsenide (GaAs) photovoltaic energy harvesters.

2. Nanoscale flexible ETSOI circuits

A surface layer film under tension in bilayer or multilayer structures may cause the formation of delamination cracks at the edges of a sample [18]. The delamination cracks generally run along the interface between the film and the substrate. If the fracture toughness of the substrate is sufficiently low, those cracks will then dive into the substrate and propagate parallel to the interface. This unusual mode of substrate cracking – referred to as spalling fracture – prompted a substantial body of work mostly in 1980s, in order to understand this phenomenon [19–21]. Those studies primarily aimed at developing robust fail-safe criteria to prevent the occurrence of spalling fracture in bilayer systems.

In recent years, mechanical exfoliation by substrate cracking has emerged as a new promising approach for producing large-area thin semiconductor layers [22–25]. Early studies of spalling fracture indicate that this mode of substrate cracking is spontaneous, in which multiple fracture fronts propagate simultaneously, thereby leading to film and/or substrate damage where the crack fronts meet. In order for the mechanical exfoliation to be utilized as a viable layer transfer method it is necessary to eliminate those undesirable features. To circumvent these issues, Bedell et al. have employed surface layers with intrinsic tensile stress in conjunction with a flexible handle layer to achieve a single fracture front and thus enable controlled spalling [24,25]. Furthermore, Shahrjerdi et al. have demonstrated the feasibility of this technique for making various advanced flexible devices including CMOS integrated circuits and high-efficiency III–V tandem solar cells on plastic substrates by exfoliating prefabricated devices from rigid substrates [26,27]. In light of the prospects of the ETSOI technology for IoT applications, we first discuss the electrical properties of flexible ETSOI devices and circuits produced by the controlled spalling technique.

2.1. Fabrication of flexible ETSOI devices

In recent years, several pioneering integration schemes have paved the way for the manufacturing of advanced ETSOI devices [28,29]. In this work, the ETSOI devices are fabricated using an implant-free integration process that utilizes *in situ* doped epitaxy for making raised source/drain (S/D) regions and a silicon channel thickness of 6 nm. A single high-k/metal gate stack was used for both n-type and p-type field-effect transistors (FETs). After forming thin spacer, *in situ* boron doped silicon germanium (SiGe) and *in situ* phosphorus doped silicon carbon (Si:C) were epitaxially grown to form the raised S/D regions for p-FET and n-FET devices, respectively. The extension junctions were then formed by driving dopants from the doped raised S/D towards the channel using rapid thermal annealing. The ETSOI device integration process was completed by forming final spacer, silicide, contacts, and metallization. Note that the entire fabrication process for the CMOS integrated circuits was performed on rigid ETSOI substrates.

Subsequently, the controlled spalling technique was applied to the rigid substrates consisting of fully fabricated ETSOI transistors and circuits to separate the top ~15 μm of the substrate. Fig. 1 illustrates the layer transfer process for making flexible ETSOI integrated circuits using the controlled spalling method. The layer transfer process was performed entirely at room temperature. For the controlled spalling process, ~6 μm thick sputtered nickel (Ni) film with an intrinsic tensile stress of 450–500 MPa was used, which drives the spalling fracture inside the substrate. The stressor layer was capped by thin polyimide tape to enable mechanical guiding of a single spalling-mode fracture across the wafer in a controllable manner.

The maximum tolerable bending radius of a stiff material is inversely proportional to t^3, where t is the total thickness. In order to maximize the mechanical flexibility of the final circuit, it is therefore desirable to remove the excess silicon layer underneath the BOX. The residual silicon was selectively removed with respect to the oxide layer in tetramethylammonium hydroxide (TMAH) solution (Fig. 1b), in which the BOX layer served as the etch stop. The representative transmission electron micrograph (TEM) image in Fig. 2a shows an array of flexible nanoscale ETSOI transistor, sandwiched between the Ni stressor and the BOX layer, confirming that the structural integrity of the devices is maintained after spalling. Although in our experiments, the residual silicon was completely removed, it is possible to leave behind a thin layer of silicon under the BOX when the body biasing feature is utilized. Next, the spalled sample shown in Fig. 1b was transposed onto a plastic substrate followed by the removal of the polyimide tape and the Ni stressor, shown in Fig. 1c and d. The photograph in Fig. 2b shows a flexible ETSOI circuit after the completion of the second transfer process, revealing the surface of the chip.

2.2. Electrical characteristics of flexible ETSOI devices and circuits

Piezoresistive properties of semiconductor materials tend to make the electrical measurement of thin flexible devices challenging. In particular, nanoscale devices are more susceptible

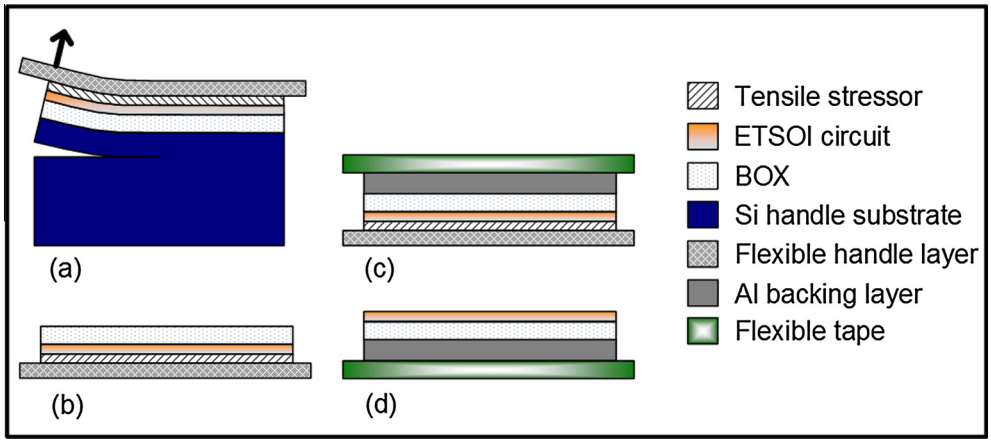

Fig. 1. Schematic illustration of the layer transfer process steps consisting of (a) controlled spalling, (b) removal of the excess silicon underneath the BOX using TMAH, (c) deposition of Al backing layer and subsequent transfer of the sample onto a plastic substrate, and (d) removal of Ni and polyimide tape.

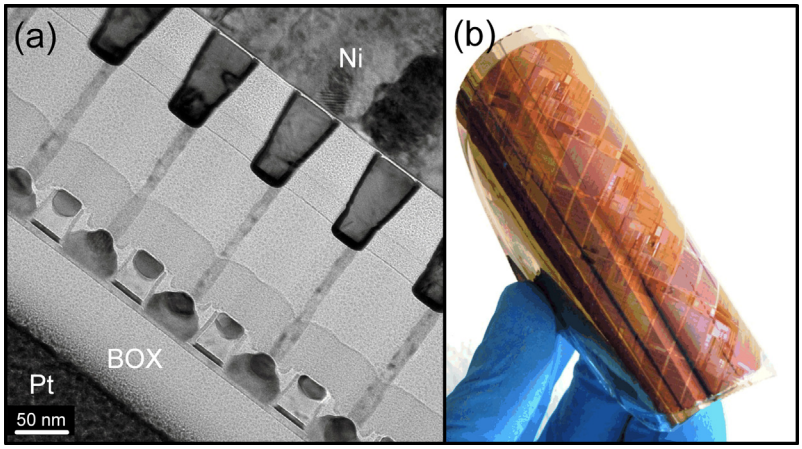

Fig. 2. (a) Representative TEM image of a flexible sample illustrating the structural integrity of the circuit after the spalling step, and (b) photograph of the final flexible circuit.

to external mechanical forces that might lead to spurious measurement results. Therefore, care must be taken when making electrical measurements on flexible nanoscale devices. One possible source of measurement error may originate from the local plastic deformation of the flexible device because of the exerted force by the probe tips, shown in Fig. 3a–c. Fig. 3d shows the representative electrical characteristics of two transistors that were measured before and after the layer transfer process indicating significant degradation of the p-FET performance, while the n-FET device performance appears to have remained nearly unchanged. To investigate the possibility of measurement artifacts as a result of the observed plastic deformation of the samples by the probe tips, the flexible circuits were rigidly bonded on a thick silicon handle wafer using silver epoxy for making electrical measurements. The comparison of the performance plots for a large number of nanoscale n- and p-FETs that were measured before and after the spalling process is shown in Fig. 4. The equivalent performance of the devices in this experiment suggests that the initial observation indicating the degradation of the flexible device characteristics is a measurement artifact and thus is not attributed to the spalling process.

Static random access memory (SRAM) cells form the backbone of SoC integrated circuits. The plot in Fig. 5a shows the butterfly curves for a flexible six-transistor (6T) SRAM cell with an area of 0.136 μm^2, illustrating the functionality of the memory cell with a good symmetry down to V_{DD} of 0.6 V. The results suggest the suitability of flexible ETSOI technology for ultra low-power applications. Another example of a deeply scaled flexible integrated circuit with a higher level of integration complexity involved the demonstration of functional ring oscillators (ROs) with the fanout of 3 and 101 stages. The plot in Fig. 5b shows the measured stage delay characteristics for a large number of flexible ROs on the flexible sample, exhibiting a stage delay as low as 16 ps at V_{DD} of 0.9 V, which is an unprecedented delay for a flexible circuit.

2.3. Effect of strain on device performance

Because of stress sharing, the intrinsic biaxial tensile stress of the nickel layer used for the spalling process induces a residual biaxial compressive stress in the thin-film semiconductor. The average compressive strain in the ultra-thin silicon circuits was simply measured from the displacement of the alignment marks on the thin-film samples relative to their original spacing before the layer transfer [26]. The average compressive strain was found to be about 0.15–0.18% for the flexible and bonded samples. From the electrical data, the small residual compressive strain does not appear to have impacted the electrical characteristics of the ETSOI devices.

Bending stability is an important factor when considering the suitability of a technology for application in flexible electronics. The transfer characteristics of an n-FET was monitored under different tensile bending conditions (Fig. 6), exhibiting slight V_{th}

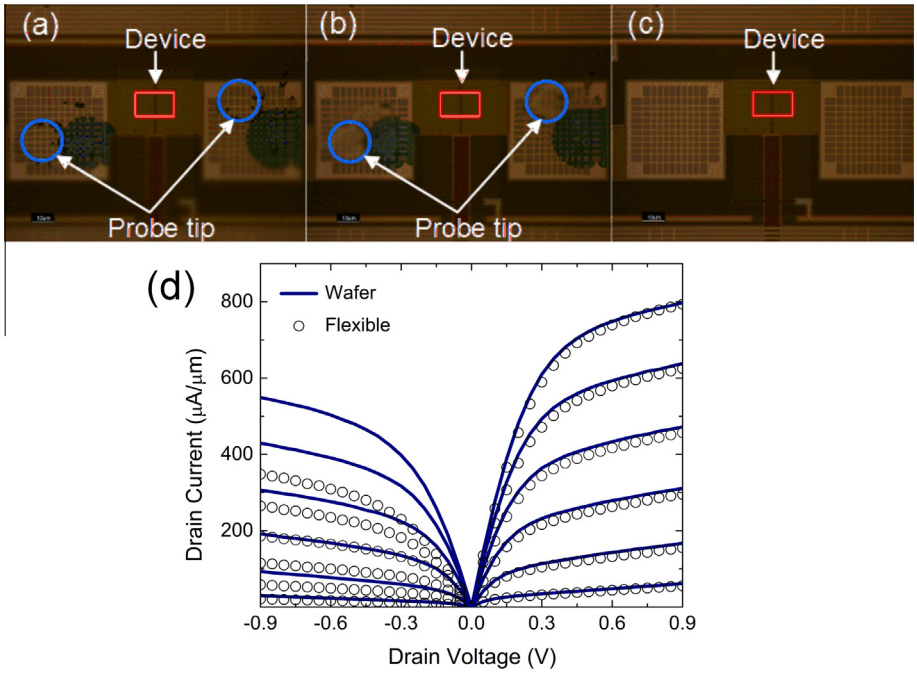

Fig. 3. Optical images of (a), (b) probed and (c) non-probed flexible devices. Different depth of focus between the pads and the device area indicates the plastic deformation of the probed regions. (d) Output characteristics of the same n-FET and p-FET, before and after the layer transfer process, indicating significant degradation of the drive current for the flexible p-FET.

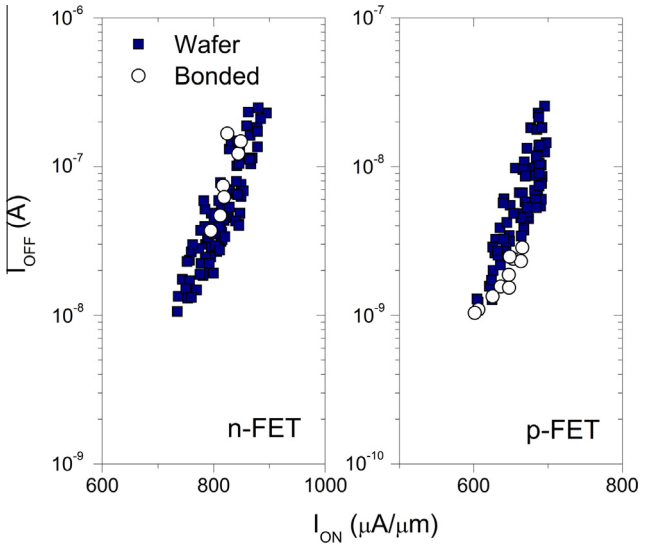

Fig. 4. Performance plots of n- and p-FET devices before and after the layer transfer, confirming that the device degradation shown Fig. 3(d), is a measurement artifact and caused by the probe pressure.

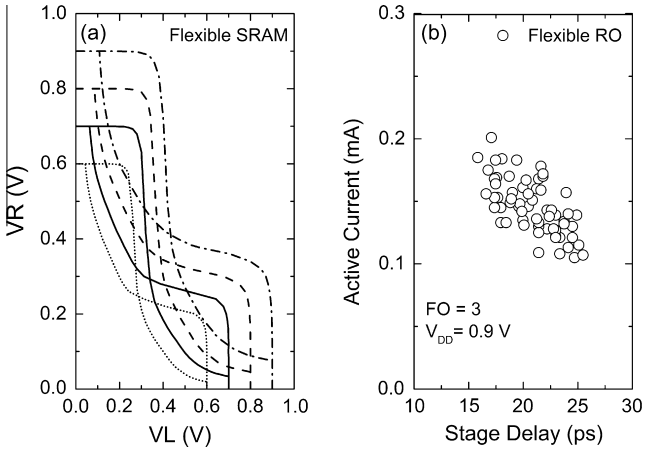

Fig. 5. (a) Butterfly curves of a flexible nanoscale 6T-SRAM cell exhibiting a good symmetry down to 0.6 V. (b) Stage delay characteristics of flexible ETSOI ring oscillators at 0.9 V.

shift to smaller values (ΔV_{th} = 35 mV at R = 6.3 mm), without changing the subthreshold slope of the device. In these experiments, the bending was performed along the direction of the current flow in the [1 1 0] channel direction. The level of the bending tensile strain ε_b for the flexible devices was estimated to be approximately 0.95% at R = 6.3 mm using $\varepsilon_b \approx t/2R$, where R is the bending radius and t is the total thickness of the flexible sample including the tape and the thin-film circuit. The observed shift in V_{th} of the n-FET device is attributed to the strain-induced change in the silicon conduction band by breaking the sixfold symmetry. It is notable that the observed shift in the threshold voltage is consistent with the previously reported theoretical and empirical results [30]. One possible solution to mitigate the effect of an external bending strain on the performance of transistors and the resulting circuits is to design a multilayer flexible system, in which the device-containing layer is located in the neutral stress plane, also known as zero-stress plane.

3. Optically-powered flexible ETSOI

As discussed earlier, one strategy for implementing flexible hybrid electronics is to utilize flexible energy harvesters that are not monolithically integrated with CMOS circuits. In this section, we discuss the application of flexible silicon and GaAs photovoltaic devices for powering up flexible ETSOI circuits.

Fig. 7a schematically illustrates the structure of the flexible silicon solar cell device. The devices are fabricated on n-type (1 1 1) silicon substrates. A $POCl_3$ diffusion process was first performed

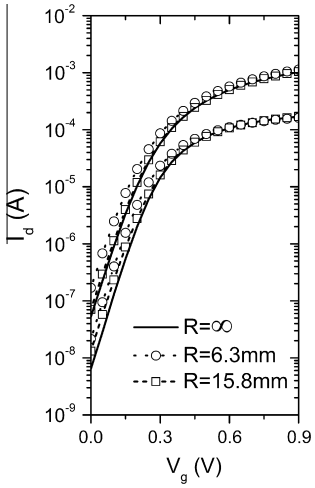

Fig. 6. Transfer characteristics of an nFET under different bending conditions measured at V_{ds} = 50 mV and V_{ds} = 1 V. The threshold voltage begins to shift to smaller voltages as the bending radius was reduced.

to create a Hi-Lo junction that forms the back-surface-field region of the solar cell device. Next, 100 nm thick SiO_2 was thermally grown during the phosphorous drive-in step, which serves as the surface passivation layer and the back reflector. The oxide layer was then patterned to form an array of 100 μm × 100 μm openings with a spacing of 2 mm. Next, the controlled spalling was performed, in which the thickness and the stress of the sputtered Ni layer was adjusted to be ~7 μm and ~400 MPa, respectively in order to separate the top ~20 μm of the silicon substrate. Since the thin-film silicon sample reside on a polyimide tape, a stack of i/p^+ a-Si:H was deposited at below 200 °C to form the emitter layer, followed by the deposition of the indium tin oxide (ITO) and aluminum front metal grid through shadow masks. Fig. 7b shows the photograph of the final flexible silicon solar cell on plastic. In addition, we fabricated single-junction GaAs solar cell devices with 3 μm thick absorber layer using a process similar to [27], shown in Fig. 7c. The current density–voltage (*J–V*) characteristics of the flexible silicon and GaAs devices were measured under simulated AM 1.5 solar spectrum at one sun intensity (100 mW/cm^2), shown in Fig. 7d. This plot underscores the advantage of the alternative integration approach that allows the use of non-silicon photovoltaic energy harvesters for powering flexible hybrid electronics. More specifically, compared with the flexible silicon solar cell, the flexible GaAs device is about 6 times thinner while it produces larger output voltage and output power.

In order to demonstrate the feasibility of flexible photovoltaic devices for powering flexible CMOS circuits, the flexible silicon and GaAs solar cells were directly connected to the flexible ETSOI ring oscillators. The performance of the flexible ROs powered by the flexible silicon and GaAs photovoltaic energy harvesters was monitored under different illumination intensities of 100 mW/cm^2 and 4 mW/cm^2. The area of the photovoltaic devices in these experiments was 1 cm × 1 cm. The plot in Fig. 8 illustrates the active current of the optically powered flexible ring oscillators as

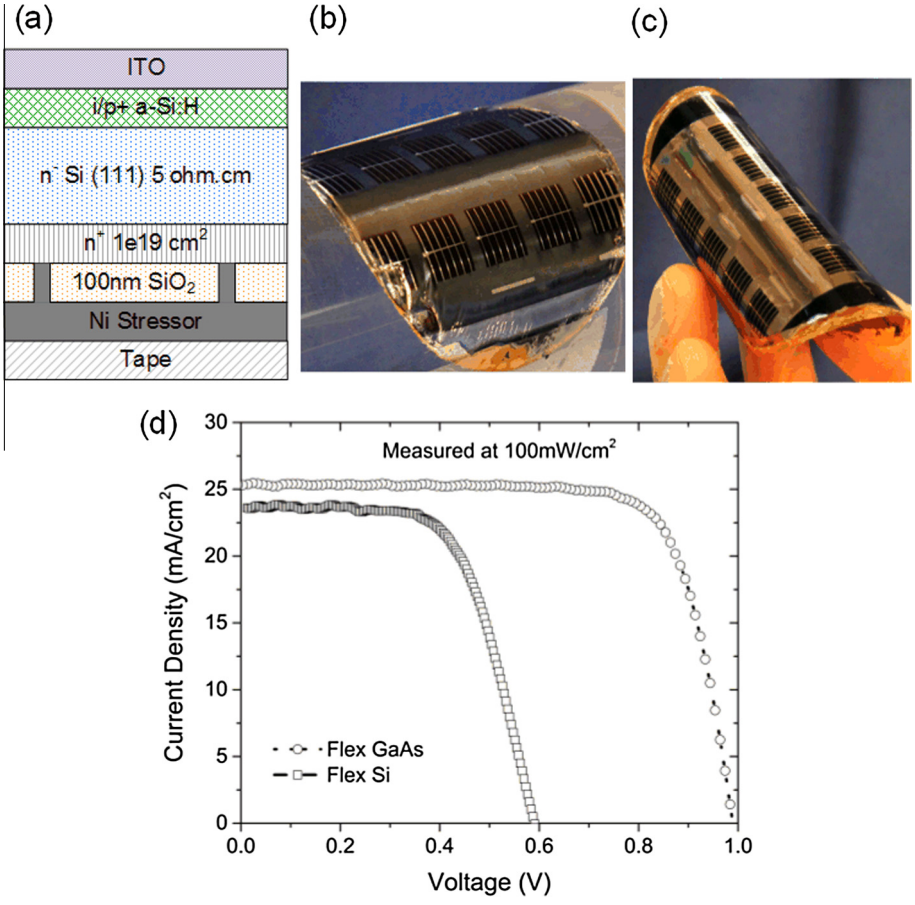

Fig. 7. (a) Schematic illustration of a flexible silicon solar cell. Photographs of flexible, (b) 20 μm thick silicon and (c) 3 μm thick GaAs solar cell devices on plastic. (d) Comparison of light *J–V* characteristics of flexible GaAs and silicon photovoltaic devices measured at 100 mW/cm^2, exhibiting the superior characteristics of the flexible GaAs photovoltaic devices.

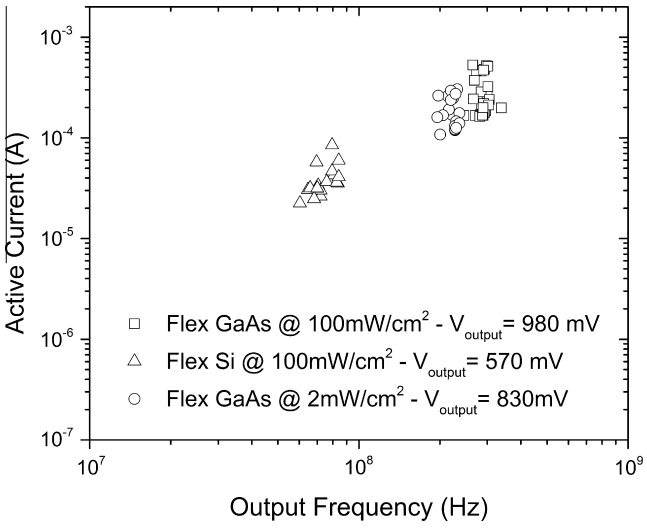

Fig. 8. Output frequency characteristics of flexible ETSOI ring oscillators power by flexible silicon and GaAs energy harvesters under different illumination conditions.

a function of their output frequency under different illumination conditions using the flexible silicon and GaAs solar cells. The results indicate the feasibility of photovoltaic energy harvesters for powering up the ETSOI circuits. Furthermore, the different output voltages in this plot were produced as a result of the change in the light intensity. It is important to note that the operating power point of solar cells is influenced by load and light intensity. Although the direct connection of the photovoltaic energy harvesters and the CMOS circuits is a straightforward method for performing feasibility studies, for practical applications, it is necessary to use additional circuitry for producing a regulated output voltage [31,32].

4. Conclusions

The present study demonstrated the solar-powered operation of flexible ETSOI circuits. Extensive electrical analyses of hundreds of devices confirmed that the performance of the ETSOI devices was preserved during the layer transfer process using the controlled spalling technique – an important requirement for flexible hybrid electronics technology. Furthermore, the superior attributes of the flexible GaAs solar cell compared to their silicon counterpart underscore the system-level advantages of non-silicon energy harvesters including higher level of mechanical flexibility, larger output voltage, and higher output power. Finally, our study indicates advantages of optically powered flexible ETSOI technology as a viable candidate of flexible hybrid electronics to create new paradigms in IoT that are inaccessible to established technologies.

Acknowledgments

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References

[1] John A, Seitz F. Electronics for the human body. Urbana 2015;51:61801.
[2] Sun Y, Rogers JA. Inorganic semiconductors for flexible electronics. Adv Mater 2007;19(15):1897–916.
[3] Kim DH, Ghaffari R, Lu N, Rogers JA. Flexible and stretchable electronics for biointegrated devices. Annu Rev Biomed Eng 2012;14:113–28.
[4] Ghaffari R. Stretchable bioelectronics for medical devices and systems. In: Bajaj A, Zavattieri P, Koslowski M, Siegmund T, editors. Proceedings of the Society Of Engineering Science 51st annual technical meeting, October 1–3, 2014. West Lafayette: Purdue University Libraries Scholarly Publishing Services; 2014. p. 2014.
[5] Caironi M, Noh Y-Y. Large area and flexible electronics. Hoboken (NJ): John Wiley & Sons Inc.; 2015.
[6] Jacquet D et al. 2.6 GHz ultra-wide voltage range energy efficient dual A9 in 28 nm UTBB FD-SOI. In: Symp VLSI tech; 2013. p. 44–5.
[7] Ishibashi K et al. A perpetuum mobile 32 bit CPU with 13.4 pJ/cycle, 0.14 μA sleep current using reverse body bias assisted 65 nm SOTB CMOS technology. In: IEEE COOL chips; 2014.
[8] Beigne E et al. A 460 MHz at 397 mV, 2.6 GHz at 1.3 V 32 bits VLIW DSP embedding F_{MAX} tracking. IEEE J Solid-State Circuits 2015;50(1):125–36.
[9] Clerc S et al. A 0.33 V/−40 °C process/temperature closed-loop compensation SoC embedding all-digital clock multiplier and DC–DC converter exploiting FDSOI 28 nm back-gate biasing. In: ISSCC; 2015.
[10] Ayazian S, Akhavan VA, Soenen E, Hassibi A. A photovoltaic-driven and energy-autonomous CMOS implantable sensor. IEEE Trans Biomed Circuits Syst 2012;6(4):336–43.
[11] Chen G, Ghaed H, Haque RU, Wieckowski M, Kim Y, Kim G, et al. A cubic-millimeter energy-autonomous wireless intraocular pressure monitor. In: 2011 IEEE international solid-state circuits conference digest of technical papers (ISSCC). IEEE; 2011. p. 310–2.
[12] Lee Y, Kim G, Bang S, Kim Y, Lee I, Dutta P, et al. A modular 1 mm 3 die-stacked sensing platform with optical communication and multi-modal energy harvesting. In: 2012 IEEE international solid-state circuits conference digest of technical papers (ISSCC). IEEE; 2012. p. 402–4.
[13] Ferrari M, Ferrari V, Guizzetti M, Marioli D. An autonomous battery-less sensor module powered by piezoelectric energy harvesting with RF transmission of multiple measurement signals. Smart Mater Struct 2009;18(8):085023.
[14] Penellalopez MT, Gasulla-Forner M. Powering autonomous sensors: an integral approach with focus on solar and RF energy harvesting. Springer Science & Business Media; 2011.
[15] Dini M, Filippi M, Costanzo A, Romani A, Tartagni M, Del Prete M, et al. A fully-autonomous integrated RF energy harvesting system for wearable applications. In: 2013 European microwave conference (EuMC). IEEE; 2013. p. 987–90.
[16] Paradiso JA, Starner T. Energy scavenging for mobile and wireless electronics. IEEE Pervasive Comput 2005;4(1):18–27.
[17] Chalasani S, Conrad JM. A survey of energy harvesting sources for embedded systems. In: IEEE southeastcon, April 2008. IEEE; 2008. p. 442–7.
[18] Evans AG, Drory MD, Hu MS. The cracking and decohesion of thin films. J Mater Res 1988;3(05):1043–9.
[19] Suo Z, Hutchinson JW. Steady-state cracking in brittle substrates beneath adherent films. Int J Solids Struct 1989;25(11):1337–53.
[20] Argon AS, Gupta V, Landis HS, Cornie JA. Intrinsic toughness of interfaces between SiC coatings and substrates of Si or C fibre. J Mater Sci 1989;24(4):1207–18.
[21] Drory MD, Thouless MD, Evans AG. On the decohesion of residually stressed thin films. Acta Metall 1988;36(8):2019–28.
[22] Dross F, Robbelein J, Vandevelde B, Van Kerschaver E, Gordon I, Beaucarne G, et al. Stress-induced large-area lift-off of crystalline Si films. Appl Phys A 2007;89(1):149–52.
[23] Martini R, Gonzalez M, Dross F, Masolin A, Vaes J, Frederickx D, et al. Epoxy-induced spalling of silicon. Energy Proc 2012;27:567–72.
[24] Bedell SW, Shahrjerdi D, Hekmatshoar B, Fogel K, Lauro PA, Ott JA, et al. Kerf-less removal of Si, Ge, and III–V layers by controlled spalling to enable low-cost PV technologies. IEEE J Photovolt 2012;2(2):141–7.
[25] Bedell SW, Fogel K, Lauro P, Shahrjerdi D, Ott JA, Sadana D. Layer transfer by controlled spalling. J Phys D Appl Phys 2013;46(15):152002.
[26] Shahrjerdi D, Bedell SW. Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic. Nano Lett 2012;13(1):315–20.
[27] Shahrjerdi D, Bedell SW, Bayram C, Lubguban CC, Fogel K, Lauro P, et al. Ultralight high-efficiency flexible InGaP/(In) GaAs tandem solar cells on plastic. Adv Energy Mater 2013;3(5):566–71.
[28] Cheng K, Khakifirooz A, Kulkarni P, Ponoth S, Kuss J, Shahrjerdi D, et al. Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications. In: 2009 IEEE international electron devices meeting (IEDM). IEEE; 2009. p. 1–4.
[29] Khakifirooz A, Cheng K, Nagumo T, Loubet N, Adam T, Reznicek A, et al. Strain engineered extremely thin SOI (ETSOI) for high-performance CMOS. In: 2012 Symposium on VLSI technology (VLSIT). IEEE; 2012. p. 117–8.
[30] Lim JS, Thompson SE, Fossum JG. Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs. IEEE Electron Dev Lett 2004;25(11):731–3.
[31] Ramadass YK, Chandrakasan AP. A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage. IEEE J Solid-State Circuits 2010;46(1):333–41.
[32] Liu X, Sanchez-Sinencio E. A highly efficient ultralow photovoltaic power harvesting system with MPPT for internet of things smart nodes. In: IEEE trans very large scale integration (VLSI) systems; 2015.