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Patterning metal contacts on monolayer MoS_2 with vanishing Schottky barriers using thermal nanolithography

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Two-dimensional semiconductors, such as molybdenum disulfide (MoS_2), exhibit a variety of properties that could be useful in the development of novel electronic devices. However, nanopatterning metal electrodes on such atomic layers, which is typically achieved using electron beam lithography, is currently problematic, leading to non-ohmic contacts and high Schottky barriers. Here, we show that thermal scanning probe lithography can be used to pattern metal electrodes with high reproducibility, sub-10-nm resolution, and high throughput ($10^5\ \mu m^2\ h^{-1}$ per single probe). The approach, which offers simultaneous in situ imaging and patterning, does not require a vacuum, high energy, or charged beams, in contrast to electron beam lithography. Using this technique, we pattern metal electrodes in direct contact with monolayer MoS_2 for top-gate and back-gate field-effect transistors. These devices exhibit vanishing Schottky barrier heights (around 0 meV), on/off ratios of 10^{10}, no hysteresis, and subthreshold swings as low as 64 mV per decade without using negative capacitors or hetero-stacks.

As conventional electronic devices reach their limits of performance, a search is underway in the microelectronics industry to find new materials[1], fabrication methods[2] and architectures[3]. Conventional lithographic techniques are, in particular, problematic in terms of resolution (optical lithography), operational costs (electron beam lithography, EBL), and their ability to pattern novel electronic materials and architectures. Among various novel materials being considered, two-dimensional (2D) molybdenum disulfide (MoS_2) is of particular interest due to its large bandgap, low dielectric constant, and heavy carrier effective mass[3–6]. At present, a key issue in creating high-performance field-effect transistors (FETs) based on MoS_2 and other transition metal dichalcogenide (TMDC) films is the poor quality of the metal contacts fabricated on these atomic layers, which gives rise to non-ohmic contacts, high Schottky barriers and large contact resistances[1,7]. Several approaches have been proposed to address these problems[8], including trying different metallic alloys and doping[9,10], using a metallic phase of MoS_2[11] or a hexagonal boron nitride (h-BN) layer as interface between the metal contact and the semiconducting MoS_2 layer[12], and exploiting graphene as contact[13–15]. However, all these strategies are either non-scalable or have not yet been fully developed. They also all rely on conventional fabrication methods, typically EBL, for metal contact patterning.

EBL is currently the most widespread and reliable nanomanufacturing method for metal electrode patterning when nanoscale dimensions are required. The technique requires ultrahigh vacuum (UHV) and does not allow in situ imaging. Its scalability is also limited by the costs and complexity of multi-beam systems. Furthermore, primary and secondary electrons in EBL, as well as ultraviolet (UV) exposure in optical lithography, can damage 2D materials, from graphene to TMDC films[16–20]. Moreover, resist contamination on the surface of the 2D material is a major impediment for the fabrication of high-performance electronic devices[21–27]. Among other nanopatterning methods, laser direct writing is a promising technique that offers far-field three-dimensional, maskless and cost-effective optical beam lithography with high throughput, even if the diffraction limit is a barrier for achieving nanoscale resolution. Laser direct writing has, for example, been shown to be effective in patterning electrodes by direct laser sintering of metal nanoparticle inks deposited on a substrate[25].

In this Article, we report a strategy to fabricate metal contacts on 2D materials with high reproducibility. Our approach is based on a double polymer stack chemical etching/lift off process combined with thermal scanning probe lithography (t-SPL). Using a commercial system based on t-SPL[2,28–31], top-gated and back-gated monolayer (a single atomic layer, 1L) MoS_2 FETs are fabricated with different metals as direct contacts on the MoS_2. The approach does not require a vacuum, allows for in situ simultaneous patterning and imaging of a monolayer of MoS_2, can achieve sub-10-nm resolution, gives rise to no resist contamination, and completely eliminates

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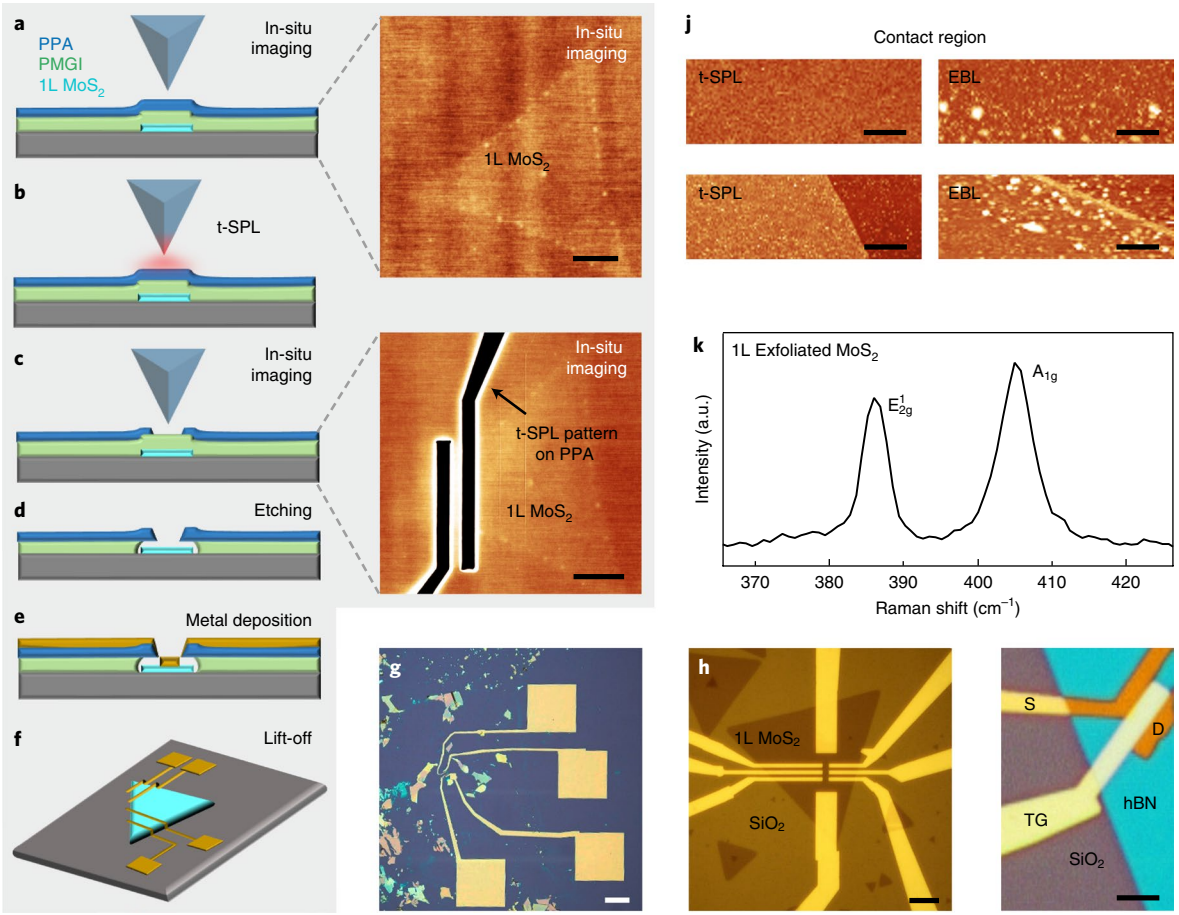


Fig. 1 | The t-SPL fabrication process. a, In situ thermal nanoimaging of the sample topography (see also Supplementary Section 1). Image of a monolayer MoS_2 flake underneath the PMGI/PPA polymer stack (230 nm). Scale bar, 4 μm. **b**, The PPA polymer film is locally evaporated by scanning a heated scanning probe on its surface at a throughput of 10^5 μm^2 h^{-1}. **c**, In situ thermal nanoimaging of the t-SPL pattern on PPA. Scale bar, 4 μm. **d**, Chemical etching of the now-exposed PMGI polymer film, which uncovers selected areas of the MoS_2 surface. **e**, Metal contacts are deposited via evaporation. **f**, The PMGI and PPA films are removed via a lift-off process. **g**, **h**, Optical images of final devices fabricated on exfoliated and CVD monolayer MoS_2, respectively. Scale bars, 50 μm (**g**) and 5 μm (**h**). **i**, Optical image of a top-gate contact fabricated on exfoliated h-BN flakes. Scale bar, 4 μm. **j**, Comparison between the exposed contact region after the chemical etching step and before metal deposition in t-SPL- (left) and EBL-fabricated (right) FETs on monolayer CVD MoS_2, acquired inside (top) and at the boundaries (bottom) of monolayer CVD MoS_2. Scale bars, 500 nm. **k**, Typical Raman spectra of monolayer exfoliated MoS_2 used for the fabrication of FETs via t-SPL. a.u., arbitrary units.

damage from either electrons or photons. As a result, the t-SPL-fabricated FETs exhibit on/off ratios up to 10^{10}, Schottky barrier heights (SBH) close to 0 mV, and subthreshold swings as low as 64 mV per decade without using negative capacitors or hetero-stacks, outperforming EBL results in the literature[4,32–36]. Applications to other TMDCs are also reported. The technique, which currently runs with a single scanning probe, has a throughput similar to EBL and can readily be implemented in a cost-effective manner to multiple probes to increase throughput.

MoS_2 FETs fabrication by t-SPL

Our approach to patterning metal contacts uses a two-layer polymer stack (Fig. 1), uniformly spin-coated on MoS_2 films. The top polymer layer is locally thermally decomposed/evaporated in less than 1 μs using a heated nanoprobe[28–31] in t-SPL (see Supplementary Information, Supplementary Figs. 1,2 and Supplementary Video 1), while the removal and optimal undercut profile of the exposed bottom polymer layer is obtained by selective chemical etching and prebake conditions (see Methods). Polyphthalaldehyde (PPA)[29] serves as the top layer resist (20 nm thick) due to its remarkable thermal sensitivity, whereas polymethylglutarimide (PMGI) is used as the sacrificial bottom layer (210 nm thick) for the high-yield and high-resolution metal lift-off process. Before starting the electrode patterning, the 1L MoS_2 structure is imaged in situ underneath the polymer stack via thermal nanoimaging (see Fig. 1a, Supplementary Information, and Supplementary Fig. 1). Single-digit-nanometre patterns in PPA, with lateral resolutions of less than 10 nm and vertical resolutions of 1 nm, can be reproducibly achieved[2,37,38] (see Supplementary Fig. 2). Moreover, the PPA thermally decomposed products evaporate immediately without re-deposition on the substrate or contaminating the nanoprobes, facilitating a complete residual-free and clean patterning process. The patterned PPA does not require any chemical development and can readily be used as an etching mask with high mechanical stability. After t-SPL patterning of PPA (Fig. 1b), the PMGI layer is locally exposed without PPA residuals, and the patterned area can be directly imaged to check the correct alignment of the pattern (Fig. 1c) before initiating the PMGI chemical etching (Fig. 1d). After PMG-selective removal, the patterned MoS_2 contact region is exposed and ready for metal deposition. The final step consists in the evaporation of the metal electrodes (Fig. 1e) and lift-off (Fig. 1f) (see also Methods). Figure 1g–i shows optical images of different examples of t-SPL-fabricated FETs on 1 L CVD and exfoliated MoS_2 flakes, illustrating that both large pads (Fig. 1g) and fine electrodes (Fig. 1h) can be fabricated by t-SPL.

Imaging by atomic force microscopy (AFM) (see Fig. 1j) indicates that the patterned MoS_2 contact region is completely free of any resist residue, whereas the contact region after the conventional EBL process shows considerable resist residues. Extensive AFM characterization of different locations on MoS_2 flakes after t-SPL and EBL fabrication shows, in the case of the EBL process, damage of the flakes' edges and the presence of residuals (see Supplementary Section 3 and Supplementary Figs. 4–6). Furthermore, X-ray photoemission spectroscopy (XPS) indicates that these residuals are indeed residues of the PMMA resist used during the EBL process (see Supplementary Section 4 and Supplementary Fig. 7). Figure 1k shows the Raman spectroscopy characterization of a typical exfoliated 1L MoS_2 flake used for FET fabrication, confirming that the E^1_{2g} and A_{1g} modes are separated by 19 cm^{-1}, characteristic of monolayer flakes[39–41]. The exfoliated[42] and CVD MoS_2 flakes used in this work have all been characterized by Raman spectroscopy to confirm their monolayer nature (see Supplementary Section 6 and Supplementary Fig. 10). Representative AFM images of monolayer exfoliated and CVD flakes used in this work are shown in Supplementary Fig. 11. The t-SPL-fabricated 1L MoS_2 FETs channel region is also characterized by Raman spectroscopy after fabrication (see Supplementary Section 5 and Supplementary Fig. 9), confirming that the t-SPL process does not damage MoS_2. We remark that, differently from t-SPL, it has been shown that, during EBL, electron beam irradiation can cause damage in 2D materials[43,44].

The bottom device layer, in this case monolayer MoS_2, is not heated ($T < 50$ °C) during the t-SPL patterning process, as verified by thermal flow finite-element simulations (see Supplementary Fig. 3). Moreover, after each writing line, the non-heated nanoprobe reads the written line, allowing for in situ correction, closed-loop patterning and self-alignment. In addition, t-SPL allows imaging of the surface before patterning using the same, non-heated probe used for t-SPL, localizing the area where the patterns need to be fabricated, and aligning features with nanometric precision, without the necessity for additional markers. The versatility of t-SPL allows fabrication on a wide range of materials, as shown in Fig. 1i, where we present the optical image of an aligned top-gate (TG) fabricated by t-SPL on an exfoliated h-BN flake (see discussion of Fig. 2); in the Supplementary Information we also report on monolayer WSe_2 FETs. Finally, the t-SPL throughput can be scaled up by multiplexing the nanoprobe arrays[30] (see Supplementary Fig. 1e), in contrast to EBL, in which multiplexing is complex and costly.

t-SPL 1L MoS_2 FETs electrical characterization

To demonstrate the capabilities of t-SPL, we fabricate dual-gate 1L MoS_2 FETs with aligned patterned top gates. First, Pd/Au source and drain contacts are fabricated, as shown in Fig. 1. Then, a 15–20 nm insulating h-BN flake is aligned and transferred to the FET as gate dielectric. After coating of the PMGI/PPA layers stack, the topography of the system was acquired in situ via thermal nanoimaging. This process allows one to directly visualize, with nanometric precision, the source/drain contacts underneath the resist as well as the h-BN flake, and precisely align the top-gate with no need for additional markers (see Supplementary Fig. 12).

Figure 2a shows a schematic of the cross-section of a top-gate 1L MoS_2 FET, with the electrical connections used in the measurements. In Fig. 2b, the optical image of the FET is shown. The regular geometry of the rectangular 1L MoS_2 flake (red dashed line in Fig. 2b, see Supplementary Fig. 13 for the optical image of the pristine flake) allows precise measurement of the channel length $L = 1.9$ µm and width $W = 3.5$ µm. Figure 2c reports the room-temperature transfer curve of the FET for a drain voltage $V_{ds} = 2$ V, measured by recording the drain current I_d as a function of the top-gate voltage V_{tg}. It features a nearly-ideal 64 mV per decade subthreshold swing, combined with the highest on/off ratio reported in the literature for a 1L MoS_2 FET of $I_{on}/I_{off} = 5 \times 10^9$. In the inset, the top-gate transfer curves are presented as a function of the back-gate voltage, ranging from $V_{bg} = -20$ V (yellow curve) to $V_{bg} = +20$ V (blue curve), demonstrating the full functionality of the dual-gate t-SPL-patterned FET. The high quality of the t-SPL contacts is demonstrated also in Fig. 2d, where the output curves of the FET for small V_{ds} are presented. The curves, acquired by recording the drain current I_d as a function of the drain voltage V_{ds}, are linear, demonstrating the ohmic character of the contacts.

To evaluate the performance of the device in terms of the on-current I_{on}, we performed additional measurements at higher V_{ds} and V_{tg} after keeping the device in vacuum for one week. In Fig. 2e, we report I_d as a function of V_{ds} up to 4 V, for different top-gate voltages ranging from $V_{tg} = -2.5$ V (orange curve) to $V_{tg} = 10$ V (black curve). The device features an extremely high $I_{on} = 154$ µA, which gives rise to the normalized value of $I_{on}L/W = 84$ µA, which is among the highest values reported for monolayer MoS_2 FETs (see discussion of Fig. 5). We remark that the corresponding transfer curve, reported in the inset, features a very low off current I_{off}, leading to the record-high $I_{on}/I_{off} = 2 \times 10^{10}$. The equivalency of the source and drain currents, acquired throughout the whole measurements (see Supplementary Fig. 14), confirms the high quality of the h-BN gate dielectric and fabrication process. Figure 2f reports the forward and reverse transfer curve at $V_{ds} = 2$ V, plotted both on logarithmic and linear scales. Importantly, it demonstrates a hysteresis-free transfer curve across the whole range of V_{tg}, due to the absence of defects and trapped charges at the dielectric interface. This provides an additional compelling demonstration that t-SPL enables a residue-free and defect-free fabrication process, which in turn preserves an extremely high quality of the materials and interfaces.

The electrical characterization of two back-gate exfoliated 1L MoS_2 FETs with Pd/Au contacts fabricated by t-SPL is shown in Fig. 3. The corresponding optical images of the devices are shown in the insets. The devices feature a channel length and width of $L = 0.6$ µm, $W = 1$ µm (Fig. 3a) and $L = 1.9$ µm, $W = 3.5$ µm (Fig. 3b). Room-temperature transfer characteristics (drain current I_d as a function of the back-gate voltage V_{bg}) are measured by sweeping V_{bg} up to +60 V with a drain voltage $V_{ds} = 2$ V. Both FETs show considerably large on-currents of 132 µA and 112 µA, respectively, which leads to normalized on-current values $I_{on}L/W$ of 84 µA and 62 µA, respectively, combined with extremely high I_{on}/I_{off} values of 3.5×10^8 and 3.4×10^9, respectively. The subthreshold swings are 500 mV per decade and 400 mV per decade, respectively, which is remarkably low for a thick global SiO_2 back gate[45]. The insets show the corresponding room-temperature output curves, featuring a linear I_d (V_{ds}) behaviour at all V_{bg}, from −60 V to +60 V, and even at low temperatures (see inset of Fig. 4a), indicating an ohmic contact between the t-SPL patterned electrodes and MoS_2. We remark that, as reported in the detailed comparison with the literature of Fig. 5, these back-gate devices feature a state-of-the-art on-current combined with a record-high I_{on}/I_{off}.

In a direct metal–MoS_2 contact there are two main components contributing to the contact resistance: the tunnelling barrier between the metal and MoS_2 due to the van der Waals gap, and the Schottky barrier between the contact and the channel region. Schottky barrier height (SBH) values vary from 370–380 meV (refs. [33–36]) for metals in direct contact with 1L MoS_2, to 16 meV when using h-BN/MoS_2 stacks[36]. Values obtained between multilayer MoS_2 and contact metals vary between 50 meV with Ti and 30 meV with Sc (ref. [46]), larger SBH have been found for monolayer MoS_2 with Ti, namely 350 meV, in part because of its smaller electron affinity (4.2 eV)[42]. The SBH is related to many factors and is a complex phenomenon[1] which accounts for the work function difference between metal and MoS_2, diffusion and doping of the metal atoms in the MoS_2 layer[42,47], the presence of defects[48], and the presence of adsorbates of various origin, including resist residuals[1,49]. To evaluate the SBH

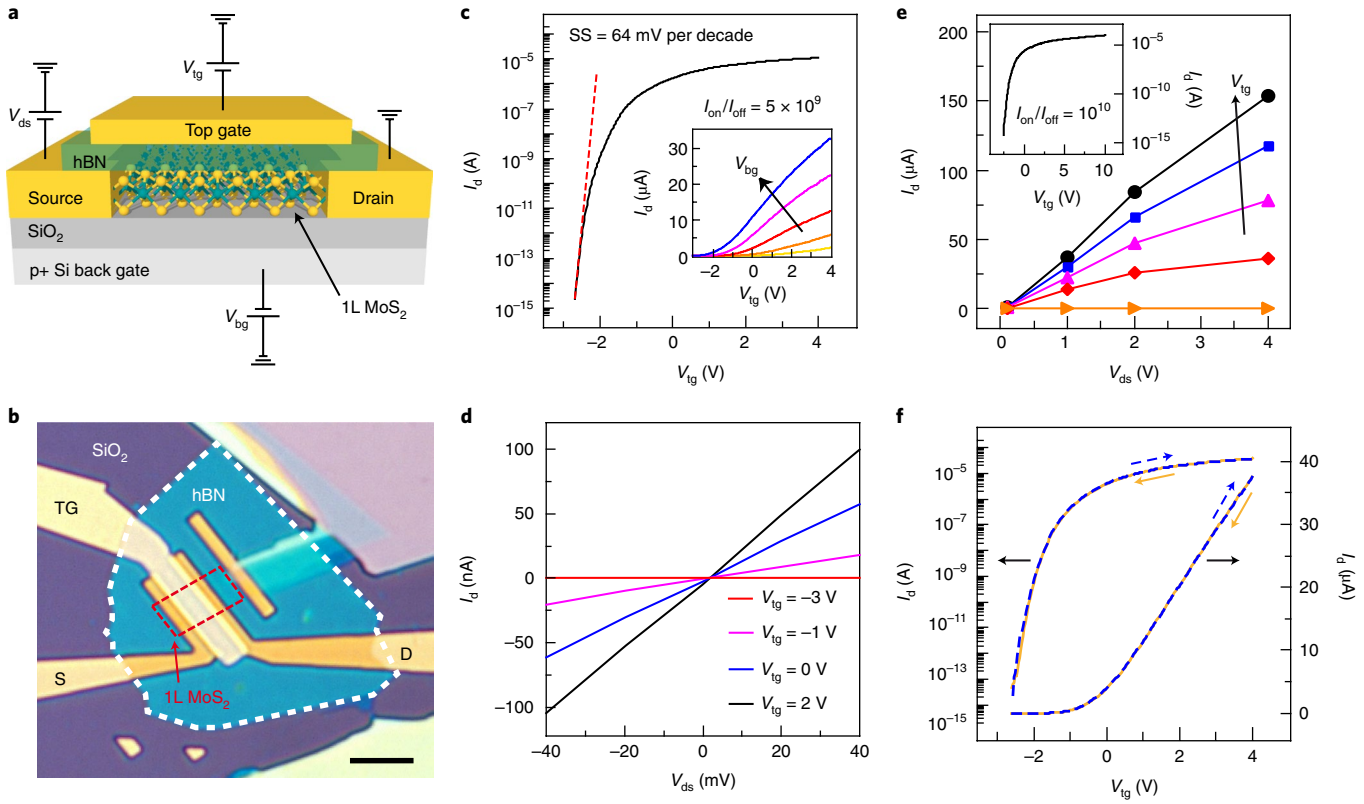


Fig. 2 | Aligned top-gate FETs on exfoliated 1L MoS_2 flakes patterned by t-SPL. a, Schematic cross-section and electrical connections of a top-gate FET. Both the source–drain contacts and the aligned top-gate are patterned via t-SPL. The structure comprises the degenerately doped Si substrate as global back gate, a 285 nm thermal SiO_2 as back-gate dielectric, and a 15 nm h-BN layer as top-gate dielectric. **b**, Optical image of the 1L MoS_2 FET, showing the source–drain Pd/Au electrodes (S-D) fabricated on the 1L MoS_2 (red dashed line) and the aligned top-gate Cr/Au contact (TG) fabricated on the h-BN dielectric. Channel length $L = 1.9$ μm, channel width $W = 3.5$ μm. Scale bar, 5 μm. **c**, Room-temperature transfer curve of the top-gate FET measured at $V_{ds} = 2$ V. Subthreshold swing (SS) = 64 mV per decade, $I_{on}/I_{off} = 5 \times 10^9$. In the inset, transfer curves at different back-gate voltages ranging from $V_{bg} = -20$ V (yellow curve) to $V_{bg} = 20$ V (blue curve). **d**. Small-voltage I_d (V_{ds}) curves at different top-gate voltages showing ohmic behaviour of the contacts. **e**, I_d as a function of V_{ds} up to 4 V, at different top-gate voltages ranging from $V_{tg} = -2.5$ V (orange curve) to $V_{tg} = 10$ V (black curve), showing a maximum $I_{on} = 154$ μA. In the inset, the transfer curve at $V_{ds} = 4$ V features an $I_{on}/I_{off} = 2 \times 10^{10}$. **f**, Forward (blue dashed line) and reverse (orange line) transfer curves on logarithmic and linear scales. The curves are hysteresis-free in the whole top-gate voltage range.

of the t-SPL-patterned electrodes, temperature-dependent transfer characteristics are collected on exfoliated 1L MoS_2 FETs with different metal contacts.

First, the transfer curves of the t-SPL-patterned FETs with Pd/Au electrodes (as reported in Fig. 3) are obtained at different temperatures at $V_{ds} = 0.1$ V, as shown in Fig. 4a. For positive gate voltages, the drain current decreases with increasing temperature, indicating a metallic behaviour, whereas for negative biases this temperature dependence is reversed, giving rise to insulating characteristics. This transition manifests as a crossing-over at $V_{bg} \sim 10$ V in Fig. 4a, and is known as the metal–insulator transition (MIT)[50–52]. The corresponding output curves at 48 K are plotted in the inset of Fig. 4a, showing a linear behaviour even at low temperatures. Together, the metallic temperature dependence shown in Fig. 4a and the linearity of the current–voltage (I–V) curves at all temperatures (see Fig. 3 and inset of Fig. 4a) indicate a vanishing SBH (also confirmed by the Arrhenius plots as a function of V_{bg} as described below) and an ohmic behavior of the t-SPL-patterned FET with Pd/Au electrodes.

Moreover, Al/Au contacts are patterned by t-SPL on a 1L exfoliated MoS_2 flake. The temperature-dependent transfer curves obtained at $V_{ds} = 2$ V are shown in the inset of Fig. 4b. To evaluate the SBH, the variations of the current through the device as a function of V_{bg} under different temperatures are used to generate the Arrhenius plots reported in Supplementary Fig. 15. It is well known that in a FET the current depends mainly on the thermionic emission and the thermally assisted tunnelling, and when V_{bg} is below the flat-band voltage, I_d can be written as[1,9,12,34]:

$$I_d = A_{2d}^{*} T^{3/2} \exp\left(-\frac{q\Phi_B}{k_B T}\right)\left[1-\exp\left(-\frac{qV_{ds}}{k_B T}\right)\right] \quad (1)$$

where A_{2d}^{*} is the 2D equivalent Richardson constant, Φ_B is the SBH, T is the absolute temperature, k_B is the Boltzmann constant and q is the electronic charge. Since we are considering $qV_{ds} >> k_B T$, equation (1) can be simplified to obtain a linear relationship between $\ln(I_d/T^{3/2})$ and $1/T$. In particular, the SBH is determined from the slope of the Arrhenius plots and plotted as a function of V_{bg} in Fig. 4b. It can be clearly seen that the thermionic emission current dominates when V_{bg} is lower than the flat-band voltage, which corresponds to the voltage at which the activation energy stops depending linearly on V_{bg}. Therefore, the flat-band Schottky barrier height for t-SPL-patterned Al/Au contacts can be readily determined from Fig. 4b to be merely 12.5 meV.

To the best of our knowledge, 12.5 meV and the vanishingly small barrier observed in Pd/Au devices are the smallest SBH ever demonstrated in any EBL-patterned direct metal contact on MoS_2

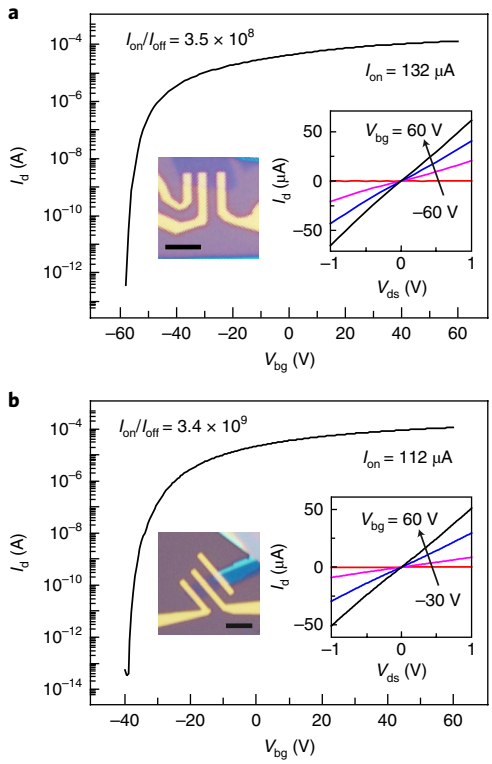


Fig. 3 | Back-gate FETs fabricated via t-SPL on exfoliated 1L MoS_2 flakes. **a**,**b**, Room-temperature transfer curves at V_{ds} = 2 V of FETs with Pd/Au electrodes, fabricated on exfoliated 1L MoS_2. The Si/SiO_2 285 nm substrate was used as global back gate and gate dielectric, respectively. The devices feature I_{on} up to 132 μA (**a**) and $I_{on}/I_{off} > 3 \times 10^9$ (**b**). Scale bars, 2 μm (**a**), 5 μm (**b**). Insets, corresponding room-temperature output curves at different back-gate voltages V_{bg}.

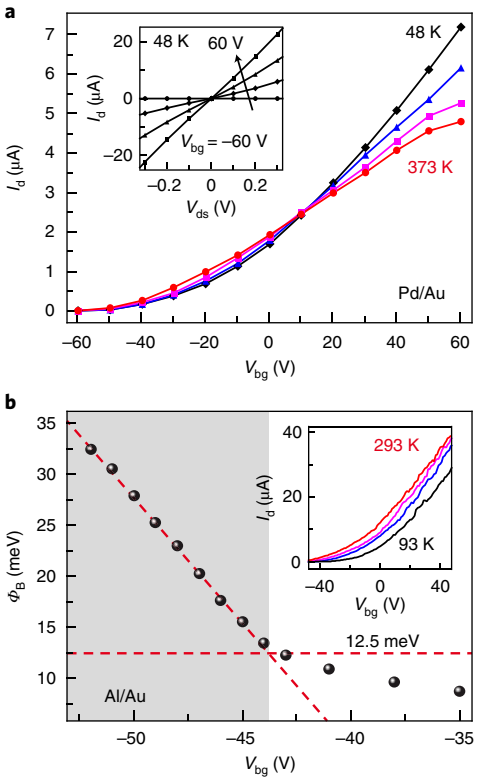


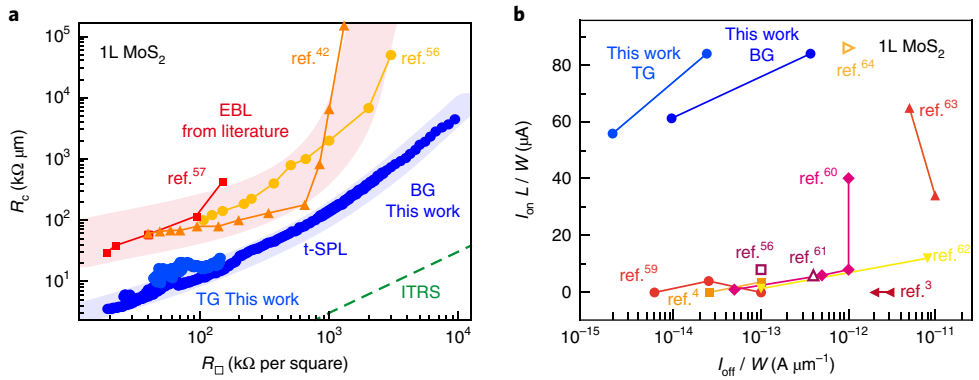
Fig. 4 | Schottky barrier height characterization of t-SPL FETs on exfoliated 1L MoS_2. **a**, Temperature-dependent transfer curves of the t-SPL FET with Pd/Au electrodes reported in Fig. 3a (V_{ds} = 0.1 V). Inset, corresponding output curves of the same FET at 48 K. **b**, Gate voltage dependence of the barrier height for a t-SPL-patterned FET on 1L exfoliated MoS_2 with Al/Au electrodes, at V_{ds} = 2 V. The deviation from the linear response at low V_{bg} (dashed red line) defines the flat band voltage and the SBH. Inset, corresponding temperature-dependent transfer curves at V_{ds} = 2 V.

back-gated FETs[1,33–35,42,53,54]. The best value reported for 1L exfoliated MoS_2 direct contacts is 38 meV (ref. [36]) and for multi-layer MoS_2 is 30 meV (ref. [46]). We notice that Al/Au contacts give larger SBH than Pd/Au in our t-SPL-patterned FETs. The factors that could potentially influence the contact resistance and the SBH in a given metal contact include[42,47,48,33,55] variations in surface contamination, defect and surface states concentration in the material, field emission, metal/semiconductor wavefunction overlap (predicted for metals on graphene to result in an effective lowering of the metal work function that may also apply to MoS_2), metal-induced gap states (MIGS), defect-dominated Schottky barrier height, interface dipole formation and metal–semiconductor-interaction-induced gap states. Also, complex mechanisms, which are metal-specific, have been highlighted as important factors in studying the metal/MoS_2 monolayer interface; for example, *s*-electron metals such as Ag, Al and Au have fully occupied *d*-orbitals and interact with MoS_2 weakly, whereas the *d*-electron metals such as Pd interact with MoS_2 strongly. We argue that the observed absence of damage at the edges and the residual-free surfaces observed for the t-SPL process as opposed to EBL (see Supplementary Figs. 4–7) may be the underlying reason for the observed vanishingly small SBH in the t-SPL 1L-MoS_2-FETs. It is indeed possible that by freeing the metal–MoS_2 interface from polymer residuals, we may change the nature itself of the interface; for example, by increasing the metal/MoS_2 interaction and the MIGS. Further experiments are required to understand the microscopic origin of the different contact behaviour for different metals and for the t-SPL and EBL processes.

Comparison of t-SPL FETs with literature results

To quantitatively characterize the quality of the t-SPL electrodes and compare them with state-of-the-art electrodes patterned with conventional methods, we have derived the contact resistance (R_c) of the different t-SPL-fabricated contacts on 1L MoS_2. Since the contact resistance depends mainly on the quality of the contact interface and on the resistivity of the MoS_2 film itself, a reliable comparison should involve MoS_2 films having similar sheet resistance to separate the effect of the contact from the effect of the material properties[1]. Accordingly, in Fig. 5a we plot the contact resistance of t-SPL-fabricated electrodes as a function of the sheet resistance ($R_\square$) for both top-gate and back-gate devices shown in Figs. 2,3 (see also Supplementary Figs. 16a,17), Fig. 4 and Supplementary Fig. 19 (blue lines and symbols), and compare these values with the EBL results reported in the literature[42,56,57] (red and yellow lines and symbols). We remark that the sheet resistance of a MoS_2 film can be modulated by changing the gate voltage in the corresponding FET.

In general, the contact resistance is expected to decrease with the sheet resistance. For example, the International Technology Roadmap for Semiconductors (ITRS) 22-nm-node requirement for low-standby-power silicon-on-insulator FETs[1], plotted in Fig. 5a (green dashed line), shows that the goal in terms of contact formation is to reduce the intercept of the linear R_c versus $R_\square$ curves; that is, to obtain contacts with lower contact resistance for samples having the same sheet resistance. When analysing the data related to EBL electrodes on MoS_2, we notice that the R_c versus $R_\square$ data points



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Layers	Configuration	I_{on}/I_{off} , S (mV per decade)	$I_{on}L/W$ (μA)	Ref.
Multilayer	Bottom gate Negative capacitor	10^6–10^7, < 60	50	[60]
Multilayer	Bottom gate (SiO_2) UHV contacts	-	45	[58]
1L	Top gate	10^6, 500	11	[65]
1L	Aligned bottom gate (graphene contact)	10^7, 64	1.5	[62]
1L	Top gate	10^8, 74	3.75	[4]
1L	Top gate	10^8, 178	86	[64]
1L	Top gate	10^9–10^{10}, 64	84	This work
1L	Bottom gate (SiO_2)	10^9, 400	62–84	This work

Fig. 5 | Comparison of t-SPL MoS_2 FET performances with literature values. a, Contact resistance R_c of the electrodes as a function of the sheet resistance $R_□$ of 1L MoS_2 FETs. The red, orange and yellow lines and symbols represent values extracted from the literature for FETs fabricated by EBL. The blue lines and symbols show the results of t-SPL-fabricated FETs which are extracted (right to left) from three back-gated FETs fabricated on 1L CVD (see Supplementary Fig. 19), 1L exfoliated MoS_2 flakes (as shown in Fig. 3 and Fig. 4), and a top-gate FET fabricated on a 1L exfoliated MoS_2 flake (as shown in Fig. 2). The shaded stripes show the range of data corresponding to EBL data from the literature (red) and t-SPL data from this work (blue). The green dashed line represents the ITRS 22-nm-node requirement for low-standby-power silicon-on-insulator FETs with the contact resistance down to 20% of the total resistance. **b**, On-current normalized to the channel width W and length ($I_{on}L/W$), as a function of I_{off}/W, for 1L MoS_2 FETs. The red and yellow symbols and lines represent EBL data extracted from the literature. The blue symbols and lines show the t-SPL results presented in this work for 1L MoS_2 FETs in the back-gate (Fig. 3) and top-gate (Fig. 2) configurations. **c**. In-depth comparison of the performances of the best MoS_2 FETs presented in the literature with the t-SPL results presented in this work.

for 1L exfoliated flakes follow the same curve, suggesting comparable contact quality (see the shaded stripe in red, as a guide to the eyes).

Here, by using t-SPL to fabricate the electrodes, we show that we are able to greatly lower the R_c versus $R_□$ curves for direct metal contacts on 1L MoS_2 in both top-gate and back-gate configurations. This is clearly demonstrated from the blue symbols reported in Fig. 5a. Data are extracted from transport measurements on transfer length measurement (TLM) structures fabricated on chemical vapour deposited (CVD) 1L MoS_2 (see Supplementary Section 11 and Supplementary Figs. 19,20), and using the Y-function method to analyse the data from the electrical measurements on top-gate and back-gate exfoliated 1L MoS_2FETs, as reported in Figs. 2–4 (for the Y-function method, see Supplementary Section 12 and Supplementary Fig. 21). It is evident that the t-SPL-patterned contacts show one order of magnitude smaller contact resistance compared to EBL-patterned electrodes for MoS_2 samples having the same sheet resistance. The lowest contact resistance obtained for a t-SPL FET with CVD 1L MoS_2 is ~20 kΩ·μm (ref. [56]), whereas, as expected, the t-SPL FETs with exfoliated flakes show much smaller sheet resistance than CVD MoS_2, with a minimum contact resistance of only 3 kΩ·μm at V_{ds} = 2 V, for the device shown in Fig. 3a. This is one of the lowest values ever reported for direct metal MoS_2 monolayer contact[1,33,42,56,58] at this V_{ds}. For example, Liu et. al.[42] demonstrated a contact resistance of 3 kΩ·μm at V_{ds} = 2 V. We notice that the dependence of the contact resistance on the sheet resistance of the exfoliated MoS_2 t-SPL FETs follows the same line as for CVD MoS_2 t-SPL FETs, indicating that the improvement in contact quality is independent of material source or quality. Although these curves represent the present benchmark of the t-SPL-patterned electrodes, they can certainly be further improved by using additional strategies recently proposed in the literature for improving contacts, such as the use of a dielectric tunnelling layer[36], 1T phase engineering[11], and the use of graphene for the contacts[15].

Figure 5b shows the detailed comparison of the on-current $I_{on}L/W$ and off-current I_{off}/W of the t-SPL 1L MoS_2 FETs, with the best values found in the literature. To compare effectively the contact quality in FETs with different geometries, the normalization to the channel width and length is crucial. In Fig. 5b, red and yellow symbols and lines report the data for EBL 1L MoS_2 FETs[3,4,56,59–64], whereas blue lines and symbols represent t-SPL 1L MoS_2 FETs presented in this work. It is noteworthy that the great majority of EBL FETs are characterized by relatively low normalized I_{on} below 10 μA, and the FETs characterized by higher on-current feature a correspondingly larger off-current, leading to a notable reduction of the I_{on}/I_{off}. Remarkably, t-SPL FETs feature a normalized I_{on} current which is the among the best reported, combined with an extremely low I_{off} current, leading to record-high I_{on}/I_{off} between 10^9 and 10^{10} for 1L MoS_2 FETs in both the top-gate and back-gate configuration.

Table 1 | Comparison of FETs based on monolayer MoS_2 with metal electrodes in direct contact with MoS_2 (no graphene contacts, h-BN tunnelling layers or NC dielectrics)

	SBH	R_c	I_{on}/I_{off}	SS	Requires UHV	Simultaneous imaging/ patterning	Throughput	Resolution
t-SPL	~0 meV	3–6 kΩ μm (back gate) 10 kΩ μm (top gate)	10^{10}	64 mV per decade	No	Yes	10^5 μm^2 h^{-1}	~10 nm
EBL in literature	38 meV (ref. [36]) 55 meV (ref. [35]) 60 meV (ref. [34]) 110 meV (ref. [33])	3 kΩ μm (UHV) (ref. [58]) 7 kΩ μm (ref. [33])	10^7 (ref. [33]) 10^8 (ref. [4])	74 mV per decade (ref. [4]) 178 mV per decade (ref. [64]) 410 mV per decade (ref. [42])	Yes	No	10^5 μm^2 h^{-1}	~10 nm

In Fig. 5c we report the comparison of the performance of t-SPL devices with the best results in the literature concerning the on/off ratio I_{on}/I_{off}, subthreshold swing (SS) and normalized on-current I_{on} (refs. [4,58,60,62,64,65]). We remark that, here, the comparison is extended to multilayer MoS_2 FETs, which are usually characterized by higher on-currents, and to different strategies for improving the FETs performances, such as the use of negative capacitor gate dielectrics. Moreover, the comparison between FETs fabricated by t-SPL and the best EBL results in the literature[4,33–36,42,58,64] for only direct metal contacts on monolayer MoS_2 is summarized, as shown in Table 1. Finally, as an additional test, the back-gate t-SPL devices based on exfoliated 1L MoS_2 is compared with equivalent EBL devices fabricated in our laboratory, with the same contact metals and device geometry. The obtained results confirm the superior performance of the t-SPL devices and are shown in Supplementary Section 9 (Supplementary Fig. 16–18) and Supplementary Table 1. It is noteworthy that the results of this work, obtained by simple metal patterning via t-SPL, show remarkably better performances in terms of combination of the 10^9 to 10^{10} on/off ratio, nearly ideal subthreshold swing of 64 mV, high normalized I_{on} and zero hysteresis. We anticipate that, by combining the t-SPL metal patterning approach with the aforementioned methods, even higher performance MoS_2 FETs can be envisaged.

To demonstrate the generality of the approach also for other 2D semiconductors, back-gated FETs are fabricated via t-SPL on monolayer WSe_2 exfoliated on Si/SiO_2 substrates. The results are reported in Supplementary Fig. 24. Along with these results we also include Supplementary Table 3 where we compare the performances of a back-gated monolayer WSe_2 FET fabricated by t-SPL with data from the literature on FETs based on the same type of material. In particular, for a meaningful comparison, we compare the previously published transfer characteristics performances of n-FET WSe_2 with our data, by reporting both maximum on current and on/off ratio for monolayer and few-layer (< 5) n-FET WSe_2. As clear from Supplementary Table 3, t-SPL can produce FETs with transfer characteristics having the highest on/off ratio and on current among n-type monolayer or few-layer WSe_2 FETs.

Conclusions

We have shown that t-SPL can be used to fabricate high-quality metal contacts on 2D materials with high reproducibility. Electron beam lithography is typically used for metal nanopatterning when high resolution is needed, but the need for UHV and high-energy electrons limits its wider application. Compared to EBL, our approach offers advantages in terms of device performance and capabilities, including not requiring a vacuum, even for 14-nm-length channels, and simultaneous in situ imaging and patterning with an overlay accuracy better than 5 nm. We have used our t-SPL-based scheme to fabricate top-gated and back-gated FETs on 1L MoS_2 and 1 L WSe_2. By eliminating resist contamination, as well as damage from either electrons or photons, our MoS_2 FETs show linear I–V curves even at low temperatures, record low Schottky barrier heights (~0 mV), record high on/off ratios (10^9–10^{10}) and exceptionally low subthreshold swing (64 mV per decade). t-SPL is compatible with standard etching procedures and could potentially be pushed to single-digit-nm spatial resolution, and, by multiplexing with thermal nanoprobe arrays[30,66], to higher throughput. The approach could thus lead to low-cost, no-vacuum, one-step industrial metal nanomanufacturing.

Methods

Materials. We use monolayer exfoliated MoS_2 flakes (from bulk MoS_2, SPI) and monolayer monocrystalline CVD MoS_2 triangular structures (from 2Dlayer) on highly doped silicon substrates covered with 285 nm of thermally grown silicon oxide. Exfoliated MoS_2 samples are dipped for 2 h in acetone to remove tape residuals, and then rinsed with isopropyl alcohol (IPrOH) before starting the fabrication. For the top-gated FETs, we use as top gate dielectric h-BN flakes mechanically exfoliated on SiO_2/Si, which are annealed (300 °C, 2h) and then transferred onto the target 1L MoS_2 FET (back-gated) with a dry stamp-assisted pick-and-place process. The thickness of the h-BN flake for the FET shown in Fig. 2 is 15 nm, as measured by AFM. The t-SPL patterning scheme is then used to image and pattern in situ the top gate without markers.

Device fabrication by t-SPL. All MoS_2 samples are kept in contact with HMDS vapours for 90 s to promote polymer adhesion. First, a solution of pure PMGI (polymethylglutarimide, Sigma) is spin-coated on the samples surface (2,000 r.p.m., 35 s) followed by a quick baking. For device fabrication this step is repeated three times; then, a PPA (polyphthalaldehyde, Sigma) solution (1.3 wt % in anisole) is spin-coated on PMGI (conditions: 2,000 r.p.m. at 500 r.p.m. s^{-1} for 4 s and then 3,000 r.p.m. at 500 r.p.m. s^{-1} for 35 s) followed by a quick baking. With these conditions, a 20-nm-thick PPA film on top of a 210-nm-thick PMGI film is deposited on the sample surface. Patterning of PPA is performed using a commercial NanoFrazor t-SPL tool (SwissLitho AG), which uses hot probes to locally heat a resist[37] with nanoscopic resolution (more details are reported in the Supplementary Information). During the lithographic writing the tip is heated to reach about 200 °C at the PPA surface. Finite-element simulations of the heat flow from the hot tip through PMGI, after all PPA is evaporated, have been performed with the FEniCS platform to evaluate the heat temperature underneath PMGI on the MoS_2 layer, as reported in Supplementary Section 2 and Supplementary Fig. 3. Patterns are performed with a pixel time in the range 30–70 μs. For patterning large pads (size: 100 x 100 μm^2) the overlay and stitching routine is used[66]. For the chemical etching of PMGI after patterning, samples are immersed in a solution of TMAH in deionized water (tetramethylammonium hydroxide AZ726 MIF, MicroChemicals) (0.17 mol l^{-1}) for 400 s, then rinsed with deionized water (30 s) and IPrOH (30 s), and finally dried with N_2. Metal deposition is performed using an AJA Orion 8E e-beam evaporator (pressure ~ 10^{-8} torr, evaporation rate: 1 Å s^{-1}). Finally, metal/resist lift-off is performed by dipping samples in Remover PG (MicroChem) for a few hours, followed by rinsing (IPrOH) and drying (N_2). The back-gate t-SPL FETs presented in this paper have been fabricated using different metals: Pd/Au (10 nm/10 nm), Pd/Au (10 nm/20 nm), Al/Au (10 nm/10 nm) and Pt/Au (10 nm/10 nm) for exfoliated MoS_2 (see Figs. 3, 4, Supplementary Figs. 15–18, 21 and Supplementary Table 1) and Cr/Au for CVD MoS_2 (10 nm/20 nm) (see Supplementary Figs. 19,20). Cr/Au (10 nm/20 nm) is used as metal for the top-gate.

Electrical measurements. Electrical characterization of CVD monolayer MoS_2 is carried out using a parameter analyser and a home-built shielded probe station working in vacuum (10^{-4} torr) with micro-manipulated probes. A 7651 Agilent DC source, a Keithley KE2400 sourcemeter and a 34401A Agilent Multimeter are used, respectively, to apply the gate voltage, the source–drain voltage and to read the drain current. Electrical measurements on exfoliated flakes are carried out following the standard routines for FETs by using either an Agilent 4155C semiconductor parameter analyser in a vacuum probe station at a pressure of 10^{-3} torr, or a Keithley 4200-scs semiconductor characterization system in a Lakeshore probe station at a pressure of 10^{-5} torr. To avoid capacitive coupling between the back and top gates during the measurements of the top-gate devices, the back gate is either grounded or biased.

Sample characterization. Tapping-mode AFM images are collected in different areas of CVD monolayer MoS_2 flakes after EBL and t-SPL fabrication and resist removal, to systematically investigate the cleanliness of the samples and the presence of residuals from fabrication. The results are shown in Supplementary Section 3 and in Supplementary Figs. 4–6. Tapping-mode AFM images are also collected to verify the monolayer nature of the CVD and exfoliated MoS_2 samples used in this work (see Supplementary Fig. 11), and before and after electrodes deposition in t-SPL fabrication to assess the resolution of the t-SPL technique (see Supplementary Fig. 2). Images are collected using a Multimode 8 AFM (Bruker) and PPP-NCH tips (Nanosensors).

Raman spectroscopy is used to establish the monolayer nature of all the exfoliated and CVD MoS_2 flakes used for t-SPL fabrication (see Supplementary Section 6 and Supplementary Fig. 10) and to investigate the contact and channel region for the t-SPL and EBL fabrication (see Supplementary Figs. 8,9). Raman spectra are collected using a Horiba LabRAM HR800 system coupled with an Olympus BX41 inverted optical microscope, and using a laser source with an excitation wavelength of 532 nm. The laser power is adjusted to avoid sample damage, or any sample modification, as observed by optical microscopy. Spectra are acquired in the range 100–900 cm^{-1} with a 1 s exposure time and as an average of 10 different measurements. The peak at 520.7 cm^{-1} from the silicon substrate is used as a reference for the position of the MoS_2 peaks. Reported spectra in Supplementary Figs. 8–10 are normalized with respect to the MoS_2 A_{1g} peak.

XPS spectroscopy is used to investigate the residuals from EBL fabrication, as reported in Supplementary Section 4 and Supplementary Fig. 7. XPS measurements are performed with a Physical Electronics VersaProbe II system (UHV pressure $< 10^{-6}$ Pa) using Al Kα radiation (1,486.6 eV). The sample is mounted on a steel sample holder and grounded. The following conditions are used: analyser acceptance angle = 20°; take-off angle = 45°; beam size = 200 μm; pass energy = 11.75 eV (C1s); integration time = 200 ms per step; step size = 0.05 eV per step.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

X.Z., A.C., E.A. and X.L. patterned the metal electrodes by t-SPL. A.S.M.A. performed the electronic measurements on the t-SPL FETs. X.Z., E.A., X.L., A.S.M.A., D.S. and E.R. designed the electronic experiments and analysed the data on the t-SPL FETs. G.A. and X.L. fabricated and measured the EBL FETs. X.Z., M.S. and E.R. developed the two-polymer stack t-SPL method. W.J.Y. and J.H. designed and analysed the EBL data. T.T. and K.W. provided the h-BN samples. C.A. analysed the XPS data. A.C. and A.K. provided the WSe_2 samples and contributed to the corresponding data analysis. B.S.L. and M.L. deposited Pd electrodes on t-SPL FETs. E.R. conceived and analysed all the experiments on t-SPL FETs. X.Z., A.C., E.A., G.A., J.H., D.S. and E.R. contributed to writing the article.

Competing interests

The authors declare no competing interests.

Additional information

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