# Short-Term Relaxation in HfO<sub>x</sub>/CeO<sub>x</sub> Resistive Random Access Memory With Selector

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Abstract—This letter illustrates short-term relaxation in CeO<sub>x</sub>-based resistive random access memory (RRAM) devices. Our results suggest that the noise of the serial selector device can impact the short-term relaxation, reduce the operating window of the RRAM, and increase the read error. Our findings indicate that the application of longer initial forming pulses can mitigate the short-term relaxation issue.

*Index Terms*—RRAM, reliability, programming algorithms, high- $\kappa$  dielectrics.

#### I. INTRODUCTION

ESISTIVERandom Access Memory (RRAM) K technology has potentials for conventional high-density storage and emerging neuromorphic computation [1]. RRAM devices made of binary transition metal oxides (TMOs) appear to be most promising owing to their low switching energy and compatibility with contemporary foundry processes. Many materials have been explored for making RRAM devices that exhibit good device characteristics (e.g.  $CeO_x$  [2],  $HfO_x$  [3],  $TaO_x$  [4], and  $TiO_x$  [5]). Despite significant progress, there are still key fundamental questions that impedes the transformation of RRAMs into a full-fledged device technology. Among those, there is short-term program instability. This phenomenon relates to the decay of the resistance state after applying a programming pulse. The short-term relaxation occurs at a timescale on the order of  $\mu$ s to a fraction of second. As such, this phenomenon is different from the retention issues in long-term reliability. This problem is particularly important for the implementation artificial neural networks (ANN) because in these implementations the output is fed back in short time intervals (e.g. recursive neural network (RNN)) [6].

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10.0m Current density (A/cm²) ,ª 00 00 (b) (a) NL ratio > 10<sup>5</sup> Ti Current (A) 20nm 0.0 -2 2 3 -3 -2 -1 0 2 0 Voltage (V) Voltage (V)

Fig. 1. (a) Semilog current density of an MSM diode. The MSM selector has an NL ratio over  $10^5$ . (b) The asymmetry of the current amplitude at the positive and negative polarities is evident from the linear I-V characteristic. The inset shows the side-view transmission electron microscope (TEM) image of a 1S1R device.

Fantini *et al.* [7] has reported the pioneering statistical study of this problem in  $HfO_x$ -based RRAMs. Here, we systematically examine the short-term program instability and its ensuing reliability issues in our CeO<sub>x</sub> bilayer RRAM with and without a selector device. Our selector device is a metal-semiconductor-metal (MSM) diode, which provides high non-linearity (NL) ratio and a current density in excess of (1MA/cm<sup>2</sup>). The RRAM device is made of CeO<sub>x</sub> filament and a sub-stoichiometric HfO<sub>x</sub> oxygen scavenging layer [8].

#### II. DEVICE FABRICATION AND EXPERIMENT

In our process, the MSM selector diode and the RRAM device are stacked vertically. 1S1R devices were fabricated on Si (111) substrates capped with thermal silicon dioxide. The bottom electrode (BE) was formed by electron beam (e-beam) evaporation of 80 nm Ti. Then, an amorphous silicon (a-Si) layer (about 15 nm) was deposited above the BE by PECVD at 250°C. The growth parameters were optimized to produce nanoscale hydrogenated a-Si thin film, similar to the report by Moravej et al. [9]. The intermediate electrode (IE) was formed by e-beam evaporation of 30 nm Ti, followed by the reactive evaporation of  $CeO_x$  in oxygen plasma at 0.2 mTorr. The  $HfO_x$  layer was formed by plasma-assisted atomic layer deposition on the top of the  $CeO_x$  layer [8]. The I-V characteristics of the MSM selector is shown in Fig. 1. The asymmetric current in Fig. 1(b) is possibly due to the different interfacial properties of the front and the bottoms interfaces. For short-term relaxation studies, we focused on Incremental Step Pulse Programming (ISPP) [10], [11]

0741-3106 © 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information. because it provides better endurance compared with the open-loop single pulse programming scheme. In our test setup, we used 200 ns long write and read pulses. The read pulses were applied for up to 1 s after each successful SET or RESET. Continuous read pulses provide real-time

read pulses were applied for up to 1 s after each successful SET or RESET. Continuous read pulses provide real-time information about the fluctuation and the relaxation of the stored bit in the RRAM device under test, which is important for understanding the short-term relaxation phenomenon.

## **III. RESULTS AND DISCUSSION**

To examine the effect of the MSM selector on the short-term relaxation, we compared the post-programming read current distributions of two structures, namely a one-RRAM (1R) structure and a one-selector-one-RRAM (1S1R) structure. All experiments were performed on virgin devices to eliminate the possible effect of device history on the short-term relaxation behavior. These devices were preconditioned by switching 50 cycles using ISPP while skipping the continuous read step. The continuous read steps were disabled during device preconditioning to avoid possible degradation of the RRAM operating window. After preconditioning, the devices were switched once with ISPP, followed by a continuous read step that lasts up to 1s. This test procedure enabled us to distinguish the short-term relaxation from the long-term degradation induced by repetitive read cycles. The test results of a 1R device is shown in Fig. 2(a), revealing the presence of two distinct current states at the low resistance state (LRS) and a continuum of random states at the high resistance state (HRS). Fig. 2(b) shows the distribution of the read current for a 1S1R structure. Compared with the 1R structure, the 1S1R structure demonstrates larger spread in the read currents at both the HRS and the LRS. These results indicate higher degradation of the operating window of the 1S1R structures, which can consequently lead to the increase of the raw read error rate. The degradation of the operating window is particularly important for devices with small operating current [12]. Increasing the resistance difference between the HRS and the LRS is a potential solution for mitigating this problem. However, we observed that increasing the operating window of our bilayer CeO<sub>x</sub>-based RRAMs degrades the endurance properties of the device. We will discuss this issue in more details later.

The continuous read procedure affords higher time resolution, which is important for studying the short-term relaxation issue. In Figs. 3(a) and (b), with continuous read, we were able to measure the random telegraph noise (RTN) of the selector devices. The RTN in an MSM device primarily originates from the charge trapping at the interfaces between the metal electrodes and the semiconductor [13]. The data in Fig. 3 illustrates the dependence of the RTN amplitude on the current amplitude. Specifically, the fluctuations of the current noise in HRS is noticeably larger than the LRS. This noise characteristic of the selector will, therefore, impact the short-term relaxation behavior of the 1S1R device during HRS and LRS differently. In Fig. 4 we compare the cumulative distribution function (CDF) plots for (a) a 1S1R structure, (b) a 1R device with short (100ns) forming pulses, and (c) a 1R



Fig. 2. Distribution of HRS and LRS read currents for (a) 1R and (b) 1S1R structures.



Fig. 3. RTN noise of an MSM selector measured at (a)  $12.8\mu$ A, and (b)  $1\mu$ A. The fluctuations of the the current noise is noticeably larger in HRS. The max noise level is 2% higher than the mean in LRS, while the max noise level is 35% higher than the mean in HRS.

device with  $(5\mu s)$  long forming pulses. To clearly illustrate the change in the operating window of these structures, the HRS curves were plotted in the form of 1 - p(x). Further, the probit unit [14] was used in Fig. 4 because it linearizes a lognormallike distribution. The measurement results reveal that the tail bits of the 1S1R structure in Fig. 4(a) exhibit a narrower gap than the 1R device in Fig. 4(b). We attribute this to noticeable fluctuations of the MSM current noise in HRS. The noise of the voltage drop across the RRAM device in HRS, thereby increasing to the overall inherent noise of the 1S1R structure. Since the implementation of the 1S1R structures are pursued for most practical applications, it is important to consider their short-term relaxation behavior when designing algorithms for ANN applications.

Next, we examined the effect of the forming pulse duration on the short-term relaxation behavior of the 1R structures, shown in Fig. 4(b) and (c). The RRAM device in Fig. 4(b) was formed using a 100ns long pulse, while the device in Fig. 4(c) was formed using a  $5\mu$ s long pulse. The comparison of the test results in Fig. 4 clearly illustrates the improvement of the tail bits distribution for the RRAM device formed using the  $5\mu$ s long forming pulse. This observation can be explained using the previously proposed model based on the



Fig. 4. CDF plots using probit units for (a) 1S1R, (b) 1R with 100ns forming pulse, and (c) 1R with  $5\mu$ s forming pulse. The arrows labeled "time" in (a) indicate the temporal progress of the experiment. The horizontal arrows indicate the gap between tail bits of the HRS and the LRS. Probit of the HRS curves are plotted in a decreasing fashion versus current, while the LRS curves are plotted in an increasing fashion versus current. The read pulse voltage in (a) is 1.7V because of voltage drop at selector device.



Fig. 5. Effect of the operating window and the forming pulse duration on the long-term reliability endurance of RRAMs. Devices were subject to ISPP with a read pulse width of 200ns.

diffusive dynamics [15]–[17]. The thermodynamic stabilization is the basis for this model, in which the charged defects are assumed to relax to a thermal equilibrium state after biasing the RRAM cell. The use of longer forming pulses is expected to give rise to the formation of more stable states for charge defects, thereby mitigating the short-term relaxation issue. Furthermore, we compared the short-term relaxation behavior of the bilayer CeO<sub>x</sub>/HfO<sub>x</sub> device in Fig. 4(b) with the HfO<sub>x</sub> device in [7], indicating faster relaxation of the bilayer device. We attribute this observation to the increase of the diffusion pre-factors at the interface of the CeO<sub>x</sub> and the HfO<sub>x</sub>, confirmed by the hybrid density functional theory and molecular dynamics (DFT-MD) simulations [18].

Lastly, we investigated the effect of the forming pulse duration on the long-term endurance of the device. Fig. 5 shows the comparison of the endurance behavior for 1R devices with 100ns forming pulse and  $5\mu$ s forming pulse. In addition, we examined the effect of the operating window on the endurance characteristics of 1R devices, shown in Fig. 5. The black square curve in Fig. 5 represents a 1R

device operated at typical on-off ratio, which is LRS 20 k $\Omega$ , HRS 200 k $\Omega$ . The blue diamond curve in Fig. 5 represents a 1R device with intentionally enlarged on-off ratio by setting switching threshold in ISPP, resulting in LRS of about 1 k $\Omega$ and HRS of about 1 M $\Omega$ . A 100ns pulse was used for forming the 1S1R structures. As pointed out earlier, increasing the operating window can mitigate the short-term relaxation issue. However, our results indicate the degradation of the endurance characteristics of the bilayer RRAM device upon increasing the operating window. Our findings suggest that the use of longer forming pulses might be a more favorable solution because it does not compromise the device endurance while mitigating the short-term relaxation problem.

# **IV. CONCLUSION**

In this work, we examined the short-term program instability of the 1S1R and the 1R structures using  $CeO_x$ -based bilayer RRAM devices. Our results indicate that the 1S1R structures are more susceptible to the short-term relaxation. Furthermore, we found out that increasing the forming pulse width can alleviate the short-term relaxation without compromising the long-term endurance.

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#### REFERENCES

- D. Kuzum, R. G. D. Jeyasingh, and H.-S. P. Wong, "Energy efficient programming of nanoelectronic synaptic devices for large-scale implementation of associative and temporal sequence learning," in *IEDM Tech. Dig.*, Dec. 2011, pp. 3–30, doi: 10.1109/IEDM.2011.6131643.
- [2] C.-C. Hsieh, A. Roy, A. Rai, Y.-F. Chang, and S. K. Banerjee, "Characteristics and mechanism study of cerium oxide based random access memories," *Appl. Phys. Lett.*, vol. 106, no. 17, p. 173108, Apr. 2015, doi: 10.1063/1.4919442.
- [3] Y. S. Chen, H. Y. Lee, P. S. Chen, P. Y. Gu, C. W. Chen, W. P. Lin, W. H. Liu, Y. Y. Hsu, S. S. Sheu, P. C. Chiang, W. S. Chen, F. T. Chen, C. H. Lien, and M.-J. Tsai, "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424411.

- [4] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnol.*, vol. 3, no. 7, pp. 429–433, Jun. 2008, doi: 10.1038/nnano.2008.160.
- [5] C. H. Cheng, P. C. Chen, Y. H. Wu, F. S. Yeh, and A. Chin, "Longendurance nanocrystal TiO<sub>2</sub> resistive memory using a TaON buffer layer," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1749–1751, Dec. 2011, doi: 10.1109/LED.2011.2168939.
- [6] S. B. Eryilmaz, D. Kuzum, S. Yu, and H.-S. P. Wong, "Device and system level design considerations for analog-non-volatile-memory based neuromorphic architectures," in *IEDM Tech. Dig.*, Dec. 2015, pp. 1–4, doi: 10.1109/IEDM.2015.7409622.
- [7] A. Fantini, G. Gorine, R. Degraeve, L. Goux, C. Y. Chen, A. Redolfi, S. Clima, A. Cabrini, G. Torelli, and M. Jurczak, "Intrinsic program instability in HfO<sub>2</sub> RRAM and consequences on program algorithms," in *IEDM Tech. Dig.*, Dec. 2015, pp. 5–7, doi: 10.1109/IEDM. 2015.7409648.
- [8] C.-C. Hsieh, A. Roy, Y.-F. Chang, D. Shahrjerdi, and S. K. Banerjee, "A sub-1-volt analog metal oxide memristive-based synaptic device with large conductance change for energy-efficient spike-based computing systems," *Appl. Phys. Lett.*, vol. 109, no. 22, p. 223501, Nov. 2016, doi: 10.1063/1.4971188.
- [9] M. Moravej, S. E. Babayan, G. R. Nowling, X. Yang, and R. F. Hicks, "Plasma enhanced chemical vapour deposition of hydrogenated amorphous silicon at atmospheric pressure," *Plasma Sour. Sci. Technol.*, vol. 13, no. 1, p. 8, Nov. 2003, doi: 10.1088/0963-0252/13/1/002.
- [10] S. Subhechha, B. Govoreanu, Y. Chen, S. Clima, K. D. Meyer, J. V. Houdt, and M. Jurczak, "Extensive reliability investigation of a-VMCO nonfilamentary RRAM: Relaxation, retention and key differences to filamentary switching," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2016, pp. 6C-2-1–6C-2-5, doi: 10.1109/IRPS.2016. 7574568.

- [11] Y. Y. Chen, R. Roelofs, A. Redolfi, R. Degraeve, D. Crotti, A. Fantini, S. Clima, B. Govoreanu, M. Komura, L. Goux, L. Zhang, A. Belmonte, Q. Xie, J. Maes, G. Pourtois, and M. Jurczak, "Tailoring switching and endurance/retention reliability characteristics of HfO2/Hf RRAM with Ti, Al, Si dopants," in *Symp. VLSI Technol. (VLSI-Technology), Dig. Tech. Papers*, Jun. 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894403.
- [12] J. Zhou, F. Cai, Q. Wang, B. Chen, S. Gaba, and W. D. Lu, "Very low-programming-current RRAM with self-rectifying characteristics," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 404–407, Apr. 2016, doi: 10.1109/LED.2016.2530942.
- [13] L. K. J. Vandamme, "Noise as a diagnostic tool for quality and reliability of electronic devices," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2176–2187, Nov. 1994, doi: 10.1109/16.333839.
- [14] C. I. Bliss, "The method of probits," *Science*, vol. 79, no. 2037, pp. 38–39, Jan. 1934, doi: 10.1126/science.79.2037.38.
- [15] S. Clima, Y. Y. Chen, A. Fantini, L. Goux, R. Degraeve, B. Govoreanu, G. Pourtois, and M. Jurczak, "Intrinsic tailing of resistive states distributions in amorphous Hf<sub>x</sub> and TaO<sub>x</sub> based resistive random access memories," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 769–771, Aug. 2015, doi: 10.1109/LED.2015.2448731.
- [16] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia, and J. J. Yang, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nature Mater.*, vol. 16, no. 1, pp. 101–108, 2017, doi: 10.1038/nmat4756.
- [17] A. Chen and M.-R. Lin, "Reset switching probability of resistive switching devices," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 590–592, May 2011, doi: 10.1109/LED.2011.2109933.
- [18] A. A. Bhatti, C.-C. Hsieh, A. Roy, L. F. Register, and S. K. Banerjee, "First-principles simulation of oxygen vacancy migration in HfO<sub>x</sub>, CeO<sub>x</sub>, and at their interfaces for applications in resistive random-access memories," *J. Comput. Electron.*, vol. 15, no. 3, pp. 741–748, Jun. 2016, doi: 10.1007/s10825-016-0847-9.