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Solid-State Electronics 48 (2004) 1953–1957
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

A lateral structure for low-cost fabrication of COOLMOS^{TM}

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Received 10 December 2003; accepted 15 March 2004

Abstract

A lateral structure for low-cost fabrication of COOLMOS^{TM} on SOI wafers is proposed and the feasibility of the fabrication steps is verified by simulation in GENESISe environment. The requirement of multiple epitaxy and implantation steps for the growth of voltage-sustaining pillars in conventional vertical COOLMOS^{TM} is automatically eliminated in the proposed method through the use of the lateral structure fabricated on SOI wafer. DESSIS simulations confirm the functionality of the proposed device, including the so-called quasi-saturation effect. In addition to the successful transistor behaviour of the lateral COOLMOS^{TM}, the proposed fabrication method has the advantage of low-cost processing steps in comparison with the conventional vertical fabrication approach, and also offers compatibility for on-chip integration with CMOS control circuitry.

Keywords: COOLMOS^{TM}; SOI; On-chip realization; Power transistor

1. Introduction

In order to function properly as a switch, power MOSFETs should meet two important requirements: having minimal resistance when the device is in the on-state and sustaining high reverse voltage when the device is off. The former needs high doping levels, while the latter calls for lower doping concentrations. So, in conventional power MOSFETs there should be a compromise between these two requirements. The drift pillar is therefore chosen a lightly doped thick strip of silicon to promote its voltage sustaining capability during the off-state, only to the extent that it maintains a reasonable conductance in the on-state operation regime. This means that the on-state conductivity and the off-state voltage sustaining capability cannot be improved independently. Recently, COOLMOS^{TM} has been proposed as a solution to this problem [1–3].

As a new generation of power MOSFETs, COOLMOS^{TM} transistors have recently found an especial scope in power electronics. After the conceptual development of the relative voltage sustaining structure [4–6], COOLMOS^{TM} has been experimentally realized to break the limit line of silicon in high voltage applications [7]. The main building block of these devices is a combination of parallel n^- and p^- strips, called a superjunction, as shown in Fig. 1(a), whereas the conventional voltage-sustaining block is a low-doped drift region given in Fig. 1(b). It is the unique capability of the superjunction that guarantees efficient voltage sustaining, when the transistor is off. In this state, the voltage applied to the drain contact appears as a reverse bias between the p^- and n^- strips. Subsequently, the drift pillar of the superjunction becomes fully depleted for a comparatively small value of the applied voltage.

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0038-1101/$ - see front matter
doi:10.1016/j.sse.2004.05.041

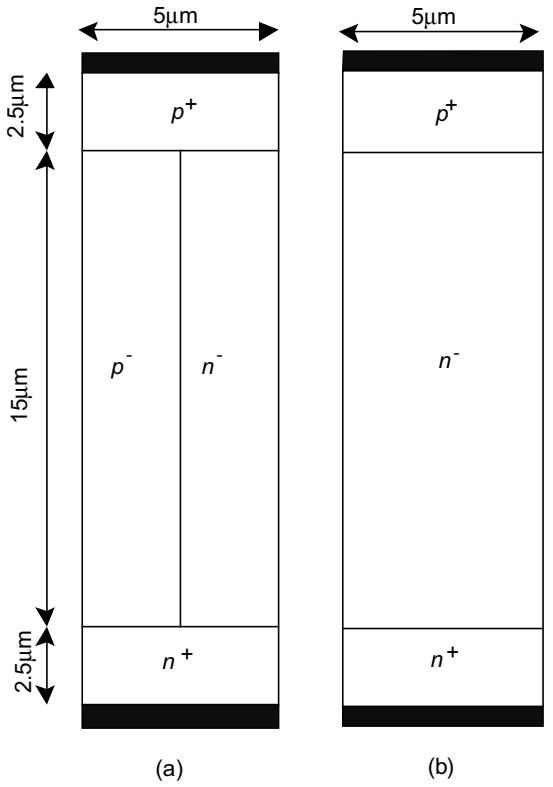

Fig. 1. (a) The superjunction and (b) conventional voltage sustaining structure.

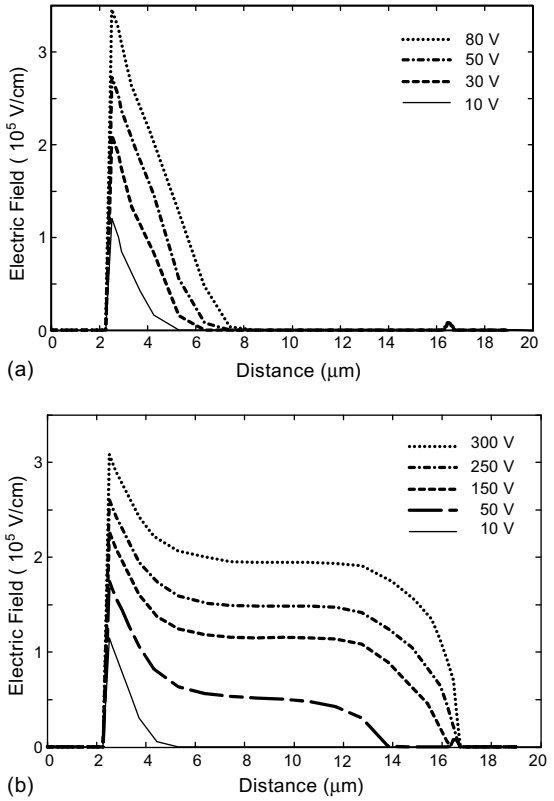

Fig. 2. The electric field profile versus distance for (a) a conventional voltage-sustaining structure, and (b) the superjunction structure.

As a result, the voltage sustaining behaviour of the n^- strip is almost equal to that of an intrinsic layer. This privilege of the superjunction leads to an optimum doping concentration for the drift pillar to optimally satisfy the on and off-state requirements.

In order to clarify how the superjunction structure sustains higher breakdown voltages in comparison with the conventional voltage-sustaining block, for the same values of doping concentration of the n^- drift pillar, consider the simplified structure of a superjunction and a conventional sustaining voltage block shown in Fig. 1. Simulations have been performed for the case that the p^+ and n^+ contacts are heavily doped ($N_A = N_D = 10^{20}$ cm^{-3}), and the n^- and p^- strips and the n^- layer of the conventional voltage-sustaining block are lightly doped ($N_A = N_D = 10^{16}$ cm^{-3}). The p^+ contact is grounded and a positive voltage is applied to the n^+ contact. The superjunction structure was found to break down at 300 V, while the conventional structure could only sustain 80 V. Variation of the electric field versus distance is plotted in Fig. 2(a) for the conventional structure. For the superjunction, the profile of the electric field is plotted along the outer edge of the n^- strip, as depicted in Fig. 2(b). It is observed that the area under the electric field profile is considerably higher for the superjunction structure for high values of reverse bias. This area is the indication of the breakdown voltage for the maximum applied reverse bias for which the critical electric field occurs throughout the depletion region. Thus, it is verified that superjunction presents superior voltage sustaining capabilities in comparison with the conventional structure.

Properties of the so-called superjunction as well as modeling and optimization of the complete relevant device structure has been pursued in previous works [8,9]. In this contribution, we are concerned with the fabrication process. As may be concluded from Fig. 1(a), formation of columnar n^- and p^- strips is an expensive process, since these regions should be formed by multiple depositions of epitaxial layers and subsequent implantation steps. For instance, the use of masked boron and phosphorous implantations on undoped epitaxy on a highly doped n^+ substrate has been reported [9]. A diffusion process is subsequently employed to form vertically coherent n^- and p^- columns. It is apparent that with columns as long as 20 μm, more than 10 steps of epitaxy and implantation might be needed, which translates into an expensive fabrication process.

2. Proposed structure

We hereby propose a lateral structure and a fabrication approach in which only one epitaxy step is involved. The only extra cost would be due to the initial SOI substrates, which is negligible in comparison with the cost reduction resulted by eliminating the frequent epitaxy steps. The proposed structure is schematically given in Fig. 3(a), where the conventional vertical structure is also given for comparison in Fig. 3(b).

2.1. Process simulation

We have simulated the fabrication process of the proposed structure with DIOS simulator in GENESISe [10]. An n-type SOI wafer with a thickness of 2.5 μm and a concentration of 10^{16} cm^{-3} is chosen as the initial substrate. The n^- upper layer of the SOI wafer serves as the n^- drift pillar. The 2.5 μm p^- strip is formed by epitaxial growth and with the same doping concentration in boron ambient. The p-well is formed by oxide-masked multiple implantations of boron with maximum energy of 250 keV and dose of 10^{13} cm^{-2}, followed by a 300-min annealing for drive-in. The needed space for the drain contact is grooved by RIE and filled with CVD-deposited highly doped PSG via standard lithography and CMP steps. The gate space is also grooved by RIE and a 180-min thermal oxidation period at 1100 °C forms the 250 nm-thick gate oxide. During this annealing period, the n^+ drain contact is also formed by diffusion of phosphorous from PSG into the Si region. The n^+ source region is formed by resist-masked implantation of arsenic, followed by annealing to activate the dopants. After removing the PSG previously deposited into the drain trench by RIE, CVD tungsten is deposited to form the gate and the drain contacts. After patterning the metal layer and CMP, source contact is deposited and patterned. Adjacent devices may be isolated by removing the dashed regions shown in the figure, via an arbitrary etching process, such as RIE. Fig. 4 demonstrates the final device simulated with DIOS. In this figure the p^- and n^- strips are lightly doped with the concentration of $N_A = N_D = 10^{16}$ cm^{-3} and doping concentration of the drain and source regions is $N_D = 10^{20}$ cm^{-3}.

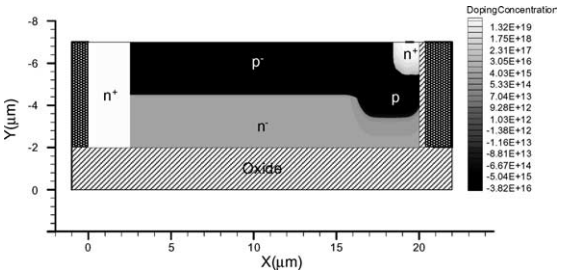

Fig. 4. The proposed lateral structure simulated by DIOS.

2.2. Device simulation

Dessis simulations are employed to characterize the COOLMOS™ structure created by DIOS. The I_D–V_{GS} and I_D–V_{DS} curves are given in Figs. 5 and 6, respectively. When the device is on, electrons flow from the source toward the drain through the channel of the MOS structure and the n^- drift region. Thus, the transistor turns on at the threshold voltage of the intrinsic MOSFET, i.e., when the channel is formed. As it is evident in Fig. 5, increasing the gate voltage raises the

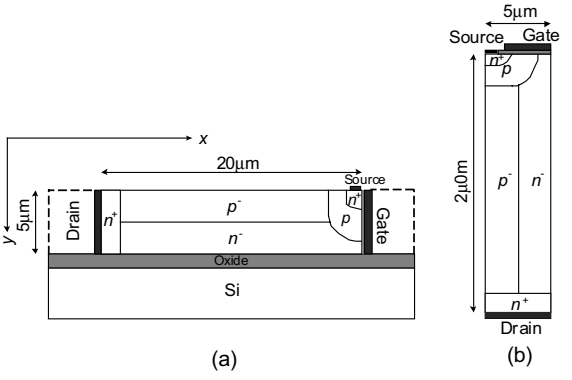

Fig. 3. (a) The proposed lateral and (b) conventional vertical COOLMOS™ structure.

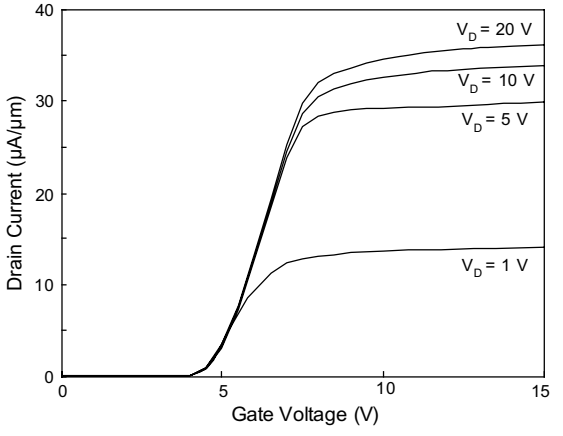

Fig. 5. Transfer characteristics of the simulated lateral COOLMOS™. The drain current saturates when the resistance of the drift region becomes comparable to the channel resistance of the transistor.

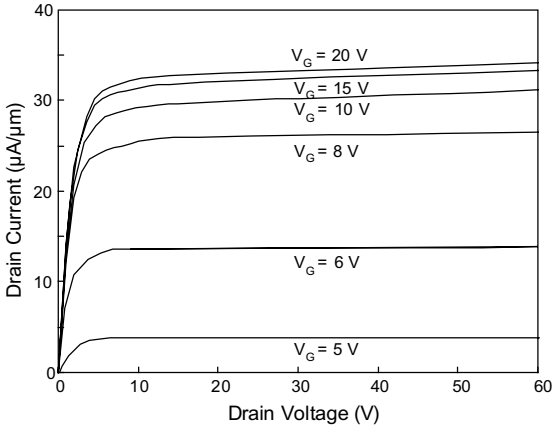

Fig. 6. The output characteristics of the simulated lateral device. The "quasi-saturation" effect is evident in this plot for gate voltages higher than 10 V.

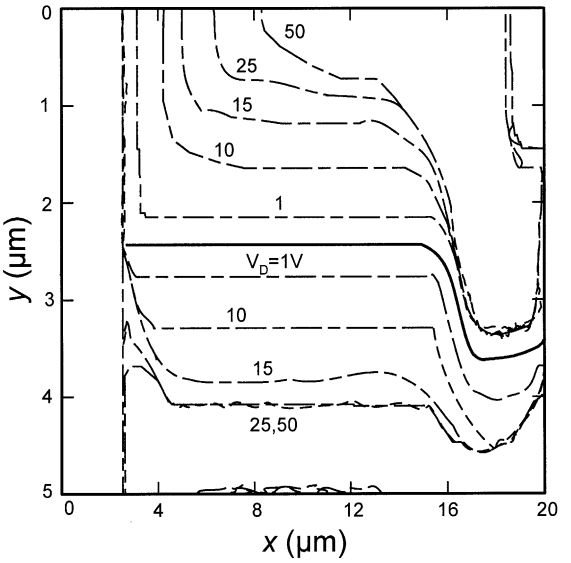

Fig. 7. Contours of the depletion region edge for different values of the drain–source voltage. The metallurgical junction is also shown with solid line.

drain current initially. However, the current starts to saturate when the resistance of the drift region becomes comparable to the channel resistance of the transistor.

In Fig. 6, the output characteristics of the device show two distinguishable behavioural regimes for different applied gate voltages. For small values of the gate voltage, the drain current is fixed on a constant value after the intrinsic MOSFET is saturated. For higher values of V_G the current does not remain constant after saturation, but it shows a slight increase as the drain voltage is increased. This increase is more significant for the gate voltages between 10 and 20 V. The mechanism responsible for this phenomenon which is often referred to as "quasi-saturation" has been elaborately investigated in the previous works [8], where the mobility degradation due to the velocity saturation has been mentioned as the main mechanism accounting for this phenomenon. In the lateral COOLMOS^{TM} transistor, the same mechanism results in the quasi-saturation effect.

The edge of the depletion region during the on-state operation of the proposed structure is depicted in Fig. 7, for various values of the drain–source voltage. The depletion region edge proceeds into the n^- strip when increasing the drain voltage, V_D. Around $V_D = 10$ V, in the vicinity of the p-well, the depletion region edge stops moving ahead into the n^- region. For higher values of V_D, about 20 V, this phenomenon takes place at other parts, in the volume of the n^- drift region. These phenomena are similar to those investigated by Daniel et al. [8]. In this work, it is probed that the neck is the first place experiencing mobility degradation due to the velocity saturation. This effect leads to large values of differential sheet resistance for this region and the additional voltage drop emanated from the increased V_D arises across this region. As V_D becomes greater than 20 V, eventually the entire drift region undergoes the velocity saturation.

The simulated values of the electric field across the line $y = 3.5$ μm is given in Fig. 8 for different drain–source voltages. This figure corroborates the above explanation contending that the additional voltage drop would appear across the mobility degraded region. This figure indicates that the incremental drain voltage causes the electric field profile of the depletion portion of the drift region only to move up with preserving its initial shape.

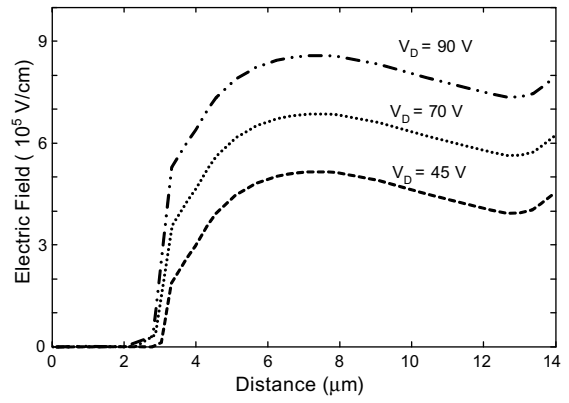

Fig. 8. The simulated electric field along $y = 3.5$ μm for the lateral device.

3. Summary and conclusions

In concise, we have described a simple process for low-cost realization of COOLMOS™ with a lateral structure. The feasibility of the fabrication process steps was verified by simulation in GENESISe. The device simulations confirm the functionality of the proposed structure. Considering the fact that all of the steps in the proposed process flow are compatible with standard CMOS technology, this method puts forth the chance of on-chip integration of the COOLMOS™ power devices with CMOS control circuitry. The elimination of the frequent epitaxy and implantation steps is the other advantage of this structure, which reduces the total cost of the fabrication process considerably.

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