Core-Shell Germanium–Silicon Nanocrystal Floating Gate for Nonvolatile Memory Applications

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***Abstract*—We have fabricated germanium–silicon (Si/HfSiO$_x$) core-shell nanocrystal (NC) structures to work as charge storage nodes in NC Flash memories. This core shell NC structure was made by doing silane annealing treatment before and after Ge NC deposition. This silicon(Si/HfSiO$_x$) shell layer can separate the Ge NC from HfO$_2$ and ambient oxidants in the following process, and reduces low-quality GeO$_x$, HfGeO$_x$ to metallic Ge. Thus, a more robust interface with low trap density between the high-κ dielectric and the NCs was achieved, which helps suppress the charges loss due to trap-assisted tunneling of electrons and results in better device performance.**

***Index Terms*—Germanium–silicon core-shell nanocrystal (NC), high-quality interface, NC Flash memory.**

I. INTRODUCTION

SINCE FIRST described by Tiwari *et al.* [1], Flash memories with nanocrystal (NC) floating gates have attracted considerable attention to improve performance, as have novel programming schemes [2]. NC floating gates are considered to be a promising way to improve memory device performance in terms of faster write/erase speed, better endurance, longer retention time, and further scaling capability. Much work has been done on investigating materials, such as Si [3] and Ni or Au [4], [5] metal NCs, for charge storage nodes in the floating gate. Germanium NCs are an attractive candidate for Flash memory applications for its enhanced carrier confinement compared to Si [6]–[8] and compatibility to today's complementary metal–oxide–semiconductor technology. However, Ge NCs are not thermally stable, and a low-quality trap-filled Ge oxide is easily formed on the NC surface even with a short exposure to ambient or the oxidizing environments. This oxide decreases the Ge dielectric interface quality and degrades the device performance [9], [10].

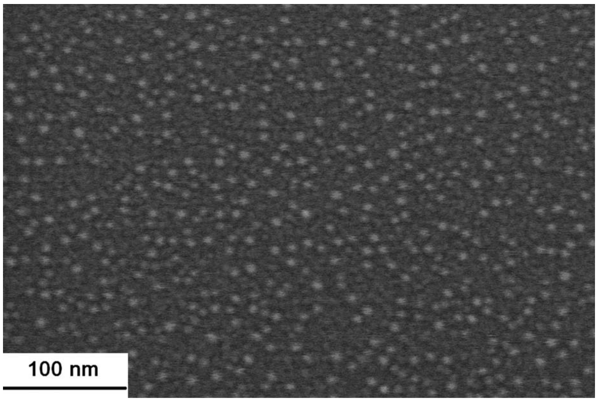

Fig. 1. SEM images of Ge NCs on HfO$_2$ surface.

In this brief, we present a Ge–Si(Si/HfSiO$_x$) core-shell NC structure, where the Ge NCs are encapsulated in an ultrathin Si(Si/HfSiO$_x$) layer to improve electrical properties of the NC–high-κ dielectric interface.

II. DEVICE FABRICATION

Three type MOS capacitor devices were fabricated using different NCs: I) bare Ge NCs, II) Ge NCs only with a Si top capping layer, and III) Ge NCs encapsulated in an ultrathin Si layer. A tunnel oxide about 40 Å hafnia (HfO$_2$) was first grown by atomic layer deposition on a p-type silicon substrate. Ge NCs were then grown by hot-wire chemical vapor deposition (HWCVD) on the HfO$_2$ tunnel oxide (sample I and II) [10]–[12]. These NCs have an average size about 8 nm and density around 3×10^{11} cm^{-2}, as shown in Fig. 1. Sample II was then annealed at a silane partial pressure of 1.9×10^{-5} torr for 45 min at 875 K, leading to the deposition of ~20 Å of Si on the Ge NCs along with hafnium silicate (HfSiO$_x$), as shown in Fig. 2(B). The Si thickness was determined *in situ* by taking the ratio of the Ge 2p X-ray photoelectron spectroscopy (XPS) signal with following equation:

$$t = -\lambda \sin\theta \ln\left(\frac{I}{I_o}\right) \qquad (1)$$

where t is the thickness of the Si layer, λ is the effective attenuation length for a Si overlayer, θ is the angle between the X-ray source and energy analyzer, I is the Ge 2p XPS signal intensity after Si deposition, and I_o is the initial Ge 2p XPS signal intensity. Minimal Si deposition was observed on the HfO$_2$ according to low Hf 4f attenuation, as its attenuation

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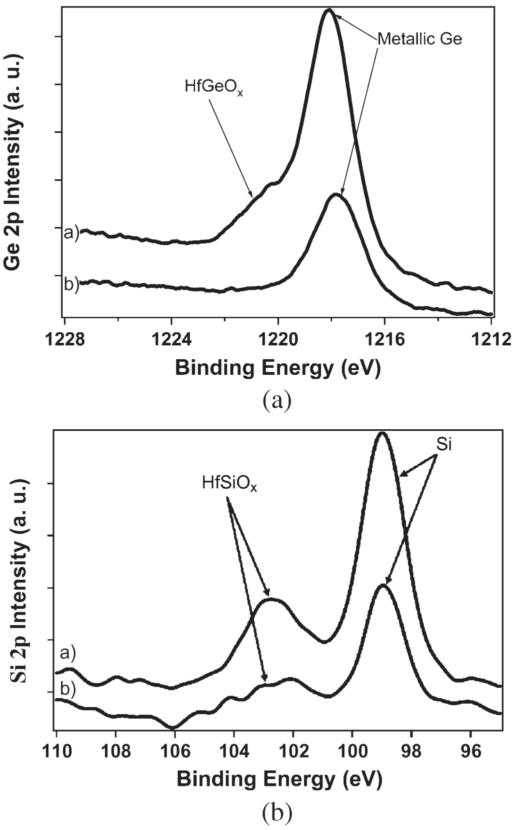

Fig. 2. (A) Ge 2p XP spectra of a) sample I and b) sample II. (B) Si 2p XP spectra for a) sample II and b) sample I.

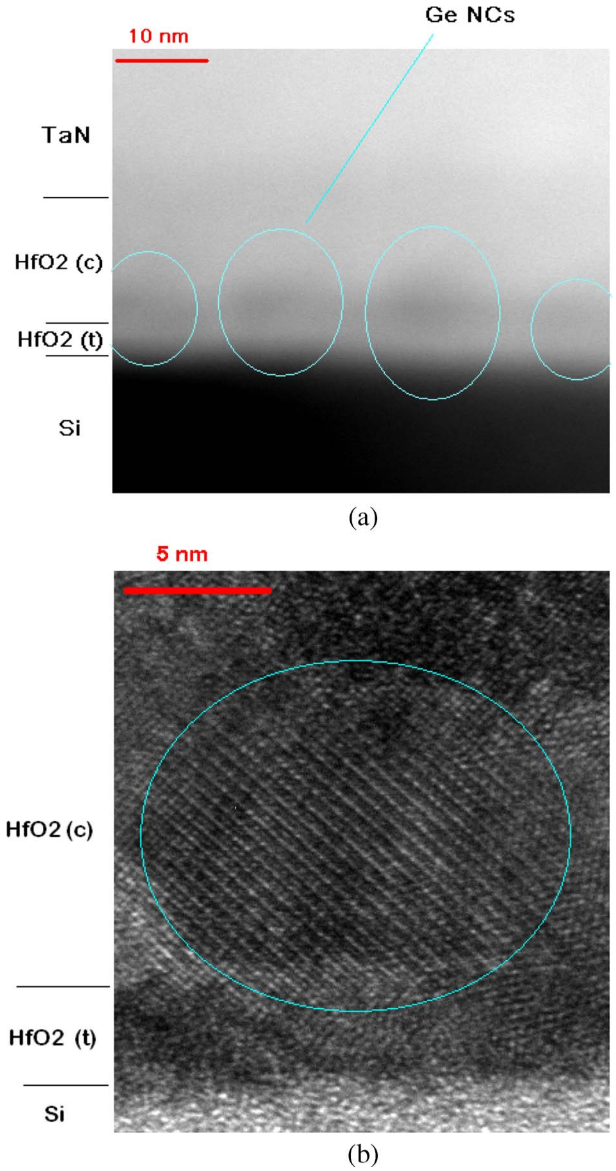

Fig. 3. (A) STEM image of Ge NCs buried in HfO$_2$ matrix. (B) Cross-sectional TEM image of Ge NCs encapsulated in Si/HfSiO$_x$ layer.

was only 0.91 ± 0.13 (spectra not shown). The uncertainty in the Hf 4f attenuation is due to variations in XPS position for the pre- and postdeposition scans. Sample III was prepared in a different manner than samples I and II: The hafnia tunnel oxide was first annealed at 800 K under a silane partial pressure of 1.9×10^{-5} torr for 30 min. Ge dots were then grown by HWCVD, and finally, the Ge dots were capped in Si using the same conditions as sample II. HfO$_2$ control oxide ($\sim$150 Å) grown by reactive dc sputtering in an Ar/O$_2$ ambient at room temperature, and 2000 Å TaN electrode deposited by reactive dc sputtering were used to complete the MOS stack structure. A control sample without Ge NCs using just two layers of HfO$_2$ was also fabricated.

III. RESULTS AND DISCUSSION

Cross-sectional scan transmission electron microscopy (STEM) and transmission electron microscopy (TEM) were used to examine the Ge NCs in the HfO$_2$ matrix. Fig. 3(A) shows a STEM image of Ge NCs buried in the HfO$_2$ matrix, and Fig. 3(B) shows a TEM image of the Ge NC encapsulated by Si/HfSiO$_x$.

XPS was used to examine the chemical state of the deposited Ge and Si, as shown in Fig. 2(A). For sample I, the Ge 2p XP spectra feature at $\sim$1220 eV is indicative of oxidized Ge while the feature at $\sim$1218 eV is from metallic Ge dots. The binding energy shift for GeO and GeO$_2$ are 1.8 and 3.2 eV, respectively [13]. The Ge feature at $\sim$1220 eV exhibits a binding energy shift of 2.5 eV indicating it is at an oxidation state between 2+ and 4+ for GeO and GeO$_2$, respectively, and is likely due to the formation of a hafnium germinate [14]. These germinate signal is originating from the exposed regions between the Ge dots, and it is highly likely hafnium germinate also exists beneath the Ge dots. The treatment of the Ge dots with silane at 875 K (sample II) has a marked effect on the hafnium germinate. The feature at $\sim$1220 eV is no longer seen and the metallic germanium signal has been significantly attenuated [Fig. 2(A)]. The role silane treatment plays in hafnium germinate removal was believed due to the following reaction [14]:

$$\mathrm{HfGeO}_x + \mathrm{Si} \rightarrow \mathrm{Ge} + \mathrm{HfSiO}_x. \tag{2}$$

For sample III, the silane anneal at 800 K produces very small mount hafnium silicate and metallic Si on the surface according to XPS (spectra not shown), and the Si 2p spectrum of sample III is similar to the Si 2p spectrum in Fig. 2(B) for sample II. Subsequent Ge dot growth to this treated surface

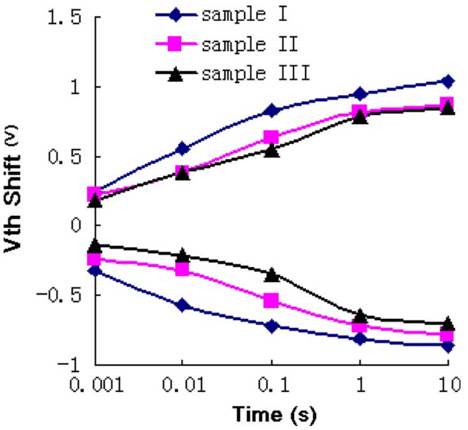

Fig. 4. Programming/erasing speed characteristics ±8-V stress.

leads to very little hafnium germinate formation [14]. The silane treatment to selectively cap the Ge dots with Si most likely also decreases the amount of exposed hafnium germinate surfaces. Furthermore, the silane treatment passivates the Ge dot surface for *ex-situ* transportation for device fabrication. Thus, the silane treatment serves multiple purposes. It significantly reduces the amount of hafnium germinate that forms during HWCVD of Ge dots and passivates the Ge dots from ambient oxidants for transportation to device fabrication. It also prevents hafnium germinate formation between the control oxide and the Ge dots. All of these factors lead to the improved device performance.

High-frequency capacitance–voltage tests (1 MHz) were used to characterize the electrical properties of all samples. After each stress pulse, a -2 to 2 V C–V scan was applied to determine the threshold voltage (V_{th}) shift. The control sample shows a only negligible memory window compared to samples with NCs under the same stress conditions, which indicates that most of the charge storage is due to the existence of the NCs. Fig. 4 shows the device programming/erasing characteristics of all the samples. The memory window of sample II and III is slightly smaller than sample I. This may be because that the samples under silane treatment have lower interface trap density due to the removal of HfGeO$_x$. Using the following equation, the charge storage density can be calculated:

$$\Delta V_{\text{th}} = \frac{q n_{\text{nc}} x}{\varepsilon_{\text{ox}}}\left(t_{\text{control}} + 0.5\frac{\varepsilon_{\text{ox}} t_{\text{nc}}}{\varepsilon_{\text{nc}}}\right) \qquad (3)$$

where the NC density $n_{\text{nc}} = 3 \times 10^{11}\ /\text{cm}^2$, average NC size $t_{\text{nc}} = 8$ nm, control oxide thickness $t_{\text{control}} = 15$ nm, tunneling oxide dielectric $\varepsilon_{\text{ox}}(\text{HfO}_2) = 20$, and NC dielectric constant $\varepsilon_{\text{nc}} = 16\,\varepsilon_0$. Under 8 V, 10 ms stress, the V_{th} shift of sample III is about 0.37 V, it yields $x = 6.6$ as the approximate number of electrons stored per NC.

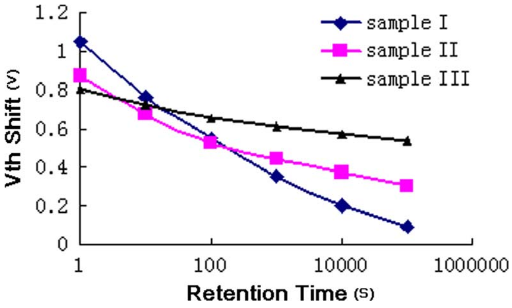

Fig. 5. Data retention characteristics at room temperature.

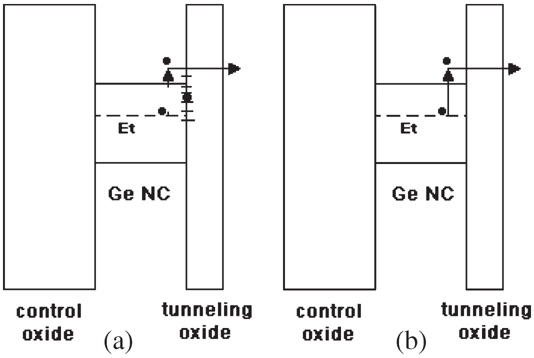

Fig. 6. (A) Band diagram of memory device with bare Ge NCs. (B) Band diagram of memory device with Ge–Si/HfSiO$_x$ core-shell NCs.

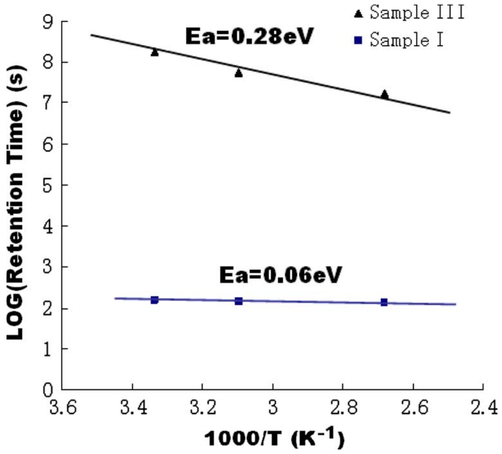

Fig. 7. Arrhenius plot of retention time versus reciprocal temperature.

Fig. 5 shows the retention characteristics of the devices. An obvious retention improvement is seen for samples II and III compared to sample I. This improvement can be understood in the following way: For sample I, due to the existence of low-quality GeO$_x$/HfGeO$_x$, lots of trap states were created at the Ge NC–high-κ dielectric interface, as shown in Fig. 6(A). With the help of these trap states, the stored electrons can easily tunnel back to the Si substrate thus degrading retention. However, for sample III, the Si/HfSiO$_x$ shell layer separates the Ge NCs from ambient oxidants in during processing and also helps to change the GeO$_x$/HfGeO$_x$ back to metallic Ge through the reaction $\text{HfGeO}_x + \text{Si} \rightarrow \text{Ge} + \text{HfSiO}_x$. Thus, a high-quality Ge NC–high-κ dielectric interface is achieved and most interface traps are removed, as shown Fig. 6(B). In this case, the charges are stored at the deep traps under the Ge conduction band, where large activation energy (E_a) is needed to activate the electrons before it can tunnel back to the Si substrate. This results in better retention characteristics. To verify this, temperature-dependent retention characteristics test was done. Fig. 7 shows the Arrhenius plot of retention time of sample I and III at room temperature, 50 °C and 100 °C. Here, the retention time was defined as the time that the threshold

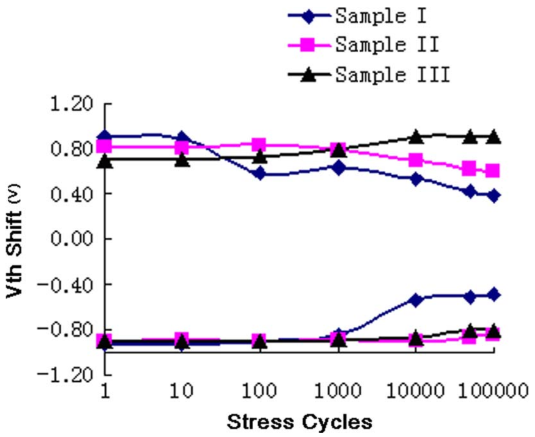

Fig. 8. Endurance characteristics of device under ±8 V at room temperature with pulsewidth 1 s.

voltage shift decreases by a factor of 50%, compared to the initial value. The activation energy of sample I is about 0.06 eV, while the activation energy of sample III is about 0.28 eV.

The device endurance characteristics under stress cycling are shown in Fig. 8. Samples II and III show better endurance characteristics than that of sample I. The reason can be considered that many interface traps at the Ge NCs–high-κ dielectric interface are not stable and may change their trapping properties under stress cycling. From the results, it can be inferred that some traps may lose their capability to capture electrons/holes, and for some other traps, it is more difficult to release the electrons/holes after capture, compared to the beginning.

IV. CONCLUSION

A new core-shell Ge–Si(Si/HfSiO$_x$) NC structure consisting of Ge NCs encapsulated with a Si/HfSiO$_x$ shell is introduced for nonvolatile memory applications. The experiments results showed that NC-dielectric interface quality was dramatically improved. The retention characteristics of the device were improved a lot and better tradeoff between retention and programming/erasing speed can be achieved.

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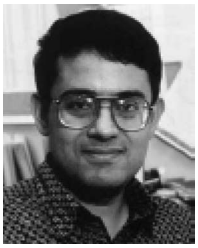

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