JVSTB Journal of Vacuum Science & Technology B

Fabrication and characterization of metal-oxide-semiconductor GaAs capacitors on Ge Si 1 x Ge x Si substrates with Al 2 O 3 gate dielectric

D. Shahrjerdi, N. Nuntawong, G. Balakrishnan, D. I. Garcia-Gutierrez, A. Khoshakhlagh, E. Tutuc, D. Huffaker, J. C. Lee, and S. K. Banerjee

Citation: Journal of Vacuum Science & Technology B **26**, 1182 (2008); doi: 10.1116/1.2835061
View online: http://dx.doi.org/10.1116/1.2835061
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/26/3?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Fabrication and characterization of metal-oxide-semiconductor GaAs capacitors on $Ge/Si_{1-x}Ge_x/Si$ substrates with Al_2O_3 gate dielectric

D. Shahrjerdi[a)]
Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758

N. Nuntawong and G. Balakrishnan
Center for High Technology Materials, The University of New Mexico, Albuquerque, New Mexico 87106

D. I. Garcia-Gutierrez
Advanced Technology Development Facility (A TDF-SEMA TECH), Austin, Texas 78741

A. Khoshakhlagh
Center for High Technology Materials, The University of New Mexico, Albuquerque, New Mexico 87106

E. Tutuc
Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758

D. Huffaker
Center for High Technology Materials, The University of New Mexico, Albuquerque, New Mexico 87106

J. C. Lee and S. K. Banerjee
Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758

(Received 26 October 2007; accepted 17 December 2007; published 30 May 2008)

In this article, we have studied fabrication and characterization of GaAs metal-oxide-semiconductor (MOS) capacitors with Al_2O_3 gate dielectric. 300 nm thick GaAs layers were grown epitaxially on $Ge/Si_{1-x}Ge_x/Si$ substrates. Cross-sectional transmission electron microscopy (TEM) confirmed a threading dislocation density of $\sim 10^7/cm^2$ in the GaAs layer. In addition, it was observed that threading dislocations were mainly confined within the first ~50 nm of the GaAs layer, adjacent to the Ge film. Interfacial self-cleaning attribute of GaAs upon atomic layer deposition of Al_2O_3 was confirmed by x-ray photoelectron spectroscopy (XPS) analysis. However, the $Al_2O_3/GaAs$ interface properties were remarkably improved by GaAs native removal in dilute HF (1%) followed by sulfur treatment in $(NH_4)_2S$, substantiated by probing electrical characteristics of the MOS capacitors and cross-sectional TEM analysis. Thermodynamic properties of Al_2O_3/sulfide-treated GaAs interface was also studied by monitoring the *C-V* characteristics of GaAs MOS capacitors implying excellent thermal stability of the $Al_2O_3/GaAs$ interface. © *2008 American Vacuum Society.* [DOI: 10.1116/1.2835061]

I. INTRODUCTION

With the end of bulk silicon (Si) complementary metal-oxide-semiconductor (CMOS) roadmap looming, identifying the next generation of logic devices is becoming crucial, leading to a tremendous increase of activity in multigate and enhanced channel mobility metal-oxide-semiconductor field-effect transistors (MOSFETs). Superior electron transport properties of III-V materials render them suitable as a potential candidate to drive CMOS technology beyond the 22 nm node.[1] There are, however, several grand challenges which impede the implementation of III-V-based logic transistors. This includes poor hole mobility of III-V materials, limitations of commercially available III-V substrates in terms of cost and size, and the lack of a compatible gate dielectric.

High-κ dielectrics have gained popularity in mainstream Si-based CMOS technology as an alternative gate dielectric to SiO_2. Furthermore, employing high-*k* dielectrics has enabled a demonstration of high performance Ge *p*-MOSFETs.[2,3] Nonetheless, Ge *n*-MOSFETs have not yet shown better performance than the Si counterpart. This, coupled with the fact that some of III-V materials are lattice matched with Ge opens up the possibility of integrating *n*-channel III-V transistors with *p*-channel Ge transistors. This proposed scheme will circumvent the first two aforementioned drawbacks of III-V based logic systems. Furthermore, in order to mitigate the gate stack issue, there has been a tremendous ongoing search for an appropriate gate dielectric which unpins the Fermi level and provides a thermally stable interface with III-V materials. This includes the use of *a*-Si and *a*-Ge interfacial layers,[4–6] molecular beam epitaxy grown Ga_2O_3/Gd_2O_3 dielectric,[7,8] GaAs surface nitridation,[9] as well as atomic layer deposition (ALD)-grown Al_2O_3.[10,11] In this article, we have studied the capacitance-voltage (*C-V*) characteristics of GaAs capacitors using Al_2O_3 gate dielectric fabricated on $Ge/Si_{1-x}Ge_x/Si$ substrates.

II. EXPERIMENT AND RESULTS

The earlier studies on the growth of GaAs on Si and Ge substrates have shown that by using off-cut wafers, antiphase boundaries (APBs) could be avoided.[12,13] Therefore,

[a)]Electronic mail: davood@mail.utexas.edu

in this work, we have chosen the (100) Si wafers with a 4° off-cut toward the [110] direction to suppress the formation of APBs within the GaAs layer. In order for integration of GaAs on Si, GaAs was grown on Ge buffer layer. The Ge buffer layer was grown in an ultrahigh-vacuum chemical-vapor-deposition (CVD) system. A very thin compositionally graded $Si_{1-x}Ge_x$ buffer layer was employed to prevent the threading dislocations from propagation into the Ge layer. This structure consisted of $Si_{1-x}Ge_x$ layers with $x=0.2$, 0.25, and 0.4, and a thickness of about 25, 20, and 30 nm, respectively. The final Ge film was ~35 nm and fully relaxed with a surface rms roughness of ~5 Å, measured by atomic force microscopy (AFM). Additional details on the growth condition and physical characterization of the $Si_{1-x}Ge_x$ buffer layer can be found elsewhere.[14] Then, samples were transferred into a metal-organic CVD (MOCVD) system where the GaAs layer was grown at 60 Torr using trimethylgallium and tertiarybutylarsine. The GaAs growth cycle was started by baking the substrate in hydrogen ambient at 450 °C for 5 min to thermally remove GeO_x. Next, GaAs layer was grown at temperatures starting from 550 to 700 °C and nominal V/III ratios from 3.5 to 12. The ultimate surface rms roughness of the sample was ~10 Å, measured by AFM. Moreover, a threading dislocation density of $\sim 10^7/cm^2$ was evaluated from the cross-sectional TEM analysis. This threading dislocation density could be sufficient for MOSFET fabrication on the GaAs layer. However, threading dislocations potentially serve as charge recombination centers and therefore lead to an increase of the off-state current in MOSFET devices. Cross-sectional TEM study also revealed that the threading dislocations within the GaAs layer were not generated at the GaAs/Ge interface; rather they were propagated mainly from the $Si_{0.6}Ge_{0.4}$/Ge interface into the GaAs layer. However, it is notable that most of the threading dislocations were confined within the first 50 nm of the GaAs, in vicinity of the Ge layer shown in Fig. 1(a). In addition, the cross-sectional composition information of the sample as obtained by energy dispersive x-ray (EDX) spectroscopy overlaid on the high angle annular dark-field scanning TEM (HAADF-STEM) micrograph is illustrated in Fig. 1(b). This reveals an abrupt interface between the Ge and GaAs layers.

Next, an ALD-Al_2O_3 dielectric was deposited on the GaAs layer at 250 °C by alternating water and trimethylaluminum (TMA) precursors. ALD-grown Al_2O_3 offers several potential advantages, including good thermal stability and relatively large dielectric constant. Interestingly, the reduction and subsequent removal of GaAs native oxide upon atomic layer deposition of Al_2O_3 using TMA precursor have been previously reported on GaAs-based substrates.[11,15] We have also investigated the latter phenomenon using x-ray photoelectron spectroscopy (XPS). In this experiment, a ~3 nm thick ALD-Al_2O_3 was deposited on the GaAs sample without performing any chemical cleaning on the GaAs surface. Figure 2(a) illustrates the obtained XPS As 3*d* and Ga 2*p* spectra of the Al_2O_3/GaAs interface. For analysis of the As 3*d* spectrum, we have considered doublets for different

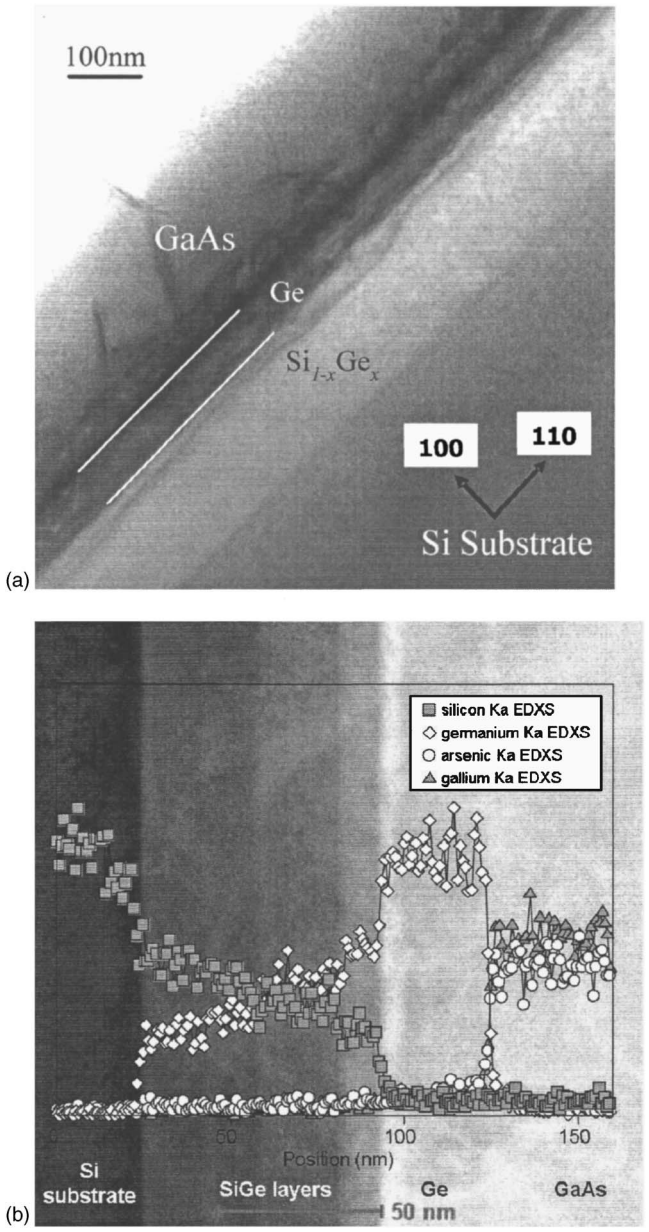
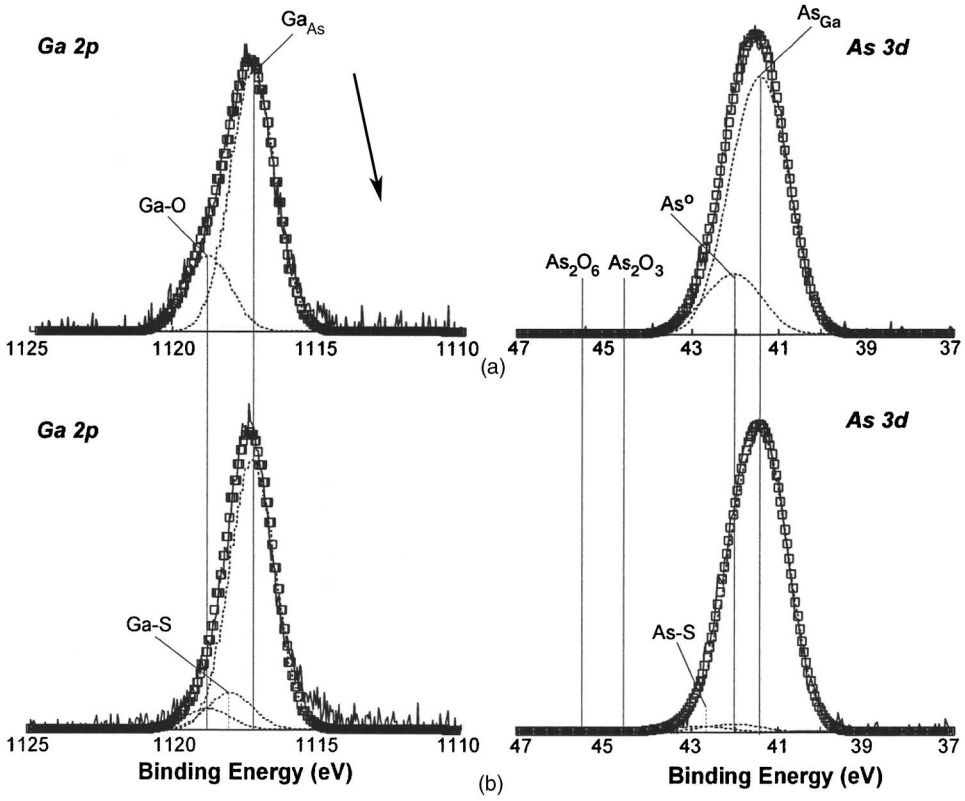


FIG. 1. (a) Cross-sectional TEM micrograph of MOCVD-grown GaAs on Ge/$Si_{1-x}ge_x$/Si substrate. (b) Cross-sectional composition information obtained by EDX overlaid on the HAADF-STEM micrograph indicates an abrupt interface between GaAs and Ge.

As bonding in this region. Arsenic doublet has a peak ratio of 3:2 with a separation of 0.7 eV. It is notable that no As–O peak is discernable from the spectral fit to the As 3*d* region, corroborating the interfacial self-cleaning attribute of atomic layer deposition of Al_2O_3 on GaAs. However, a Ga–O bond is detectable as evidenced by the presence of a peak at 1118.8(±0.2) eV in Ga 2*p* region. In order to diminish the undesirable GaAs native oxide thickness, we have recently developed a simple chemical cleaning protocol for GaAs where we have demonstrated that a combination of HF(1%) dip for 1 min, followed by sulfur passivation using ammonium sulfide (20%) for 10 min, improves *C-V* characteristics of GaAs MOS capacitors.[16] XPS analysis was also carried



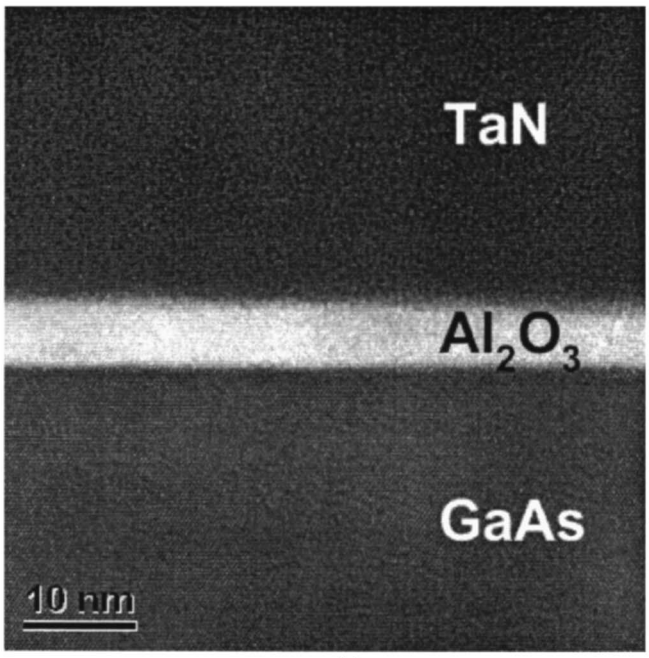


FIG. 2. The XPS Ga 2*p* and As 3*d* spectra of the Al_2O_3/GaAs interface for samples (a) without and (b) with GaAs surface chemical treatment prior to ALD-Al_2O_3 deposition. (c) An abrupt Al_2O_3/GaAs interface was revealed by cross-sectional TEM analysis.

out on a sulfide-treated sample capped with an ~3 nm ALD-Al_2O_3. Despite the chemical surface treatment of GaAs, a Ga–O peak is detectable in the Ga 2*p* region. However, no clear evidence of As–O bonding is discernable from the fits to the As 3*d* spectrum shown in Fig. 2(b). The intensity of the Ga 2*p* and As 3*d* XPS spectra were normalized relative to the Ga_{As} and As_{Ga} peaks, respectively.

ALD-Al_2O_3 (82 Å thick) was grown as the gate dielectric on GaAs, with and without GaAs surface chemical treatment prior to the oxide deposition. The sulfide-treated samples underwent different postdeposition annealing (PDA) conditions in N_2 ambient. Finally, TaN was deposited as the metal gate and was patterned using standard photolithography and reactive ion etching. Figure 2(c) exhibits the cross-sectional TEM micrograph of the final gate stack of a sulfide-treated sample annealed at 600 °C for 7 min, indicating an abrupt interface between Al_2O_3 and GaAs.

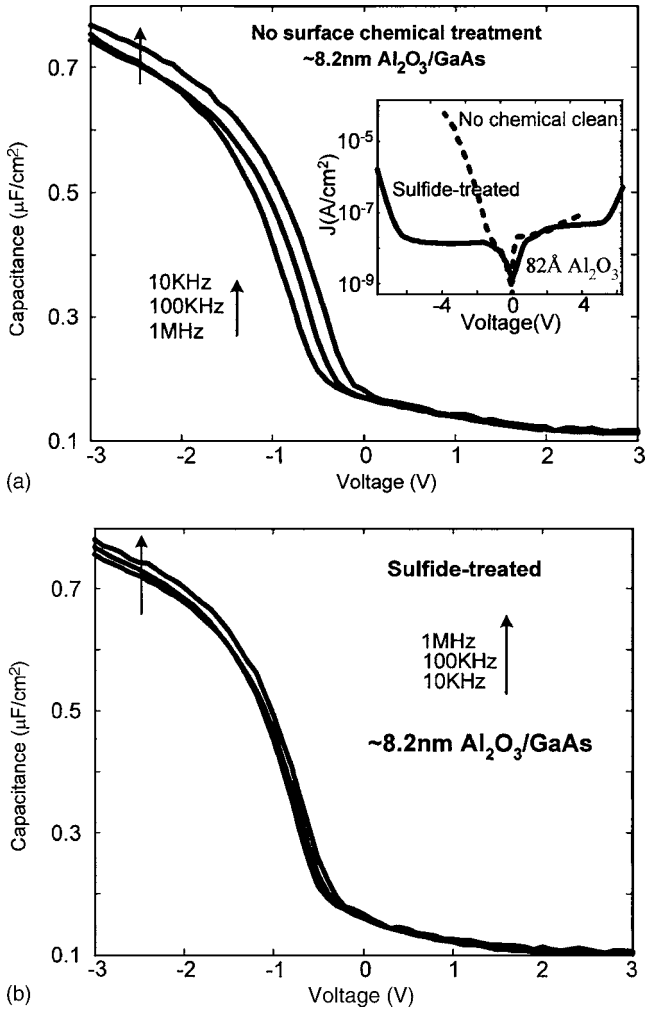


FIG. 3. Frequency dispersion behavior of GaAs MOS capacitors (a) without and (b) with chemical surface treatment. The inset of figure (a) indicates the improvement of interface quality by employing sulfur passivation.

In order to further characterize Al_2O_3/GaAs interface quality, *C-V* characteristics of the GaAs MOS capacitors were monitored at different frequencies. Figure 3 compares the frequency dispersion behavior of GaAs MOS capacitors with and without GaAs surface chemical treatment indicating an improved interface quality upon sulfide treatment. The inset of Fig. 3(a) compares the leakage current density–voltage characteristics of these two samples. This also further confirmed high quality interface between Al_2O_3 and the sulfide-treated GaAs sample.

Thermal stability of Al_2O_3/GaAs interface was also investigated for different PDA conditions, by probing the *C-V* characteristics of the samples (Fig. 4). The frequency dispersion behavior, capacitance equivalent thickness (CET) and hysteresis of the sulfide-treated GaAs samples were closely monitored implying excellent thermal stability of Al_2O_3/GaAs interface. The reduction of CET as well as hysteresis at elevated temperatures could stem from further densification of Al_2O_3. However, the mechanism for degradation of the frequency dispersion behavior at elevated temperatures is still unknown. We surmise that the outdiffusion of As

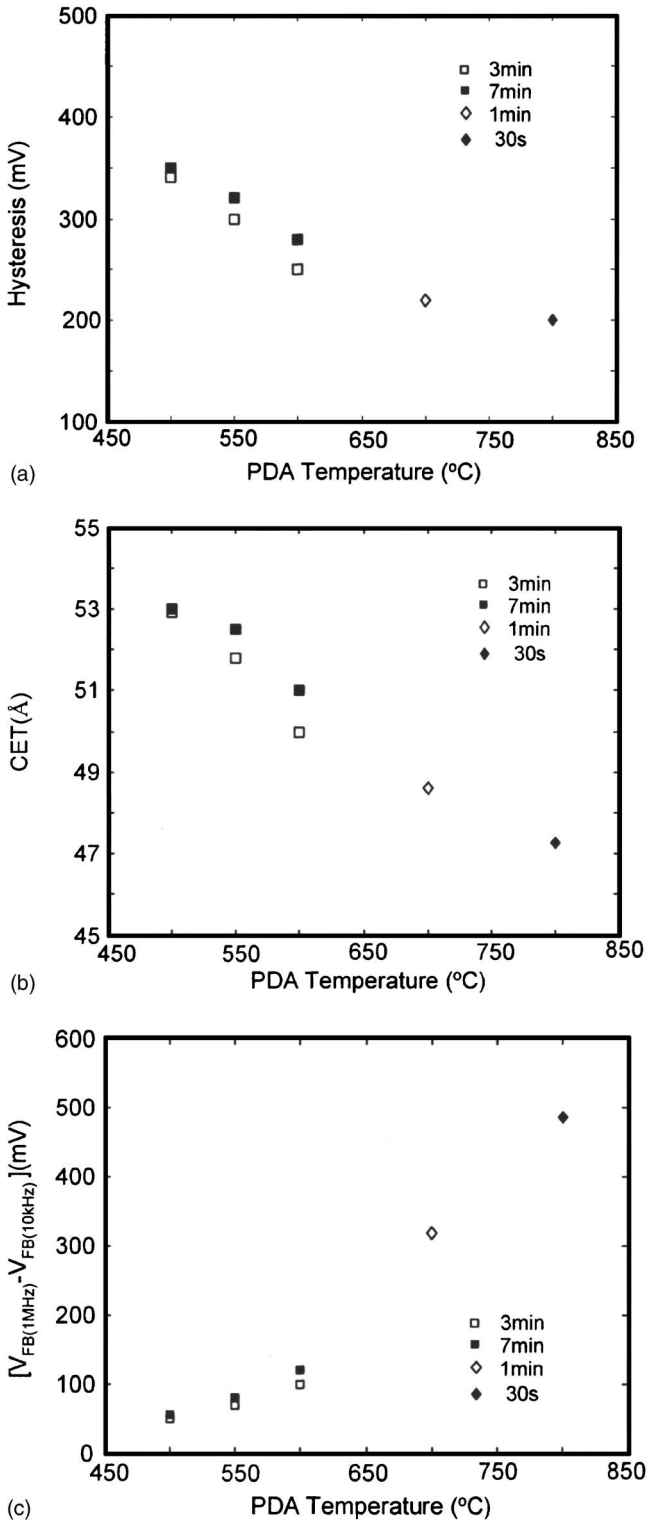


FIG. 4. ALD-Al_2O_3/GaAs interface exhibited an excellent thermal stability confirmed by monitoring (a) hysteresis, (b) CET, and (c) frequency dispersion of GaAs capacitors with 82 Å Al_2O_3 under different PDA conditions.

atoms could possibly be the culprit for degradation of the *C-V* frequency dispersion behavior. The excellent characteristics of the ALD-Al_2O_3/GaAs interface, in terms of state traps as well as thermal stability, make ALD-Al_2O_3 an appropriate choice of dielectric for fabrication of inversion-type enhancement-mode GaAs MOSFETs.

III. CONCLUSIONS

In summary, we have fabricated and characterized GaAs MOS capacitors using ALD-Al_2O_3 on $Ge/Si_{1-x}Ge_x/Si$ substrates. Cross-sectional TEM analysis revealed an abrupt interface between Ge and GaAs layers. In addition, it was observed that threading dislocations were mainly confined within the first 50 nm of the GaAs layer in vicinity of the Ge film. A threading dislocation density of $\sim 10^7/cm^2$ was deduced from the cross-sectional TEM analysis. XPS analysis confirmed the removal of arsenic oxides upon atomic layer deposition of Al_2O_3 on GaAs with no surface chemical cleaning. However, surface chemical treatment with HF followed by sulfur passivation appeared to remarkably improve the frequency dispersion behavior of GaAs MOS capacitors. In addition, excellent thermal stability of ALD-Al_2O_3/GaAs interface was determined by monitoring electrical characteristics of the sulfide-treated GaAs MOS capacitors annealed under different PDA conditions.

ACKNOWLEDGMENTS

This work has been supported in part by DARPA and Micron foundation.

[1]International Technology Roadmap for Semiconductors, 2004 update.
[2]D. Q. Kelly, J. P. Donnelly, S. V. Joshi, S. Dey, D. I. García-Gutiérrez, M. José-Yacamán, and S. K. Banerjee, Tech. Dig. - Int. Electron Devices Meet. **2005**, 923.
[3]W. P. Bai *et al.*, Tech. Dig. VLSI Symp. **2003**, 121.
[4]S. Koveshnikov, W. Tsai, I. Ok, J. C. Lee, V. Torkanov, M. Yakimov, and S. Oktyabrsky, Appl. Phys. Lett. **88**, 022106 (2006).
[5]D. Shahrjerdi, M. M. Oye, A. L. Holmes, Jr., and S. K. Banerjee, Appl. Phys. Lett. **89**, 043501 (2006).
[6]I. Ok, H. Kim, M. Zhang, C. Kang, S. J. Rhee, C. Choi, S. A. Krishnan, T. Lee, F. Zhu, G. Thareja, and J. C. Lee, IEEE Electron Device Lett. **27**, 145 (2006).
[7]M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, R. Gregory, and D. Nguyen, IEEE Electron Device Lett. **26**, 713 (2005).
[8]K. Rajagopalan, J. Abrokwah, R. Droopad, and M. Passlack, IEEE Electron Device Lett. **27**, 959 (2006).
[9]F. Gao, S. J. Lee, D. Z. Chi, S. Balakumar, and D.-L. Kwong, Appl. Phys. Lett. **90**, 252904 (2007).
[10]Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, Appl. Phys. Lett. **88**, 263518 (2006).
[11]M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **87**, 252104 (2005).
[12]R. Fischer *et al.*, J. Appl. Phys. **58**, 374 (1985).
[13]E. A. Fitzgerald, C. L. Dohrman, K. Chilukuri, and M. J. Mori, ECS Trans. **3**, 561 (2006).
[14]S. Dey, S. Joshi, D. Garcia-Gutierrez, M. Chaumont, A. Campion, M. Jose-Yacaman, and S. K. Banerjee, J. Electron. Mater. **35**, 1607 (2006).
[15]M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, Appl. Phys. Lett. **86**, 152904 (2005).
[16]D. Shahrjerdi, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **91**, 063501 (2007).