Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach

Davood Shahrjerdi, Domingo I. Garcia-Gutierrez, and Sanjay K. Banerjee

***Abstract*—Fabrication of nickel nanocrystal Flash memories using a polymeric approach is presented. Heat treatment of the poly (styrene-*b*-methyl methacrylate) block copolymer with a molecular weight of 67 000 g/mol followed by PMMA removal in an organic solvent created a porous PS film with 20-nm-diameter pores and a total pore density of $\sim 6 \times 10^{10}$ cm^{-2}. A trilayer pattern-transfer approach was employed in order to solve the metal lift-off issue intertwined with the low aspect ratio of the block copolymer patterns. As a result, a highly uniform self-assembled array of nickel nanocrystals was attained and utilized for Flash memory fabrication. The memory devices demonstrated an unchanged memory window for up to 2×10^5 stressing cycles.**

***Index Terms*—Diblock copolymer, nanocrystals, nonvolatile memory, self-assembly.**

I. Introduction

THE MARKET for NAND floating gate nonvolatile Flash memory is growing fast. Currently, NAND Flash memory is the dominant technology for high-volume, low-cost, and low-power memory applications such as cellular phones, memory cards, and multimedia storage appliances. Flash memory devices are pushing to sub-50-nm dimensions, imposing formidable challenges on device scaling mainly due to the stringent leakage requirements for long term charge storage which severely restrict tunnel oxide scaling [1], [2].

Nanocrystal floating gate Flash memory is considered as a promising candidate to continue the scaling trend which offers potential advantages over the conventional floating gate structure, including improved scalability, as well as superior charge storage properties [3]. In general, an electrically isolated discrete array of nanocrystals provides better immunity against local defects in the tunnel oxide, thereby allowing the use of a thinner oxide which, in turn, gives rise to a lower operating voltage [4], [5]. Moreover, charge loss through the lateral paths appears to be significantly suppressed by utilizing nanocrystals, as opposed to a continuous film as the charge trapping layer, leading to a better retention properties. From a material standpoint, metal quantum dots are of interest due to their higher density-of-states and potentially larger work function, as compared to silicon nanocrystals. This consequently provides a larger barrier for stored electrons [6], [7]. Nonetheless, formation of quantum dots with uniformity in both size and density remains a challenge which can be considered as the overriding hurdle to device manufacturability.

For the first time, Guarini *et al.* [8] have successfully demonstrated silicon nanocrystal Flash memory devices using a self-assembled poly (styrene-*b*-methyl methacrylate) (PS-*b*-PMMA) copolymer nanotemplate. In addition to synthetic polymers, self-assembly of biological polymers such as Chaperonin and Ferittin protein molecules has also attracted a lot of interest for nanoscale ordering of materials intended for nanocrystal Flash memory application [9], [10].

In this letter, we demonstrated fabrication of nickel nanocrystal Flash memory using a polymeric self-assembly approach in order to attain a tight control over the size and the density of metal nanocrystals using PS-PMMA diblock copolymer as a nanotemplate. Using the block copolymer only as the sacrificial layer during the metal lift-off process, limits the thickness of the deposited metal to a few nanometers [11]. Hence, a trilayer pattern-transfer approach was employed in order to engineer the aspect ratio of the patterns which is intended to facilitate the metal lift-off process [12], [13].

II. Copolymer Self-Assembly

Block copolymers are composed of two chemically distinct polymer chains that are covalently linked at one end. Polymer blends are, in principle, immiscible and phase separate. The connectivity between the two segments of a block copolymer limits the length scale of this phase separation. Upon annealing, block copolymers tend to self-assemble into nanometer scale domains in order to minimize the total free energy of the system [14], [15]. In this letter, a PS-*b*-PMMA block copolymer with a molecular weight of 67 000 g/mol and polydispersity of 1.09 was used.[1] Surface modification was carried out by spin casting a comparatively thick film of a random copolymer,[1] followed by heat treatment of the samples at 170 °C for 48 h. Then, the unanchored part of the random copolymer was washed off in excess toluene, leaving behind a ~6-nm-thick polymer film on the surface. Subsequently, a ~36-nm-thick PS-*b*-PMMA block copolymer layer was spin cast and annealed for 24 h at 180 °C. As a result, a highly uniform array of hexagonally close-packed PMMA cylinders was produced within a PS matrix.

Manuscript received May 11, 2007; revised June 11, 2007. This work was supported in part by the Defense Advanced Research Projects Agency, by the Microelectronics Advanced Research Corporation-Focus Center on Materials, Structures and Devices, by the Department of Energy, by the National Science Foundation Nanotechnology Interdisciplinary Research Team, and by the Micron Foundation. The review of this letter was arranged by Editor Y. Taur.

D. Shahrjerdi and S. K. Banerjee are with the Microelectronics Research Center, University of Texas, Austin, TX 78758 USA (e-mail: davood@mail.utexas.edu).

D. I. Garcia-Gutierrez is with the Advanced Technology Development Facility (ATDF-SEMATECH), Austin, TX 78741 USA.

Digital Object Identifier 10.1109/LED.2007.902612

[1]Diblock copolymer and random copolymer were synthesized by Polymer Source, Inc.

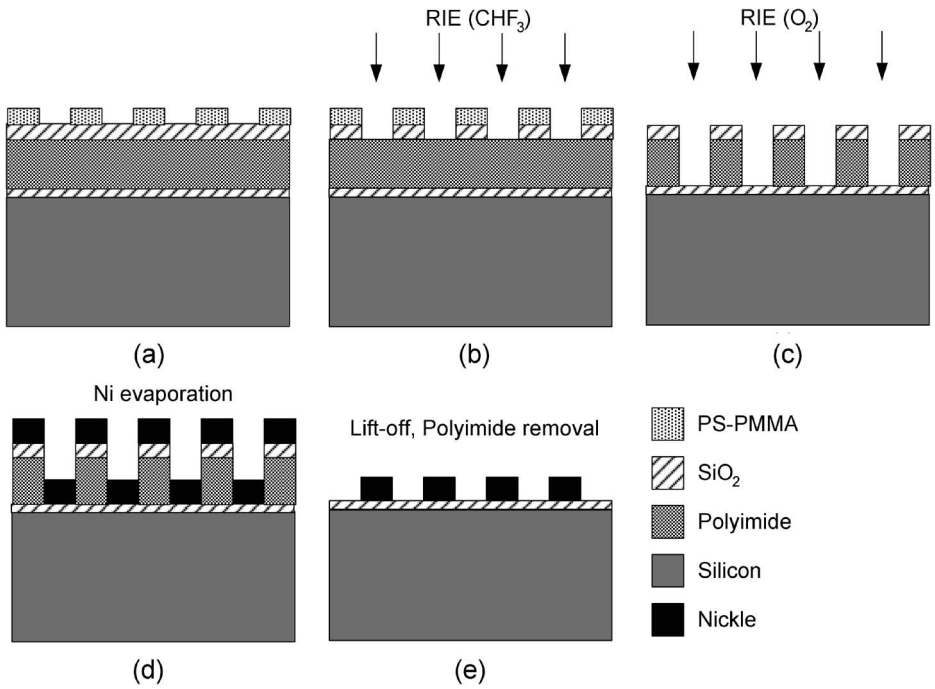

Fig. 1. Schematic of the pattern-transfer approach representing the process flow to creating a highly uniform array of nickel nanocrystals.

The impact of annealing temperature, as well as film thickness on the self-assembly of the aforementioned polymer, has been systematically examined in [16]. Finally, the PMMA blocks were removed in glacial acetic acid creating a PS nanotemplate with 20-nm-diameter pores and a total pore density of $\sim 6 \times 10^{10}$ cm^{-2}.

Although the use of this specific copolymer enables us to control the spatial distribution of nanoparticles, from a technological perspective, the obtained size and density specifications need to be significantly improved in order to meet the requirements for sub-32-nm nonvolatile memory devices. It is notable that the spontaneous microphase separation of diblock copolymers with a narrow polydispersity occurs above their glass transition temperature if $\chi N > 10$ where χ is the Flory–Huggins interaction parameter, and N is the number of monomers per chain [14]. For the current copolymer system, this value is $\sim$12 indicating that the cylindrical phase is almost at the low phase separation limit. However, Russell *et al.* [17] have demonstrated phase separation of a PS-*b*-PMMA with cylindrical microdomains and a pore density of 1.9×10^{11} cm^{-2} by means of an external electric field in order to orient the domains parallel to the field lines. Alternatively, utilizing other polymer systems such as spherical microdomains can easily generate porous copolymer templates with pore densities $> 10^{11}$ cm^{-2} simply by annealing a thin spin-coated film of the copolymer [18]. The resulting polymeric scaffolds may be suitable for sub-50-nm devices if an extremely tight distribution of nanocrystals among the cells is ensured.

III. Device Fabrication

Metal–oxide–semiconductor capacitors were fabricated on conventional p-type (100) silicon substrates. Initially, a 47-Å-thick tunnel oxide was thermally grown on Si wafers followed by the formation of a trilayer sandwich of organic/inorganic/organic structure. The trilayer structure consists of a polyimide bottom layer, a plasma enhanced chemical vapor deposition (PECVD) SiO_2 middle layer, and a block copolymer top layer. Polyimide was chosen as the bottom layer due to its high glass transition temperature of 309 °C, which is higher than the subsequent annealing temperatures. A 60-nm-thick polyimide film was spin coated, and a 15-nm-thick PECVD SiO_2 layer was deposited onto the polyimide at 285 °C. Subsequently, a PS-*b*-PMMA block copolymer layer was spin coated and treated to produce a porous PS nanotemplate [Fig. 2(a)]. The statistical analysis of the copolymer pore size distribution with a Gaussian fit is illustrated in Fig. 2(d).

This structure was used in the trilayer pattern-transfer technique, which is shown in Fig. 1, to form an array of nickel nanocrystals. The polymer patterns were transferred into the underlying oxide using CHF_3 reactive ion etch (RIE) [Figs. 1(b) and 2(b)]. The pattern-transfer process was further continued within the polyimide layer using an O_2 RIE [Fig. 1(c)] followed by evaporation of $\sim$120-Å-thick nickel [Fig. 1(d)]. Next, polyimide was removed using a polyimide stripper [2] [Fig. 1(e)] leaving behind a highly uniform array of 20-nm nickel nanodots, as shown in Fig. 2(c). Fabrication of capacitors was finished by depositing a 12-nm LPCVD SiO_2 at 600 °C as the control oxide followed by TaN metal gate deposition and patterning. The inset of Fig. 3(b) demonstrates the cross-sectional TEM micrograph of the ultimate gate stack of the memory MOSCAP with 20-nm-diameter Ni nanoparticles with $\sim$37-nm pitch. A control sample underwent the entire aforementioned processing steps with the exception of nickel deposition.

[2]Polyimide stripper was purchased from Arch Chemicals, Inc.

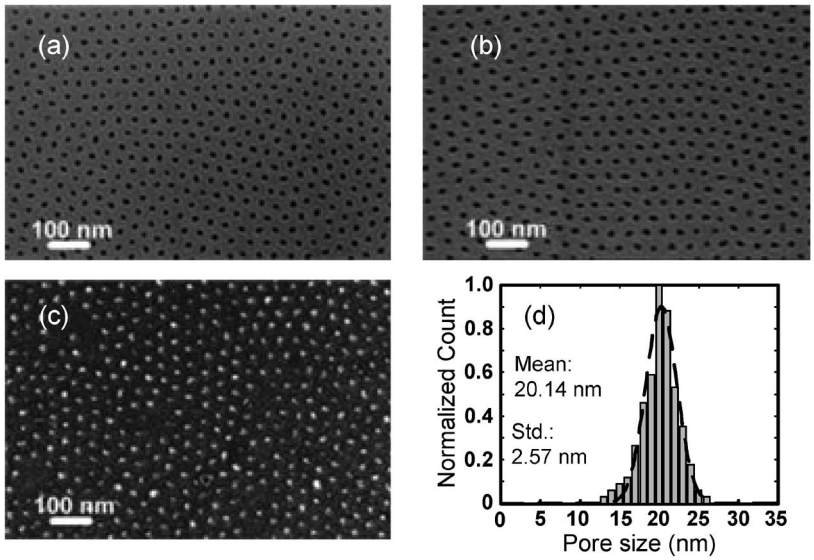

Fig. 2. SEM micrographs of (a) the copolymer patterns, (b) transferred patterns into the underlying PECVD oxide, and (c) nickel nanocrystals. (d) Histogram of the copolymer pore size distribution.

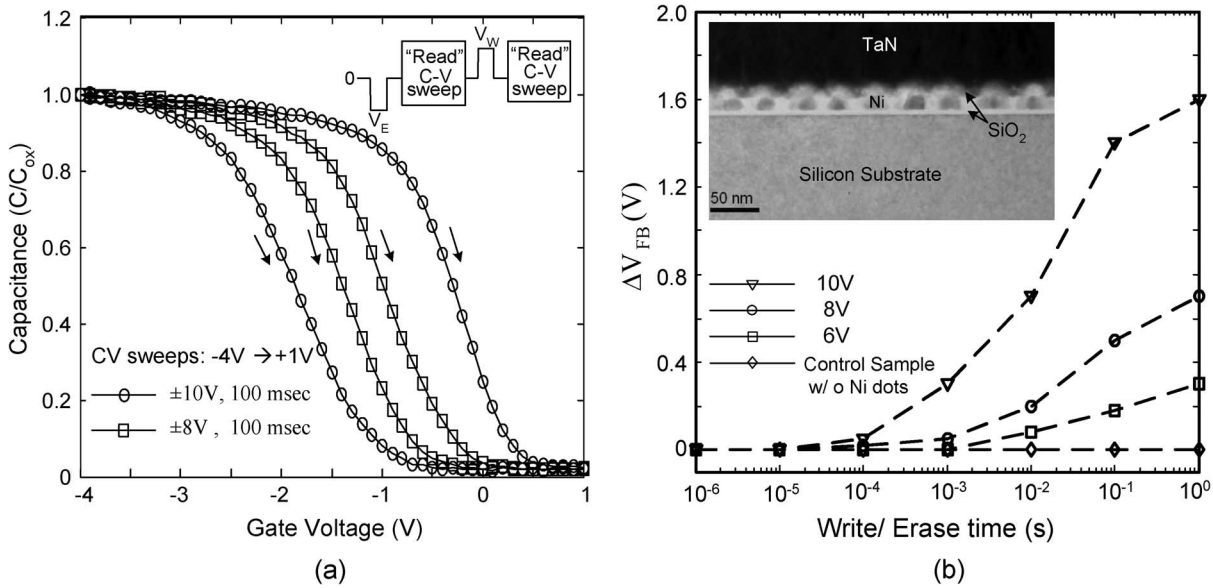

Fig. 3. (a) High-frequency (1 MHz) C–V characteristics of the memory devices under different programming conditions. (b) Transient characteristics of the memory device as a function of write voltage. The inset exhibits the cross-sectional TEM micrograph of the memory gate stack.

IV. Device Characterization

Electrical characteristics of the memory devices were monitored after Fowler–Nordheim tunneling program/erase. Fig. 3(a) shows the high-frequency C–V characteristics of the memory devices for two different programming stress pulses. The inset illustrates the procedure for applying write/erase pulses to devices. A flatband voltage shift of 0.5 V was obtained with a 100-ms write/erase voltage of ± 8 V. No flatband voltage shift was observed for the control sample at different pulse durations with a program voltage of 10 V [Fig. 3(b)] implying that the flatband voltage shift of memory devices is attributed to the charge storage in nanocrystals. Metal nanocrystals potentially possess a higher density-of-states than semiconductors due to their smaller deBroglie wavelengths. As a result, a smaller quantum confinement effect allows a larger storage capacity for each metal nanocrystal. The shift in flatband voltage can be used in order to evaluate the number of trapped charges theoretically by the following expression:

$$\Delta V_{\mathrm{FB}} = \frac{d}{\varepsilon_{\mathrm{ox}}} Q_t \tag{1}$$

where d is the distance between the storage node and the gate electrode, and Q_t is the area density of the trapped charges. For a memory window of 0.5 V obtained with a 100-ms write/erase pulse of ± 8 V, using $d = 40$ Å gives a Q_t of $\sim 4.3 \times 10^{-7}$ C $\cdot$ cm^{-2}. Considering the density of dots, it is expected that approximately 40 electrons were trapped in each nanocrystal. The inset of Fig. 4(a) represents the energy band diagram of the memory system. Endurance characteristics of the memory devices were observed for up to 2×10^5 cycles with 2-ms stress

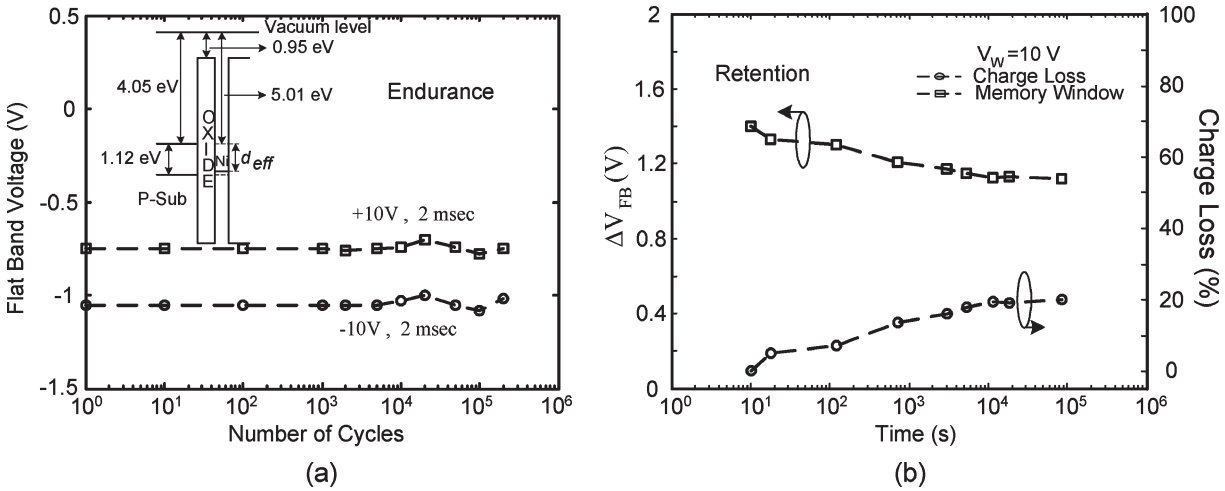

Fig. 4. (a) Endurance characteristics of the memory device. $\Delta V_{\rm FB}$ remains unchanged even after 2×10^5 program/erase cycles. The inset illustrates the energy band diagram of the memory device. (b) Retention properties of the memory device and its charge loss percentage versus time (s).

pulses of ± 10 V, demonstrating a relatively stable memory window [Fig. 4(a)]. The memory devices also demonstrated good retention characteristics, as shown in Fig. 4(b). The percentage charge loss versus time was evaluated using the following expression:

$$\text{Percentage charge loss} = \left(1 - \frac{V_{\rm FB}(t)}{V_{\rm FB}(0)}\right) \times 100 \qquad (2)$$

where $V_{\rm FB}(0) = V_{\rm FB\_prog} - V_{\rm FB\_erase}$, $V_{\rm FB}(t) = V_{\rm FB\_prog} - V_{\rm FB}(t)$, t is time, and $V_{\rm FB\_prog}$ and $V_{\rm FB\_erase}$ are the flatband voltages after program and erase, respectively [19]. This graph indicates that the memory device initially loses a significant amount of charge. However, beyond $\sim 10^4$ s, the charge loss appears to be remarkably diminished.

V. Conclusion

In summary, nickel nanocrystal Flash memory devices were realized using a polymeric approach which offers a tight control over both size and density of nanocrystals. In this letter, the PS-*b*-PMMA block copolymer was used in order to create a nanotemplate for the formation of nickel dots. However, the low aspect ratio of the copolymer patterns inhibited the polymer removal during the lift-off process. A trilayer pattern-transfer technique was utilized to address this limitation and facilitate the metal lift-off process. As a result, a uniform self-assembled array of nickel dots was formed and used to fabricate Flash memory devices. The memory devices demonstrated good retention and endurance characteristics.

Acknowledgment

The authors would like to thank S. Coffee for valuable discussions.

References

[1] *International Technology Roadmap for Semiconductors*, 2005. [Online]. Available. http://public.itrs.net

[2] R. Bez and P. Cappelletti, "Flash memory and beyond," in *VLSI Symp. Tech. Dig.*, 2005, pp. 84–87.

[3] J. D. Blauwe, "Nanocrystal nonvolatile memory devices," *IEEE Trans. Nanotechnol.*, vol. 1, no. 1, pp. 72–77, Mar. 2002.

[4] H. I. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention-time nano-crystal memory," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1553–1558, Sep. 1996.

[5] T.-H. Hou, C. Lee, V. Narayanan, U. Ganguly, and E. C. Kan, "Design optimization of metal nanocrystal memory—Part I: Nanocrystal array engineering," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3095–3102, Dec. 2006.

[6] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystals memories—Part I: Device design and fabrication," *IEEE Trans. Electron Devices*, vol. 49, no. 9, pp. 1606–1613, Sep. 2002.

[7] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystals memories—Part II: Electrical characteristics," *IEEE Trans. Electron Devices*, vol. 49, no. 9, pp. 1614–1622, Sep. 2002.

[8] K. W. Guarini, C. T. Black, Y. Zhang, I. V. Babich, E. M. Sikorski, and L. M. Gignac, "Low voltage, scalable nanocrystal flash memory fabricated by templated self-assembly," in *IEDM Tech. Dig.*, 2003, pp. 22.2.1–22.2.4.

[9] S. Tang, C. Mao, Y. Liu, D. Q. Kelly, and S. K. Banerjee, "Nanocrystal flash memory fabricated with protein-mediated assembly," in *IEDM Tech. Dig.*, 2005, pp. 174–177.

[10] A. Miura, T. Hikono, T. Matsumura, H. Yano, T. Hatayama, Y. Uraoka, T. Fuyuki, S. Yoshii, and I. Yamashita, "Floating nanodot gate memory devices based on biomineralized inorganic nanodot array as a storage node," *Jpn. J. Appl. Phys.*, vol. 45, no. 1, pp. L1–L3, 2006.

[11] K. W. Guarini, C. T. Black, K. R. Milkove, and E. M. Sikorski, "Nanoscale patterning using self-assembled polymers for semiconductor applications," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 19, no. 6, pp. 2784–2788, Nov. 2001.

[12] J. M. Moran and D. Maydan, "Device processing using the trilevel technique," *Polym. Eng. Sci.*, vol. 20, no. 16, pp. 1097–1101, 1980.

[13] M. Park, P. M. Chaikin, R. A. Register, and D. H. Adamson, "Large area dense nanoscale patterning of arbitrary surfaces," *Appl. Phys. Lett.*, vol. 79, no. 2, pp. 257–259, Jul. 2001.

[14] I. W. Hamely, *The Physics of Block Copolymers*. New York: Oxford Univ. Press, 1998.

[15] G. H. Fredrickson and F. S. Bates, "Dynamics of block copolymers: Theory and experiment," *Annu. Rev. Mater. Sci.*, vol. 26, pp. 501–550, 1996.

[16] K. W. Guarini, C. T. Black, and S. H. I. Yueng, "Optimization of diblock copolymer self-assembly," *Adv. Mater.*, vol. 14, no. 13, pp. 1290–1294, 2002.

[17] T. Thurn-Albrecht, R. Steiner, J. DeRouchey, C. M. Stafford, E. Huang, M. Bal, M. Tuominen, C. J. Hawker, and T. P. Russell, "Nanoscopic templates from oriented block copolymer films," *Adv. Mater.*, vol. 12, no. 11, pp. 787–791, 2000.

[18] C. Harrison, M. Park, P. M. Chaikin, R. A. Register, and D. H. Adamson, "Lithography with a mask of block copolymer structures," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 16, no. 2, pp. 544–552, Mar. 1998.

[19] B. De Salvo, G. Ghilbaudo, G. Pananakakis, B. Guillaumot, P. Candelier, and G. Reimbold, "A new physical model for NVM data-retention time-to-failure," in *Proc. IEEE/IRPS*, 1999, pp. 19–23.