Fabrication of Self-Aligned Enhancement-Mode $In_{0.53}Ga_{0.47}As$ MOSFETs With $TaN/HfO_2/AlN$ Gate Stack

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***Abstract*—In this letter, we report the fabrication and characterization of self-aligned inversion-type enhancement-mode $In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor field-effect transistors (MOSFETs). The $In_{0.53}Ga_{0.47}As$ surface was passivated by atomic layer deposition of a 2.5-nm-thick AlN interfacial layer. $In_{0.53}Ga_{0.47}As$ MOS capacitors showed an excellent frequency dispersion behavior. A maximum drive current of 18.5 $\mu A/\mu m$ was obtained at a gate overdrive of 2 V for a MOSFET device with a gate length of 20 μm. An I_{ON}/I_{OFF} ratio of 10^4, a positive threshold voltage of 0.15 V, and a subthreshold slope of $\sim$165 mV/dec were extracted from the transfer characteristics. The interface-trap density is estimated to be $\sim 7-8 \times 10^{12}$ $cm^{-2} \cdot eV^{-1}$ from the subthreshold characteristics of the MOSFET.**

***Index Terms*—Atomic layer deposition (ALD), enhancement mode, MOSFETs.**

I. Introduction

The III–V materials are considered to be promising candidates for future scaled n-channel metal–oxide–semiconductor field-effect transistors (nMOSFETs) due to their high electron mobility. However, the absence of a thermodynamically stable oxide has been the main impediment to the fabrication of enhancement-mode (E-mode) III–V MOSFETs. Consequently, there has been a tremendous effort to search for dielectrics that can effectively passivate the surface of III–V materials and unpin the Fermi level. This includes the use of molecular beam epitaxy (MBE)—grown $Ga_2O_3(Gd_2O_3)$ [1]–[4], employing a-Si and a-Ge interfacial layers [5], [6], sputtered AlON interfacial layer [7], and atomic layer deposition (ALD) of Al_2O_3 [8]–[11]. Nonetheless, the fabrication of high-performance inversion-type E-mode III–V MOSFET still remains challenging due to the stringent interface requirements.

There have been a few demonstrations of GaAs and $In_{0.53}Ga_{0.47}As$ inversion-type nMOSFETs with MBE-grown $Ga_2O_3(Gd_2O_3)$ [2], [3] and ALD Al_2O_3 [9], [12] gate dielectrics, using the gate-replacement scheme. Interestingly, the $In_{0.53}Ga_{0.47}As$ MOSFETs exhibit superior performance to their GaAs counterparts. This observation can be attributed to much lower interface state density of InGaAs with respect to GaAs, which was deduced by measuring the surface recombination velocity at the interface of GaAs and InGaAs with their native oxides [13], [14]. Although the previous reports have demonstrated high-performance E-mode $In_{0.53}Ga_{0.47}As$ nMOSFETs, it should be noted that MOSFET fabrication using the self-aligned process is simpler than the gate-replacement scheme.

The key issue for demonstrating the self-aligned III–V MOSFETs is to maintain the smoothness and electrical quality of the high-κ/III–V interface, in terms of the interface states, while attempting to achieve the highest level of dopant activation in the source/drain (S/D). In this letter, we have initially examined the chemical and electrical characteristics of the interface between an ALD-grown AlN interlayer and $In_{0.53}Ga_{0.47}As$, using X-ray photoelectron spectroscopy (XPS) and capacitance–voltage (C–V) technique, respectively. Aluminum nitride offers several potential advantages, including large bandgap and excellent chemical stability. This attribute makes AlN a good reaction barrier layer between high-κ and channel material. Finally, exploiting the effective passivation of $In_{0.53}Ga_{0.47}As$ surface, using the ALD AlN interlayer, we have demonstrated high-performance self-aligned inversion-type E-mode $In_{0.53}Ga_{0.47}As$ nMOSFETs.

II. Device Fabrication

Device fabrication was started with surface chemical cleaning of the InGaAs layer, using a combination of HF dip and sulfide treatment, where MOS capacitors and MOSFET devices were fabricated on MBE-grown n- and p-type $In_{0.53}Ga_{0.47}As$ layers, respectively, with a doping concentration of 1×10^{17} cm^{-3}. We have recently shown that this chemical cleaning protocol can effectively render the surface properties of GaAs-based materials appropriate for ALD high-κ deposition, diminishing the undesirable interfacial layer between high-κ and GaAs [10]. Next, samples were transferred into the ALD reactor, where 2.5-nm-thick AlN was deposited by alternating tris(dimethylamido) aluminum precursor and NH_3 gas as a coreactant [15]. A 5-nm-thick ALD HfO_2 immediately followed the AlN deposition. High-κ depositions were carried out at temperatures from 200 °C to 250 °C. The samples underwent postdeposition anneal (PDA) at 550 °C for 5 min in N_2 ambient, which is followed by the deposition and patterning of sputtered-TaN metal gate. Next, MOSFET

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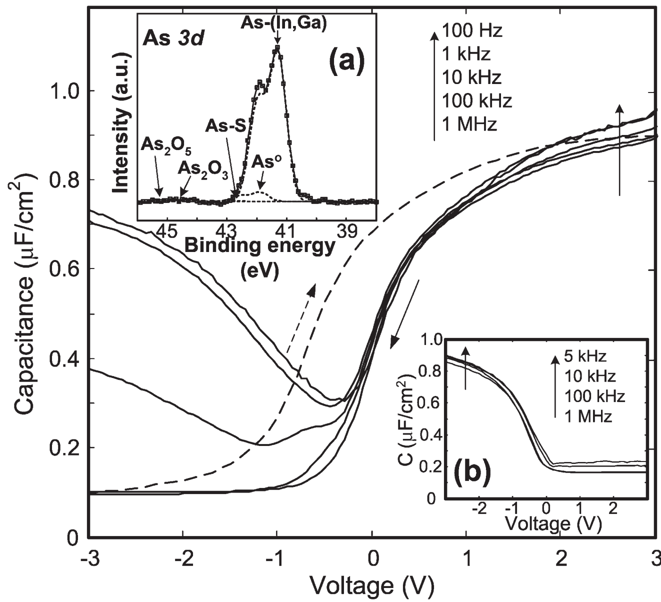

Fig. 1. Frequency dispersion behavior of an InGaAs MOS capacitor fabricated on an n-type substrate. The bidirectional C–V sweeps measured at 1 MHz reveal a hysteresis of ∼670 mV. The inset (a) shows the XPS As $3d$ spectrum of the $\mathrm{AlN/In_{0.53}Ga_{0.47}As}$ interface. The C–V characteristics of a transistor device exhibit a slight degradation of the frequency dispersion behavior, shown as the inset (b).

devices received a silicon implant of 35 keV with a dose of 1×10^{14} cm^{-2} that corresponds to an impurity concentration of $\sim 2 \times 10^{18}$ cm^{-3}. The S/D dopant activation was performed at temperatures ranging from 650 °C to 750 °C for 10–60 s in N_2 ambient. Finally, S/D and backside ohmic contacts were formed by the evaporation of AuGe/Ni/Au $(400/100\ /600)$ and Ti/Au $(250\ /600\ )$ alloys, respectively, followed by rapid thermal annealing at 420 °C for 30 s.

III. Results and Discussion

It is widely believed that the presence of thermally unstable arsenic oxides could possibly cause the Fermi level pinning at the oxide/III–V interface [16]. Therefore, in order to enable the fabrication of inversion-type E-mode III–V MOSFETs, it is crucial to eliminate detrimental native oxides from the high-κ/III–V interface. We have examined the chemical bonding at the AlN/InGaAs interface, using monochromatic XPS. The inset (a) in Fig. 1 shows the As $3d$ spectrum of a sample prior to HfO_2 deposition, where almost no arsenic oxides were detected by XPS. However, the existence of Ga–O and In–O bonds was evidenced by the fitted Gaussian curves to the Ga $2p$ and In $3d$ spectra (data not shown). The capacitance–voltage C–V characteristics of the MOS capacitors, which are fabricated on n-type substrates, were monitored in the dark at different frequencies, showing a fairly high density of interface traps (Fig. 1). The equivalent oxide thickness (EOT) of the capacitors was deduced to be ∼3.8 nm. The bidirectional C–V sweeps measured at 1 MHz, as shown in Fig. 1, indicate a hysteresis of ∼670 mV. Bulk traps and near-interface slow states, in principle, are responsible for the hysteresis in bidirectional C–V sweeps. It is notable that the MOS capacitors exhibit smaller hysteresis after PDA. This could be primarily attributed to further densification of high-κ gate stack by reducing the bulk trap density. Thus, the observed hysteresis after the PDA step could be mainly attributed to near-interface slow traps. The inset (b) in Fig. 1 shows the C–V characteristics of a transistor device, indicating the degradation of frequency dispersion behavior after activation anneal. An EOT of ∼3.9 nm was determined for the transistor device from its C–V data.

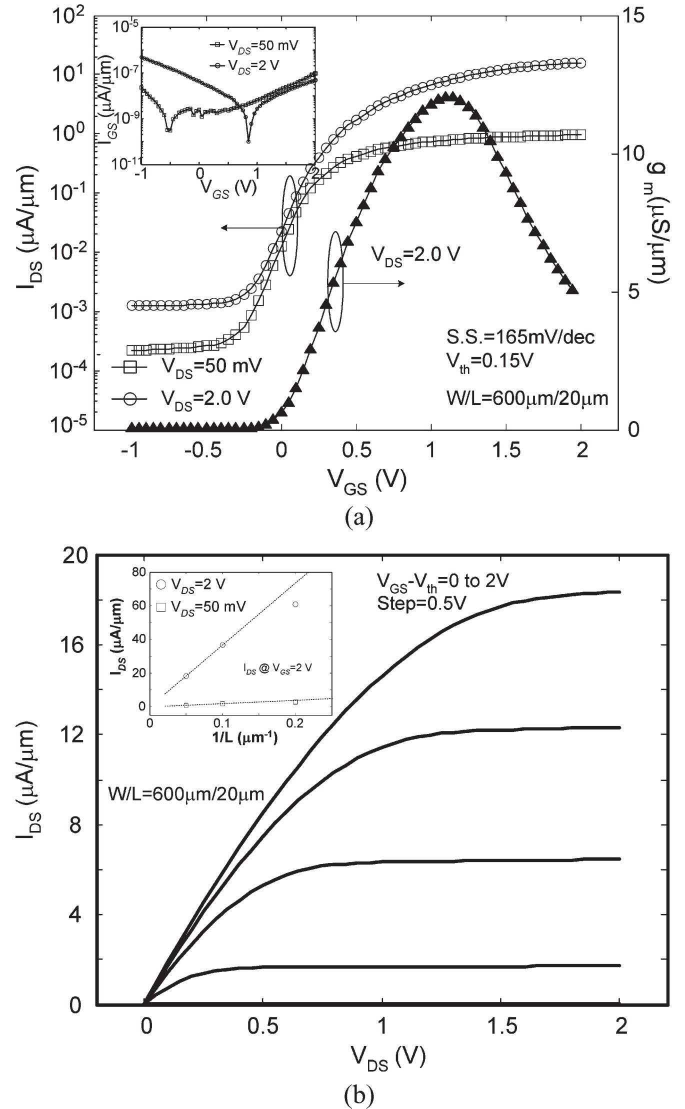

Fig. 2. Measured (a) I_d–V_g and (b) I_d–V_d characteristics of a long channel $\mathrm{In_{0.53}Ga_{0.47}As}$ nMOSFET. The maximum transconductance was determined to be 12.1 mS/mm at a drain voltage of 2 V. The I_{GS}–V_{GS} plot [the inset in (a)] illustrates a very low gate leakage current. It appears that the drive current of shorter channel length devices is more degraded by the large parasitic series resistance, shown as the inset in (b).

We fabricated $\mathrm{In_{0.53}Ga_{0.47}As}$ nMOSFETs employing the same gate stack, using a ring-FET geometry consisting of an annular gate, in order to simplify the device isolation process. Fig. 2(a) shows the transfer characteristics of an nMOSFET with a gate length of 20 μm. An $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of $\sim 10^4$ and a subthreshold slope (S.S.) of 165 mV/dec were determined from the I_d–V_g plot. The interface-trap density (D_{it}) with the assumption of uniform distribution in the upper bandgap

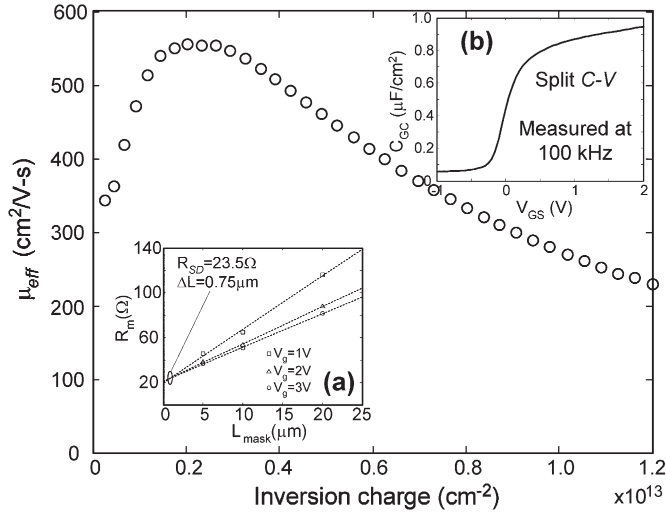

Fig. 3. Effective electron mobility was deduced at a drain voltage of 50 mV, using the I_d–V_g plot shown in Fig. 2(a). The inset (a) shows the R_m versus L_{mask}, as a function of gate voltage. A S/D series resistance of 23.5 Ω was extracted from the plot. The inset (b) shows the corresponding split C–V of the MOSFET device, confirming the formation of inversion layer.

is estimated to be $\sim$7–8×10^{12} $\mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$, using the following [17]:

$$S = 2.3 \times (kT/q)\,[1 + (C_D + C_{\mathrm{it}})/C_{\mathrm{ox}}] \qquad (1)$$

where C_D, C_{it}, and C_{ox} are the depletion capacitance, the interface-trap capacitance, and the gate capacitance, respectively. A threshold voltage of 0.15 V was extracted by a linear extrapolation technique. A maximum transconductance (G_m) of 12.1 mS/mm was obtained for the device at a drain voltage of 2 V, as shown in Fig. 2(a). The inset in Fig. 2(a) shows the corresponding I_{GS}–V_{GS} characteristics of the device, indicating a very small gate leakage current. The output characteristics of the MOSFET device are shown in Fig. 2(b), where a maximum drain current of 18.5 μA/μm was obtained at a gate overdrive of 2 V. It is notable that the drain current sublinearly increases with gate bias for gate overdrives larger than 1 V. This could be caused by a strong dependence of the mobility on the transverse electric field [17]. This gate-bias dependence of the drive current can be clearly observed from the previous reports on GaAs-based field-effect transistors [1], [9]. From the slope of the I_d–V_d curves in the linear region, it is also evident that these devices suffer from a relatively high S/D series resistance. As a result, the drive current of shorter channel length devices is more degraded by the large parasitic resistance, shown in the inset in Fig. 2(b). It should be noted that the poor thermal stability of InGaAs tends to limit the total thermal budget of the fabrication process. This, coupled with the fact that the highest obtainable impurity concentration in III–V materials is in the range of 10^{18}–10^{19} cm^{-3}, could severely degrade the S/D series resistance. Hence, further improvement of drive current should be achievable by optimizing S/D ohmic contacts and implantation/activation conditions. The S/D series resistance (R_{SD}) and the difference between the mask-defined gate length and the effective channel length $(\Delta L = L_{\mathrm{mask}} - L_{\mathrm{eff}})$ were determined to be 23.5 Ω and 0.75 μm, respectively, from the plot of $R_m (= V_{\mathrm{DS}}/I_d)$ versus different L_{mask} values, as a function of gate voltage [the inset (a) in Fig. 3]. R_m values were evaluated at a drain voltage of 100 mV to ensure the device operation in the linear region. The effective electron mobility (μ_{eff}) was evaluated for the same device from the I_d–V_g plot (measured at a drain voltage of 50 mV) and its corresponding split C–V [the inset (b) in Fig. 3]. A high interface-trap density, which is deduced from the subthreshold characteristics of this device, could be the major cause of the mobility degradation, as well as the poor S.S.

IV. Conclusion

In summary, we have demonstrated the self-aligned inversion-type E-mode $In_{0.53}Ga_{0.47}As$ nMOSFETs, using an ALD-grown AlN interfacial layer. An interface-trap density of $\sim$7–$8 \times 10^{12}/\mathrm{cm}^2 \cdot \mathrm{eV}$ was estimated from the subthreshold model. A maximum drive current of 18.5 μA/μm was achieved at a gate voltage of 2 V for a MOSFET device with a gate length of 20 μm. An $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of 10^4 and an S.S. of $\sim$165 mV/dec were extracted from the I_d–V_g plot. However, further improvement of drive current should be achievable by optimizing S/D activation and ohmic contact.

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