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Hall mobility measurements in enhancement-mode GaAs field-effect transistors with Al_2O_3 gate dielectric

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We report the direct measurement of the inversion charge density and electron mobility in enhancement-mode n-channel GaAs transistors using gated Hall bars. The Hall data reveal the existence of a reduced mobile charge density in the channel due to significant charge trapping. The peak electron mobility was found to be relatively high ($\sim$2140 $cm^2/V\,s$), in agreement with inherent high carrier mobility of electrons in III-V materials. © *2010 American Institute of Physics*. [doi:10.1063/1.3521284]

Although fabrication of enhancement-mode (E-mode) III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) has been pursued for several decades,[1–3] recently there has been renewed interest in exploring these materials as potential candidates for post-Si complementary metal-oxide-semiconductor applications.[4] However, passivation of the interface between gate dielectric and III-V-channel materials has long been a key challenge to realize III-V MOSFETs. This, in turn, has driven the research to develop various schemes for interface passivation of III-V materials.[5–16] Carrier mobility is a main figure of merit used to benchmark the MOSFET performance, and, therefore, it is important for the carrier mobility to be evaluated accurately. For example, charge trapping in Si MOSFETs with high-k gate dielectrics can result in the overestimation of inversion charge (Q_{inv}) using conventional split capacitance-voltage (*C-V*) method[17] and charge trapping can influence the calculated effective mobility by distorting the threshold voltages in the measured split *C-V* and I_d-V_g curves.

Despite current progress in passivation of high-k/III-V interface, the reported device characteristics indicate the presence of significant charge traps.[5–15] Therefore, to determine the carrier mobility in III-V MOSFETs with high-k gate dielectrics, a direct measurement of Q_{inv} is necessary. Recently, there have been efforts to decouple the contribution of interface traps from the split *C-V* data for mobility extraction in $In_{0.53}Ga_{0.47}As$ MOSFETs either by conducting the *C-V* measurements at low temperatures[18] or by analyzing the small signal response of the inversion layer using a comprehensive equivalent circuit model.[19] In this work, we use gated Hall bars (GHBs) to directly measure Q_{inv} and mobility in E-mode GaAs-channel MOSFETs with Al_2O_3 gate dielectrics.

Figure 1 shows schematically the GHB structure. The fabrication process for the GHB devices is similar to our previous paper, reporting the fabrication of self-aligned E-mode GaAs n-MOSFETs.[10] The GHB transistors were fabricated on (001) undoped semi-insulating GaAs substrates (carbon doped, resistivity $\geq 1\times10^8$ Ω cm, bulk mobility $\geq$4000 $cm^2/V\,s$). After an *ex situ* wet clean process using a combination of dilute hydrofluoric acid dip and sulfur passivation in $(NH_4)_2S$,[20] the samples were immediately transferred to an atomic layer deposition (ALD) reactor. Then, an 8.1 nm thick Al_2O_3 layer was grown using trimethylaluminum precursor, which has been shown to effectively reduce the thickness of GaAs native oxides at the high-k/GaAs interface.[20–23] Next, TaN metal gate was sputtered and patterned. Active areas were defined prior to Si implantation in order to isolate the source/drain (S/D) regions and sensing voltage areas. The Si implantation was performed at 35 keV with a dose of 1×10^{14} cm^{-2}, followed by S/D activation at 800 °C. Finally, AuGe/Ni/Au Ohmic contacts were evaporated and annealed at 450 °C in N_2 ambient.

The Hall resistance was measured using small amplitude (100 nA), low frequency current flown from source to drain. The magnetic field was swept from −0.3 to 0.3 T while the transverse ($V_{xy}=V_1-V'_1$) and longitudinal ($V_{xx'}=V_2-V_1$) voltages were measured at different gate voltages using low frequency lock-in techniques.

The typical I_d-V_g characteristics of the GaAs transistors with a gate length of 20 μm are shown in Fig. 2. The inset

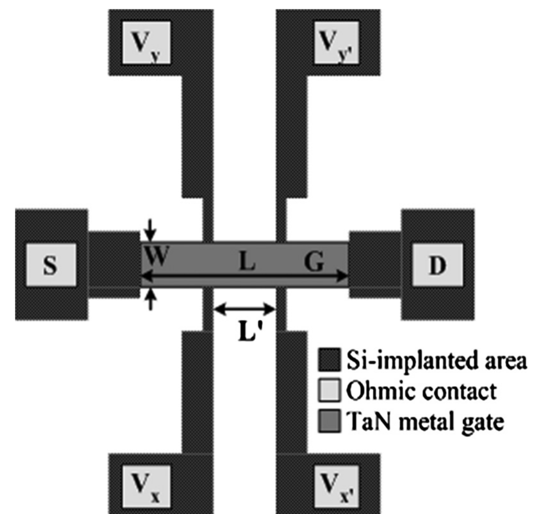

FIG. 1. The schematic illustration of a GHB structure.

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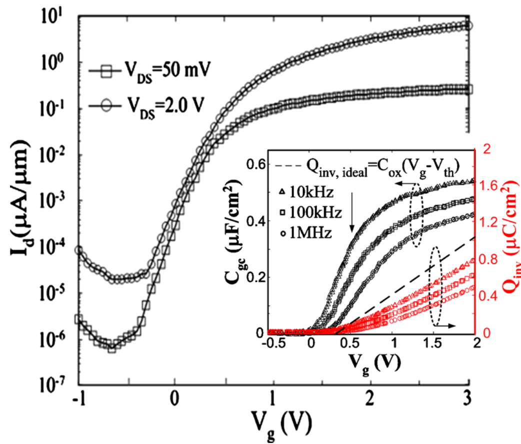

FIG. 2. (Color online) The typical I_d-V_g characteristics of a GaAs MOSFET with a gate length of 20 μm. The inset shows the corresponding split *C-V* data and the extracted Q_{inv}, manifesting noticeable frequency dispersion.

of Fig. 2 shows the split *C-V* curves and their corresponding Q_{inv}. The strong frequency dispersion of the *C-V* data indicates the presence of fast traps. The dispersion of the *C-V* data by itself renders the conventional effective mobility extraction by split *C-V* method unreliable due to the frequency dependence of the extracted Q_{inv}. The dispersion in split *C-V* data can be also seen in several other reports for III-V MOSFETs,[5–8,18,19] revealing the importance of a direct Q_{inv} measurement. The interface state density (D_{it}) of the devices was estimated from the subthreshold slope model[24] (assuming a uniform distribution of D_{it} in the upper half of the bandgap for n-MOSFETs) to be $\sim 1\times 10^{12}$ $cm^{-2}\,eV^{-1}$. In addition to the interface state traps, slow "border traps"[25,26] further degrade the current, confirmed by pulsed *I-V* measurements. Figure 3(a) shows the typical pulsed *I-V* behavior of our devices for two different pulsed widths. The initial fast drop of the current is due to fast traps. As can be also seen, increasing the charging time results in higher degradation of the drain current. The inset shows the schematic illustration of the pulsed *I-V* setup. Furthermore, the logarithmic time dependence of the V_{th} shift (and the drain current degradation in the linear transistor operation regime) is a direct indication of charge trapping in the high-k dielectric, shown in Fig. 3(b). As will be discussed, the presence of the slow traps can further complicate the determination of the channel mobility.

To determine the density of mobile electron charges in the channel, Hall measurements were carried out using the GHB structures. The bottom right inset of Fig. 4(a) shows the timing diagram used for the Hall measurements. This is to primarily alleviate the effect of slow traps during the Hall and four-point measurements. The 60 s hold time after applying V_{gs} and I_d, and before sweeping the magnetic field (B), is to fill the majority (more than 95%) of the traps that will otherwise respond during the magnetic field sweep, where the V_{xy} and $V_{xx'}$ voltages are measured. Figure 4(a) illustrates the Hall resistance ($R_H=V_{xy}/I$) as a function of magnetic field for a GaAs GHB, measured at two different gate bias voltages. The linearity of the R_H-B curves indicates negligible charge trapping after the hold time. We note that the R_H-B curve does not pass through the origin due to the mixing between $V_{xx'}$ and V_{xy}, which can result from rotational misalignment between the pads and/or inhomogeneity

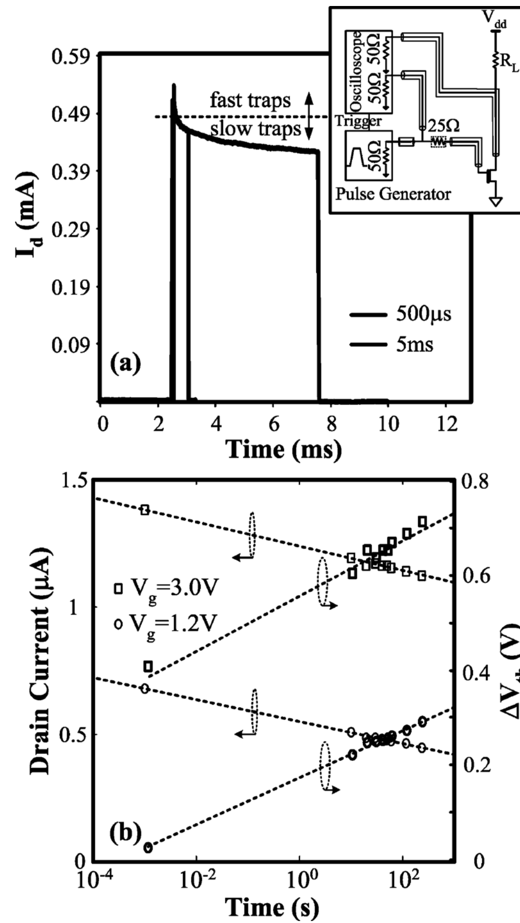

FIG. 3. (a) The typical pulsed *I-V* behavior of our GaAs devices for two different pulse widths, confirming the presence of fast and slow traps. The inset shows the schematic illustration of the pulsed *I-V* setup. (b) The representative logarithmic time dependence of the V_{th} shift and the drain current degradation for a GaAs device, indicating charge trapping by border traps in the ALD-Al_2O_3.

in the inversion layer. However, this does not influence the extracted Q_{inv} as the charge density is evaluated from the slope of R_H-B curve using $N_{inv}=(Q_{inv}/q)=(dR_H/dB)^{-1}/q$, where q is the electronic charge (inset of Fig. 5). The Hall

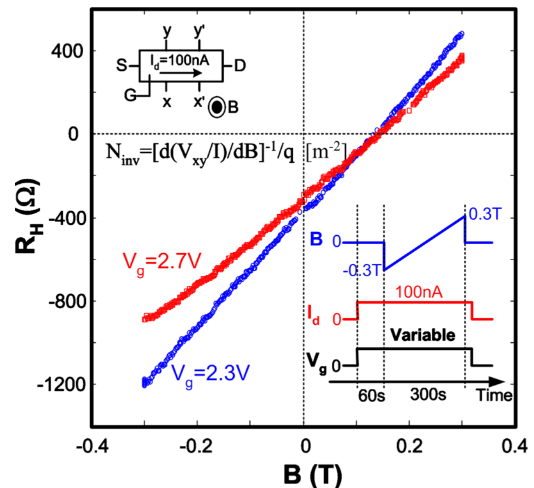

FIG. 4. (Color online) The representative R_H-B characteristics for two different V_g values. The inset illustrates the Hall measurement scheme as well as the timing diagram for the test based on which the GHB measurements were carried out.

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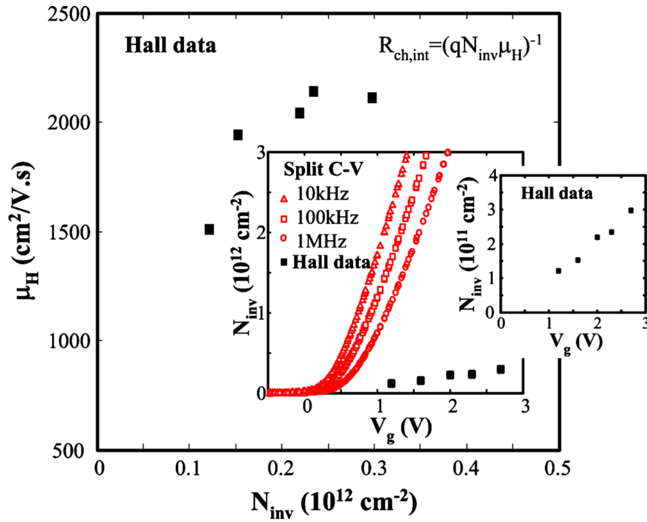

FIG. 5. (Color online) Measured Hall mobility as a function of N_{inv}. The inset compares the density of measured true mobile charges in the channel with the extracted N_{inv} from the split *C-V* data. The data indicate a relatively low mobile charge density due to significant charge trapping.

data show a relatively low N_{inv} by comparison to the expected values from split *C-V* data, revealing significant charge trapping in our GaAs transistors. Nevertheless, unlike the split *C-V* data, which are contaminated by the effect of charge traps, the measured N_{inv} by the Hall measurements is the true mobile charge density in the channel.

Another advantage of the GHB structure is the elimination of the parasitic effect of the source/drain series resistance on the extracted mobility through four-point measurements. As a result, the intrinsic channel resistance $[R_{ch,int} = V_{xx'}/I_d = (qN_{inv}\mu_n)^{-1}]$ was directly measured at different gate voltages. The mobility was evaluated using the extracted mobile charge density in the channel at different gate voltages via Hall measurements, in combination with the corresponding intrinsic channel resistance, shown in Fig. 5. The peak Hall channel mobility was measured to be ~ 2140 cm²/V s, consistent with the high intrinsic electron mobility of GaAs. The high mobility of electrons may stem from the screening of the scattering sites created by the fast interface states during the Hall mobility measurements. The sufficiently long hold time of 60 s allows the majority of traps to be filled by electrons prior to the sweep of the B-field. Therefore, the Hall mobility measured by this technique indicates the intrinsic mobility of electrons in the channel in the absence of interface traps.

It is notable that the field-effect mobility for our devices (extracted from the slope of their corresponding I_d-V_g curves assuming ideal MOSFET equations) was found to be much lower ($\mu_{FE} \sim 100$ cm²/V s). These data indicate that substantial charge trapping can be the major cause for the significant degradation of the dc characteristics of our high-k III-V transistors, as well as in many other reports in the literature. Furthermore, the normalized drain current of our devices with respect to the channel length, oxide capacitance (C_{ox}), and gate overdrive is comparable to the recent reports for GaAs MOSFETs.[5–13] Therefore, the findings of this study can explain the relatively low drive current of these devices.

In summary, we demonstrated that charge trapping significantly impacts the mobility extraction using the conventional split *C-V* method. To overcome this issue, we have directly measured the inversion charge density and the corresponding intrinsic channel mobility for self-aligned inversion-type E-mode high-k GaAs transistors using gated Hall bars. The high mobility of mobile charges in the channel measured using this technique suggests that charge trapping significantly degrades the performance of our high-k III-V transistors.

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[1]T. Mimura, K. Odani, N. Yokoyama, Y. Nakayama, and M. Fukuta, IEEE Trans. Electron Devices **ED-25**, 573 (1978).
[2]F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, Solid-State Electron. **41**, 1751 (1997).
[3]F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsai, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, IEEE Electron Device Lett. **19**, 309 (1998).
[4]International Technology Roadmap for Semiconductors (ITRS), 2006 update; available at www.itrs.com.
[5]I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, Tech. - Dig. Int. Electron Device Meeting 2006, p. 829.
[6]H.-C. Chin, M. Zhu, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, IEEE Electron Device Lett. **29**, 553 (2008).
[7]H.-S. Kim, I. Ok, F. Zhu, M. Zhang, S. Park, J. Yum, H. Zhao, and J. C. Lee, Conf. Dig. - Device Research Conference 2007, p. 99.
[8]M. Xu, K. Xu, R. Contreras, M. Milojevic, T. Shen, O. Koybasi, Y. Q. Wu, R. M. Wallace, and P. D. Ye, Tech. - Dig. Int. Electron Device Meeting 2009, p. 865.
[9]H.-C. Chin, M. Zhu, X. Liu, H.-K. Lee, L. Shi, L.-S. Tan, and Y.-C. Yeo, IEEE Electron Device Lett. **30**, 110 (2009).
[10]D. Shahrjerdi, T. Akyol, M. Ramon, D. I. Garcia-Gutierrez, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **92**, 203505 (2008).
[11]F. Gao, S. J. Lee, and D. L. Kwong, J. Vac. Sci. Technol. B **27**, 214 (2009).
[12]Y. Q. Wu, Y. Xuan, T. Shen, P. D. Ye, Z. Cheng, and A. Lochtefeld, Appl. Phys. Lett. **91**, 022108 (2007).
[13]H. Zhao, D. Shahrjerdi, F. Zhu, M. Zhang, H.-S. Kim, I. OK, J. H. Yum, S. Park, S. Banerjee, and J. C. Lee, Appl. Phys. Lett. **92**, 233508 (2008).
[14]Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, Tech. - Dig. Int. Electron Device Meeting 2007, p. 637.
[15]N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C. K. Gaspe, M. B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, Tech. - Dig. Int. Electron Device Meeting 2008, p. 363.
[16]R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, IEEE Electron Device Lett. **28**, 1080 (2007).
[17]W. Zhu, J.-P. Han, and T. P. Ma, IEEE Trans. Electron Devices **51**, 98 (2004).
[18]C. L. Hinkle, A. M. Sonnet, R. A. Chapman, and E. M. Vogel, IEEE Electron Device Lett. **30**, 316 (2009).
[19]A. Ali, H. Madan, S. Koveshnikov, and S. Datta, IEEE Trans. Electron Devices **57**, 742 (2010).
[20]D. Shahrjerdi, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **91**, 063501 (2007).
[21]M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, Appl. Phys. Lett. **86**, 152904 (2005).
[22]M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **87**, 252104 (2005).
[23]C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, Appl. Phys. Lett. **92**, 071901 (2008).
[24]B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices* (Prentice Hall, Upper Saddle River, NJ, 1999), p. 302.
[25]E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett. **96**, 012906 (2010).
[26]D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, J. Appl. Phys. **73**, 5058 (1993).

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