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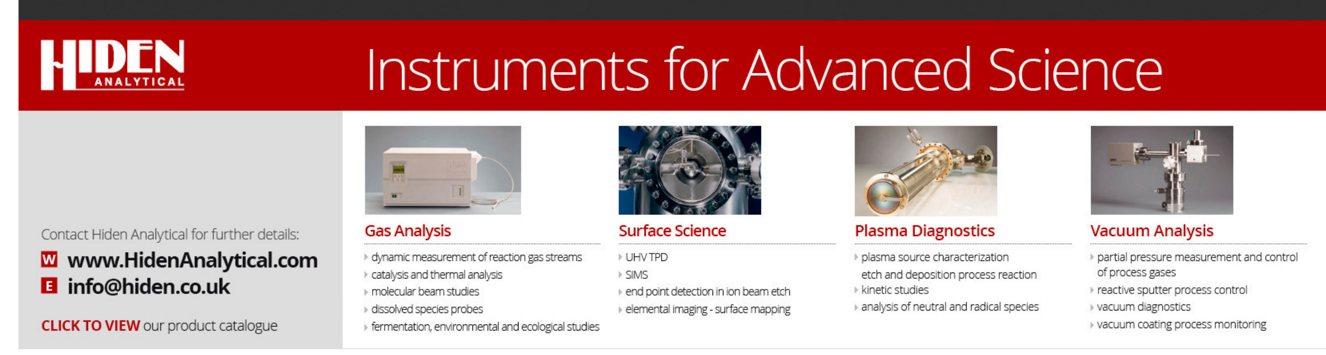

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Low temperature crystallization of germanium on plastic by externally applied compressive stress

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The conventional Cu-induced crystallization of *a*-Ge has been facilitated by different types of external stress mechanically applied to the flexible substrate. It has been observed that in the case of compressive stress, crystallization becomes possible at temperatures as low as 130 °C and evolves as stress becomes more stringent. High electrical conductance and a hole mobility of 110 $cm^2/V\,s$ show the crystallinity of the Ge film, further confirmed by x-ray diffraction, scanning electron microscopy, and transmission electron microscopy analyses. The temperature of the annealing process (between 130 and 180 °C) expedites the process (from 6 to 1 h) as it is increased, but the principal mechanism seems to be independent of temperature. Temperatures higher than 180 °C are detrimental to the plastic substrate, polyethylene terephthalate. Evolution of cracks in Ge layer has been studied as the main consequence of the interfacial stress between Ge layer and substrate. The crack density was minimized by patterning the *a*-Ge layer before annealing. The main explanation of the physical phenomenon accounting for crystallization is believed to be the externally applied compressive stress, which reinforces the inherently present internal stress between the layer and the substrate. © *2003 American Vacuum Society.*
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I. INTRODUCTION

Crystallization of amorphous semiconductors such as silicon and germanium has been seriously investigated because of its wide range of applications in microelectronics. An important concern in this field is the temperature of crystallization. It has been known for a long time that certain metals can reduce the crystallization temperature if they are in contact or alloyed with the semiconductor. Methods such as metal-induced crystallization (MIC) and metal induced lateral crystallization have been proposed.[1–3] Al-induced crystallization of *a*-Ge has been studied by forming sandwiched multilayers of Al/Ge.[4–7] The crystallization temperature is lowered to about 100 °C by increasing the percentage of the Al involved, which adversely degrades the semiconductor properties because of considerable metal contamination. If the temperature is increased to 200 °C or higher, crystallization can take place with smaller percentage of Al. Cu-induced crystallization of *a*-Ge at 400 °C has also been reported.[8,9]

On the other hand, stress-induced interactions between substrate and layer or between layers has been a subject of study in previous works. It is generally believed that the rate of nucleation and crystal growth is higher at locations where the periodic crystal structure is terminated to internal dislocations or interface defects, mainly due to the local stress fields. It has been reported that crystallization of *a*-Si starts at the interface between the *a*-Si film and the glass substrate, indicating the driving force of stress caused by the difference in the thermal expansion coefficient between *a*-Si and glass, leading to preferential nucleation along SiO_2 steps in *a*-Si.[10] On the other hand, there are some reports on the suppressing effect of the interfacial stress on the rate of crystallization and that nucleation starts at the surface of the *a*-Si rather than the interface, when a biaxial stress is induced from the fused silica substrate[11] or from an overlayer such as a $Si_3\,N_4$ cap.[12] In the case of MIC, while the basic mechanism is still a subject of study, it has been recently claimed that compressive stress and lattice shrinkage caused by the introduced metal is the principal factor in Al-induced crystallization of *a*-Ge.[13] Although there is no kind of established technique to manipulate the internal or external stresses in order to enhance the crystallization of semiconductors, such techniques are widely used in the area of polymer research and technology, such as the stress-induced crystallization of polyethylene composites.[14]

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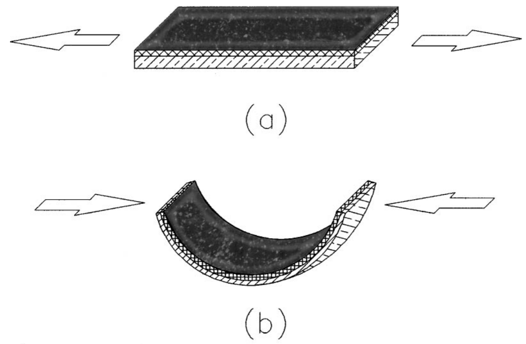

FIG. 1. Schematic setup for applying mechanical stress: (a) stretching the sample for applying tensile stress and (b) bending the sample inward for applying compressive stress.

In this article, a stress-assisted Cu-induced crystallization method of Ge is presented, which not only puts forth the chance of low metal contamination, but also is performed at temperatures as low as 130 °C. This temperature is suitable for flexible substrates and potentially leads to a variety of diverse applications, such as low temperature crystallization of Si–Ge alloys and fabrication of high mobility thin film transistors (TFTs) on plastic. The main idea of this work is reducing the crystallization temperature by mechanically applying a uniaxial compressive stress to the substrate, which will be consequently transferred to the layer via the interface.

II. EXPERIMENT

Polyethylene terephthalate (PET) films with a thickness of 100 μm have been used as the main substrates. All depositions were performed in vacuum chamber at a temperature of 100 °C and a base pressure of 1×10^{-6} Torr. A sandwiched structure of Ge/Cu/Ge with a thickness of 500 Å/10 Å/500 Å was formed by *e*-beam deposition of Ge and thermal deposition of Cu. The prepared samples then have been treated with different types of mechanical stress, and annealed at different temperatures in the range of 130–180 °C. Compressive stress was applied by bending the flexible substrate inward, while applying tensile stress was performed by stretching the substrate. The amount of stress was evaluated by the correspondent strain, both for compressive and tensile stress. Applied $\Delta L/L$ was measured directly for tensile stress, whereas inward curvature was used to assess the equivalent $\Delta L/L$ for compressive stress. A simple schematic is depicted in Fig. 1 to demonstrate the experimental setup briefly.

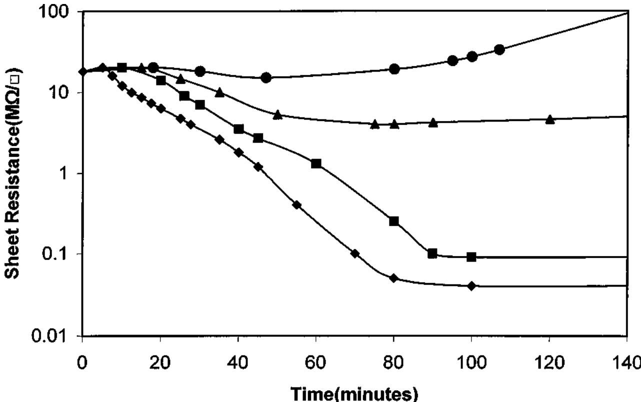

FIG. 2. Variations in electrical sheet resistance versus time for samples with different treatments, in a semi-logarithmic plot.(△) marks indicate data for mere annealing, (○) marks indicate 0.1% equivalent tensile strain, (□) and (◇) indicate 0.03% and 0.05% equivalent compressive strain, respectively.

III. RESULTS AND DISCUSSION

The change of electrical sheet resistance has been continuously monitored during annealing at a constant temperature of 150 °C and plotted in Fig. 2. Three types of treatment have been carried out while annealing, applying tensile stress with a strain of 0.1% and applying compressive stress with two different amounts of strain, 0.03% and 0.05%. Mere annealing of another sample was also performed for comparison. All samples have an initial sheet resistance of 17 MΩ/□. An initial increase to about 20 MΩ/□ is observed in all of the curves. This increase is mainly due to the primary diffusion of Cu in Ge. After this slight increase, sheet resistance begins to decrease. When no stress is applied, the curve stops dropping at 4 MΩ/□. In the case of tensile stress, a considerable increase in resistance follows the small drop. For the other two curves, applying compressive stress has led to a drastic drop of electrical sheet resistance by more than 2 orders of magnitude. Final sheet resistance for samples with 0.05% and 0.03% strains is 25 and 80 kΩ/□, respectively.

The final hole mobility of mentioned Ge samples has been determined by Hall measurement; that is 2.8 cm^2/V s before annealing and reaches 5.9 cm^2/V s after annealing without external stress. Parallel to conductivity enhancement, the mobility is increased by 2 orders of magnitude from the no stress case to a maximum of 110 cm^2/V s in the compressive stress case with 0.05% strain. This maximum mobility is higher than that with 0.03% strain (85 cm^2/V s), further indicating the effect of compressive stress in improving the crystallization.

The scanning electron microscopy (SEM) micrograph of a sample annealed for 60 min in 150 °C with 0.05% compressive strain is given in Fig. 3. The graph shows that grains of polycrystalline Ge are initially grown at locations where compressive strain is more densely accumulated, as evidenced by the presence of buckling. This feature verifies the assistance of stress in growth of Ge grains. Figure 4 shows the SEM micrograph of another sample annealed with the same conditions for 100 min. Grains of polycrystalline Ge are distributed on the surface with an average size of 0.2 μm. This graph is taken from a part of the sample where no buckling exists, so it can be anticipated that compressive stress has a nearly homogenous distribution. This surface morphology indicates the crystallinity of the layer, justifying increase in mobility.

X-ray diffraction (XRD) analysis was also performed for the mentioned sample after 100 min of annealing (Fig. 5). PET is partially crystalline, with a high peak located at $2\theta=26°$ and another peak at $2\theta=54°$. The potential ⟨111⟩ Ge peak is buried in this rather high peak of the substrate. The

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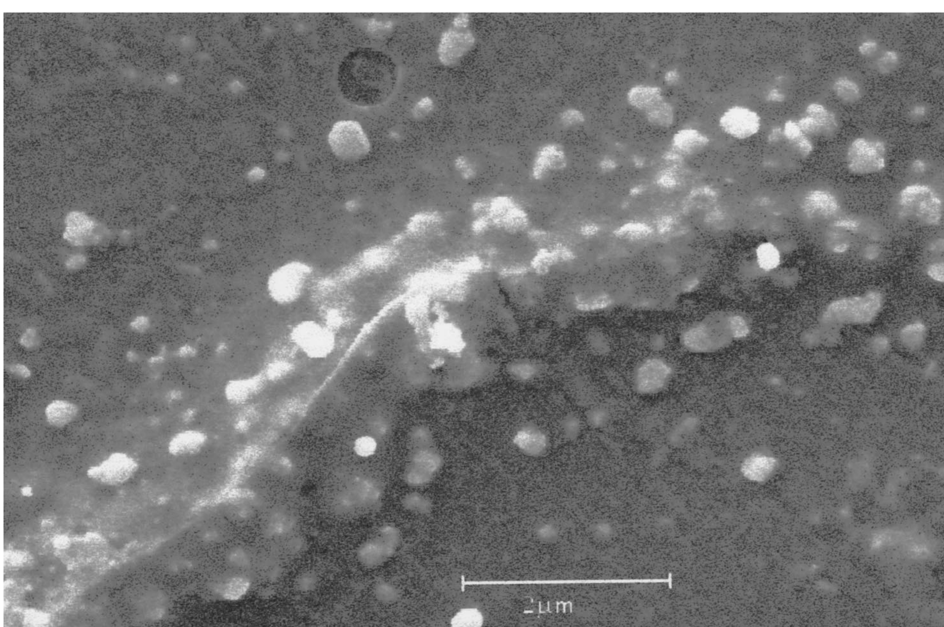

FIG. 3. SEM micrograph showing the presence of grains in the vicinity of buckling features.

⟨400⟩ and especially the ⟨220⟩ orientation of polycrystalline Ge is easily discernible in the spectrum. Transmission electron microscopy (TEM) analysis of this sample also reveals the polycrystalline structure of the Ge layer. The diffraction pattern is given in the insert of the figure. Specimen preparation for TEM has been done by partial chemical etching of PET, followed by cutting the desired area to expose the Ge layer.

The evolution of cracks in Ge layer would be an important concern for practical application. Fig. 6 shows the SEM graph of parallel cracks formed in the Ge layer. These cracks are located at about 50 μm separations from each other. Such buckling features are signs of interfacial compressive stress. Further accumulation of strain causes the Ge layer to peel off, seriously degrading the electrical properties of the layer. This problem is considerably alleviated by patterning the *a*-Ge layer before annealing, as shown in Fig. 7. As the SEM graph shows, buckling is completely eliminated in 50, 75, and 100 μm squares, while 125 and 150 μm squares are still attacked by cracks.

Similar mechanical treatments were performed at other temperatures between 130 and 180 °C. PET is deformed and then severely damaged at temperatures higher than 180 °C. The basic electrical behavior of these samples is analogous in the mentioned temperature range and principally like Fig. 1, however the whole annealing time needed for crystallization process must be increased from one hour at 180 °C to 6 h at 130 °C. Crystallization nearly stops for lower temperatures. The variation of electrical sheet resistance at a constant equivalent compressive strain of 0.05%, for three annealing temperatures of 130, 150, and 180 °C is plotted in Fig. 8. This plot proposes that the major delay resulted by temperature reduction occurs in the initial behavioral regime of re-

FIG. 4. SEM micrograph showing the morphology of grains after treatment with 0.05% equivalent compressive strain, for 100 min of annealing in 150 °C.

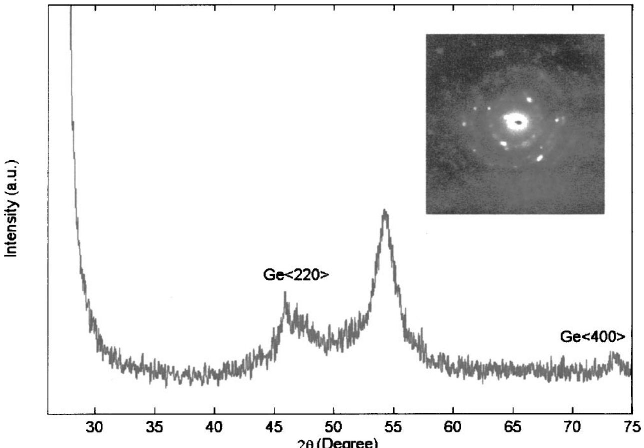

FIG. 5. X-ray diffraction spectrum for the sample treated with compressive stress corresponding to 0.05% strain. ⟨220⟩ and ⟨400⟩ peaks of Ge film are clearly observed in the picture. The inset shows the TEM diffraction patterns of the mentioned sample.

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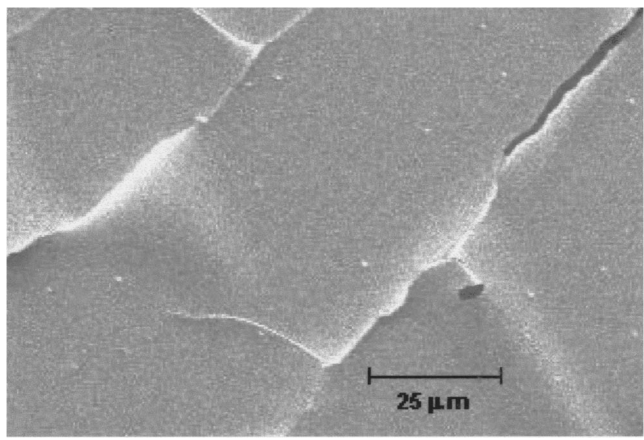

FIG. 6. SEM graph depicting the progressive formation of parallel cracks in Ge coating. Cracks are located at about 50 μm separations from each other.

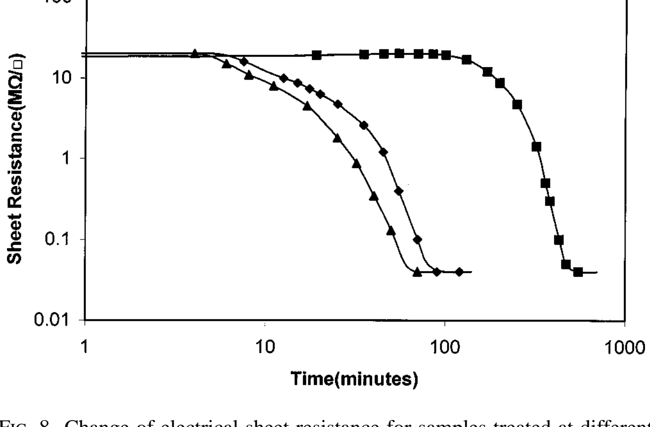

FIG. 8. Change of electrical sheet resistance for samples treated at different temperatures in constant equivalent compressive strain of 0.05%. (△), (◇), and (□) represent data for 180, 150, and 130 °C, respectively.

sistance variation. This includes the preliminary slight increase caused by diffusion, which exponentially depends on temperature, and also at the first parts of the following resistance drop. Referring to Fig. 3, it can be concluded that the mentioned part of drop pertains to the initial formation of grains, especially at the locations of densely accumulated strain, where temperature plays a considerable role in making the initial growth feasible. The final stage of conductivity enhancement seems to have a little dependence on temperature and is completed only in the case of compressive stress, leading to the final crystallization of the Ge layer.

IV. SUMMARY AND CONCLUSION

In summary, stress-assisted Cu-induced crystallization of *a*-Ge has been presented and effects of external stress and specially the compressive one have been discussed and verified by XRD, SEM, TEM, and Hall mobility measurement.

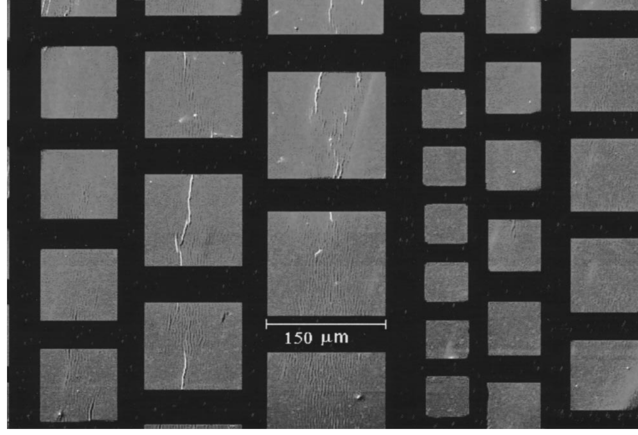

FIG. 7. SEM graph showing surface morphology of cracks after treating the patterned Ge coating. Squares with lengths of smaller than 125 μm are almost free from cracks.

The results of this study are consistent with the claims of a previous work[11] in which the compressive stress and lattice shrinkage caused by the introduced metal, has been known as the main driver of MIC. In the present work, external compressive stress has been applied to reinforce the internal one and finally compensate for a considerable temperature reduction. We are currently using this method to fabricate pure Ge thin film transistors on plastic and possibly extend it to realize Si–Ge TFTs.

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