JVSTA Journal of Vacuum Science & Technology A

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Citation: Journal of Vacuum Science & Technology A **22**, 856 (2004); doi: 10.1116/1.1705581
View online: http://dx.doi.org/10.1116/1.1705581
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvsta/22/3?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Low-temperature stress-assisted germanium-induced crystallization of silicon–germanium alloys on flexible polyethylene terephtalate substrates

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(Received 12 September 2003; accepted 23 February 2004; published 17 May 2004)

The application of mechanical-compressive stress during low-temperature annealing has been investigated for the crystallization of SiGe alloys on plastic substrates. It was observed that crystallization of an amorphous Ge/Cu/Ge ''sandwich'' can occur at temperatures as low as 130 °C with the application of an equivalent compressive strain of 0.05%. By using this sandwich as a seed for crystallization of an underlying amorphous SiGe film, partial crystallization of the film was observed to occur at a temperature of 180 °C, again under an equivalent compressive strain of 0.05%. Without the application of the compressive strain, crystallization was not observed for either system at the temperatures investigated. The atomic percentage of Si in the SiGe alloy was 35% as confirmed by Rutherford backscattering spectroscopy and the partial crystallization of the SiGe layer was verified by scanning electron microscopy, x-ray diffraction, and transmission-electron microscopy analyses. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1705581]

I. INTRODUCTION

The realization of conventional silicon-based electronic circuits onto flexible plastic substrates offers unique opportunities for the development of new technologies, particularly in the field of flexible displays. Some of the advantages to using plastic substrates are: potential for large-area coverage, lightweight durable mechanically flexible circuits, low-cost solution-based printing techniques and rapid, high-volume reel-to-reel processing.[1] However, one of the limitations to the widespread application of plastic substrate electronics is the requirement for low-temperature processing steps that will not thermally degrade the plastic substrates. In particular, one of the highest temperature processes is the crystallization of the semiconductor layers, a critical step in the fabrication of high-performance devices. With respect to the application of thin-film transistors (TFTs) for use as drivers in flexible displays, the driving power of the TFTs is directly proportional to the field-effect mobility, in turn requiring a device-quality polycrystalline layer in the channel region.[2] Therefore, there has been increasing interest in the development of low-temperature crystallization methodologies.

One well-known method that considerably reduces the crystallization temperature of semiconductors is metal-induced crystallization (MIC).[3] Some examples of MIC of Si and Ge that have been reported recently include: Al-induced crystallization of Ge,[4–6] Cu-induced crystallization of Ge,[7,8] and Ni-induced lateral crystallization of Si.[9] Since the crystallization temperature of Ge is lower than Si, Ge is typically the first material to be considered for low-temperature crystallization applications. Unfortunately, Al-MIC of Ge can significantly degrade the properties of the semiconductor,[4–6] and although Cu-MIC of Ge can lead to excellent device properties, process temperatures as high as about 400 °C are required.[7,8] Therefore, additional techniques are required to further reduce the crystallization temperature.

One promising technique is the application of stress during the growth and/or annealing steps. For example, it has been reported that stresses induced by the difference in the thermal expansion coefficient between Si and SiO_2 might lead to preferential nucleation of Si along SiO_2 steps.[10] Furthermore, the microscopic mechanism accounting for MIC has been investigated and believed to be related to the internal compressive stress induced by the lattice shrinkage imposed by the introduced metal.[11] If internal stresses can lead to reduced crystallization temperatures, it appears reasonable that the application of an external mechanical stress could have a similar effect. This hypothesis has been proven correct for Ge, and in a previous work we were able to demonstrate a reduction in the crystallization temperature of conventional Cu-MIC to 130 °C in the presence of mechanical compressive stress externally applied to the flexible substrate by inward bending.[12] High-quality depletion-mode poly-Ge TFTs were fabricated on flexible polyethylene terephtalate (PET) substrates using this process with a mobility of 120 $cm^2/V\,s$ and an ON/OFF current ratio of 10^4.[13]

In this article, we report on the stress-assisted growth of poly-SiGe, for a Si content of 35%, at a maximum processing temperature of 180 °C. This is an exciting result since

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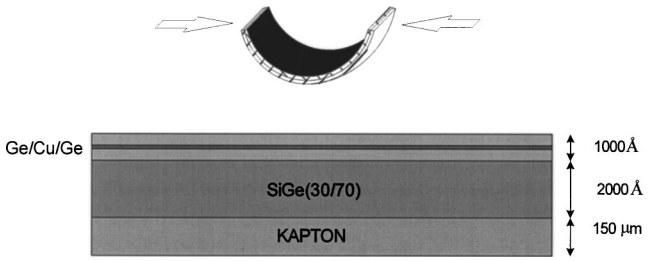

FIG. 1. Top—A schematic picture of the experimental setup and compressive stress is applied by bending the flexible substrate inward. Bottom—The structure of the deposited SiGe/Ge/Cu/Ge multilayer on PET and Kapton substrates.

conventional solid-phase crystallization of SiGe alloys have previously required temperatures above 400 °C.[14–17]

II. EXPERIMENT

The flexible substrates used were PET films with a thickness of 150 μm. Deposited directly onto the substrate was a 2000 Å SiGe layer by simultaneous e-beam evaporation of Si and thermal evaporation of Ge at a substrate temperature of 100 °C and a base pressure of 10^{-6} Torr. Using these same conditions, on top of the SiGe layer was deposited a 500 Å/10 Å/500 Å Ge/Cu/Ge sandwich by e-beam evaporation of Ge and thermal evaporation of Cu. Thermo-mechanical post-treatment is performed by exerting compressive stress during annealing and is applied by bending the flexible substrate inward as depicted schematically in Fig. 1. The thermo-mechanical post-treatments for this sample were an equivalent compressive strain of 0.05% and an annealing temperature of 180 °C for 12 h. Since this work is in its initial stages, it is expected that significant optimization of the thermo-mechanical parameters can be achieved in future work.

III. RESULTS AND DISCUSSION

Rutherford backscatter (RBS) analysis was performed to determine the composition of the multilayer deposited by co-evaporation and the spectrum is given in Fig. 2. The energy of the protons used in the analysis was 1.5 MeV and the Si and Ge concentrations were determined to be 35% and 65% (atomic percent), respectively, for the as-grown material prior to annealing. In general, we have observed that the percentage of Ge is significantly lower than that predicted by the individual deposition rates of Si and Ge and this effect is believed to be due to the more rapid surface evaporation of Ge from the sample in comparison to Si.

The crystalline structure of the SiGe layer has been studied by XRD analysis and the poly-Ge layer was removed by wet etching prior to acquiring the spectrum. Since PET is partially crystalline, it possesses a strong diffraction peak that is superimposed on the ⟨111⟩ peak of poly-SiGe. However, the ⟨220⟩ peak is not convolved with any PET peaks and is distinguishable from the background as shown in the x-ray spectrum of Fig. 3, providing further evidence of the polycrystalline nature of the SiGe layer. The ⟨200⟩ diffraction

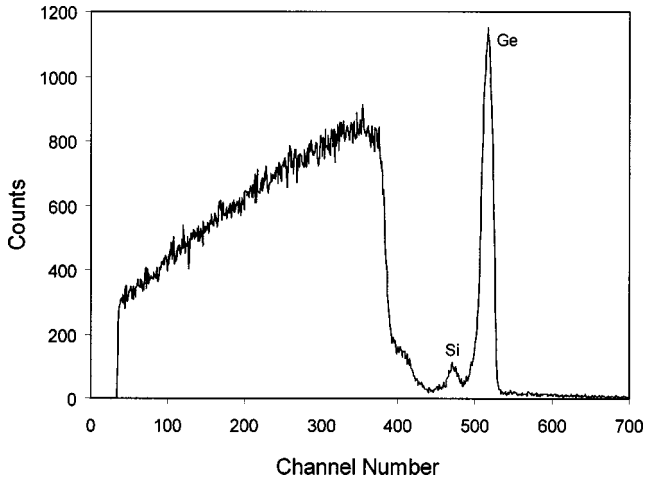

FIG. 2. RBS spectrum yielding Si and Ge concentrations of 35% and 65%, respectively, for the as-deposited multilayer.

peak is kinematically forbidden for Si and Ge and the higher order diffraction peaks are difficult to distinguish from the background.

TEM analysis has been also performed to provide a deeper insight into the nature of growth. A bright-field image of the SiGe layer in plan-view orientation and a selected area diffraction pattern from this same region of sample are given in Figs. 4(a) and 4(b), respectively. The diffraction pattern displays a superposition of polycrystalline and amorphous rings, indicating that the layer contains both polycrystalline and amorphous regions. A TEM image of a cross-sectioned sample taken under dark-field conditions is given in Fig. 5 and three distinct regions are observed. The top layer is the 1000 Å Ge/Cu/Ge sandwich and nucleating from this layer are poly-SiGe crystals growing towards the PET substrate. The uniformly gray region consists of amorphous SiGe. Future work will focus on the optimization of the thermo-mechanical annealing conditions to yield SiGe films that are more uniformly crystallized.

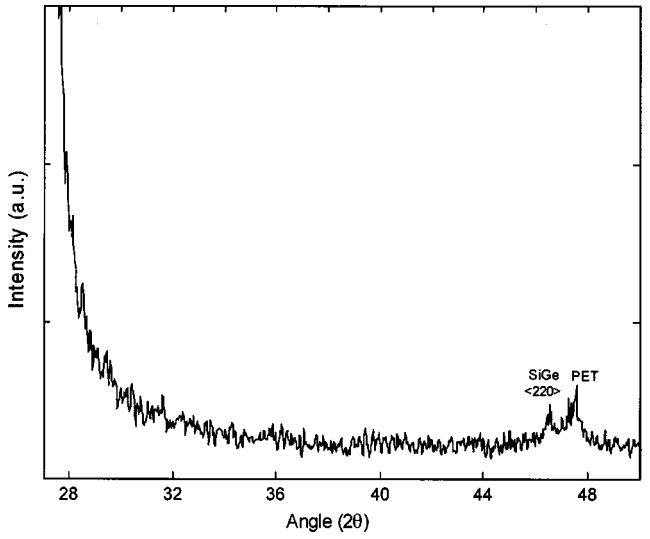

FIG. 3. XRD spectrum showing the ⟨220⟩ peak of polycrystalline SiGe. Note that the ⟨111⟩ SiGe peak is masked by the strong peak of the PET substrate.

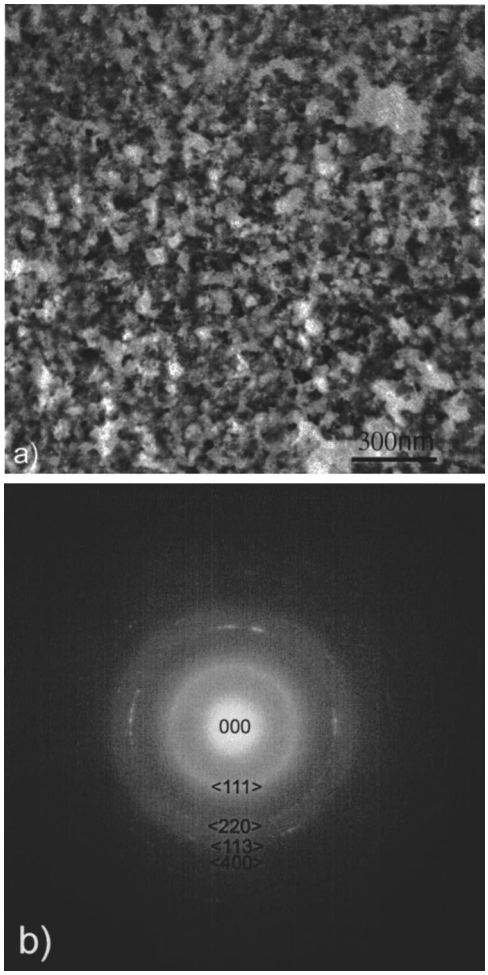

FIG. 4. (a) TEM bright-field image of the SiGe layer in planview and (b) a selected area diffraction pattern displaying a superposition of polycrystalline and amorphous rings.

IV. SUMMARY AND CONCLUSION

In summary, the stress-assisted Ge-induced crystallization of SiGe alloys has been presented and verified by SEM, XRD, and TEM analyses. This crystallization technique is a two-step growth process where the first step is the stress-assisted Cu-induced crystallization of a-Ge (Ref. 12) and the second step is the growth of poly-SiGe where the crystallization is nucleated by the poly-Ge layer grown in the first step. We believe that the second step is also a stress-assisted crystallization phenomenon since conventional growth of SiGe on poly-Ge requires considerably higher temperatures than those observed in the presence of compressive stress. Growth of the poly-SiGe layer is initiated at its interface with the top poly-Ge layer and propagates down in the bulk SiGe. Further characterization of the stress-assisted growth mechanism is currently under study and this method appears to be a promising candidate for the low-temperature fabrication of polycrystalline SiGe TFTs on flexible substrates.

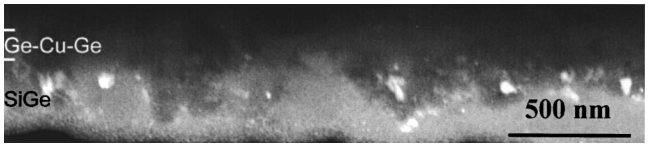

FIG. 5. TEM cross-sectional image taken under dark-field condition displaying the growth of poly-crystalline SiGe nucleated on poly-Ge seeds and advancing into the amorphous SiGe region.

ACKNOWLEDGMENTS

This work was supported by the Iran Telecommunication Research Center, the Natural Sciences and Engineering Research Council of Canada, and the Canada Research Chairs Program.

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