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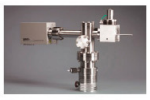
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Molecular-beam epitaxy growth of device-compatible GaAs on silicon substrates with thin (~80 nm) $Si_{1-x}Ge_x$ step-graded buffer layers for high-κ III-V metal-oxide-semiconductor field effect transistor applications

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The authors report the fabrication of TaN–HfO_2–GaAs metal-oxide-semiconductor capacitors on silicon substrates. GaAs was grown by migration-enhanced epitaxy (MEE) on Si substrates using an ~80-nm-thick $Si_{1-x}Ge_x$ step-graded buffer layer, which was grown by ultrahigh vacuum chemical vapor deposition. The MEE growth temperatures for GaAs were 375 and 400 °C, with GaAs layer thicknesses of 15 and 30 nm. We observed an optimal MEE growth condition at 400 °C using a 30 nm GaAs layer. Growth temperatures in excess of 400 °C resulted in semiconductor surfaces rougher than 1 nm rms, which were unsuitable for the subsequent deposition of a 6.5-nm-thick HfO_2 gate dielectric. A minimum GaAs thickness of 30 nm was necessary to obtain reasonable capacitance-voltage (*C-V*) characteristics from the GaAs layers grown on Si substrates. To improve the interface properties between HfO_2 and GaAs, a thin 1.5 nm Ge interfacial layer was grown by molecular-beam epitaxy *in situ* after the GaAs growth. The Ge-passivated GaAs samples were then transferred in air for the subsequent *ex situ* HfO_2 formation. This Ge interfacial layer in between HfO_2 and GaAs was necessary to avoid relatively flat *C-V* characteristics that are symptomatic of high interface state densities. © *2007 American Vacuum Society.* [DOI: 10.1116/1.2713119]

I. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) recently outlined a series of "Grand Challenges" for enhancing device performance of traditional complementary-metal-oxide-semiconductor (CMOS)-based architectures.[1] One of the long-term goals—for year 2014 and beyond—is the implementation of advanced, nonclassical CMOS device structures with enhanced drive current.[2] This can be potentially accomplished through the integration of III-V semiconductor channels due to the higher mobilities of III-V-based materials.[3,4] But historically, III-V materials have been incompatible with conventional high-κ gate dielectrics[5–7] and the mature silicon-based process technology.[8,9] Therefore, we present our efforts in tackling two of the key compatibility challenges involving the realization of high-κ III-V metal-oxide-semiconductor field effect transistors (MOSFETs) on silicon substrates.

The first challenge involves the molecular-beam epitaxy (MBE) growth of smooth, *device-compatible* III-V materials on silicon substrates using thin (~80 nm) $Si_{1-x}Ge_x$ buffer layers. Typically, the MBE growth conditions necessary to achieve smooth GaAs epitaxial layers on Si substrates are contradictory to that which is necessary for growing high-quality materials. Low MBE growth temperatures (<400 °C) are typically necessary to achieve smooth surfaces that are critical for future generations featuring thin gate dielectrics—the reason is because rough surfaces could create an electrical short between the semiconductor channel and the metal gate, in addition to increasing surface roughness scattering. However, the low MBE growth temperatures below 400 °C also results in a poor quality of the as-grown material.[10] Many groups have previously worked to address this dichotomy,[11,12] most notably in the collaborative work of Andre *et al.*[13] The most common approach reported in the literature begins with a low temperature GaAs growth by migration-enhanced epitaxy (MEE) onto the $Si_{1-x}Ge_x$ buffer layers, which is followed by some form of an elevated temperature process to obtain a high-quality GaAs layer.[14] This elevated temperature process usually involves a combination of either an *in situ* anneal and/or MBE growth under "standard" conditions that are typically used for homoepitaxial GaAs growth. The various methodologies have previously demonstrated GaAs material quality on Si substrates that are comparable to homoepitaxial growth onto GaAs substrates. However, the buffer layers typically reported in the literature between the MBE-grown GaAs layer and the Si substrate is usually larger than several hundreds of nanometers, and most

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often require an additional *ex situ* chemical-mechanical polishing (CMP) step in order to recover smooth semiconductor surfaces.[15] This is where our efforts to grow GaAs onto Si substrates differ from the conventional approach. Our objective is to ultimately integrate device-compatible III-V materials on the Si substrate with the thinnest buffer layers possible, without the need for an additional *ex situ* process, such as CMP. These thin buffer layers may also allow for the development of a single hybrid[16] microelectronic chip that combines the individual advantages from both the columns IV- and III-V-based materials.[17] Our GaAs-on-Si growth approach introduces new MBE growth compatibility challenges that must be identified and addressed.

A second compatibility challenge involves the use of thin MBE-grown Ge interfacial layers placed in between the high-κ gate dielectric (HfO_2) and the III-V semiconducting channel material. The lack of a compatible dielectric layer analogous to that of Si/SiO_2 has been a major obstacle toward the integration of III-V-based MOSFETs. A poor dielectric interface due to a large fast interface state density (D_{it}) leads to Fermi level pinning and thereby prevents gate control of the channel region. It has been long believed that one can realize an unpinned Fermi level at the GaAs/oxide interface by employing an interfacial silicon layer in between the insulator and GaAs layers.[18,19] Adopting this paradigm, we have demonstrated the fabrication of MOS capacitors (MOSCAPs) with a relatively low D_{it}.[20] This was achieved with an *in situ* termination of the MBE-grown GaAs layer by a thin (1.5 nm) MBE-grown Ge interfacial layer prior to exposing samples to air for the *ex situ* deposition of HfO_2. We therefore demonstrate that our approach does not necessitate an *in situ* vacuum deposition of high-κ gate dielectrics in the same chamber as for the GaAs epitaxial growth.

II. EXPERIMENT

All samples were grown, characterized, and processed at The University of Texas at Austin. Samples were grown on either (001) GaAs substrates or on (001) Si substrates cut 6° off-axis toward the [110] direction.[15] The growth of GaAs on the Si substrates utilized a thin ~80 nm step-graded $Si_{1-x}Ge_x$ buffer layer grown by ultrahigh vacuum chemical vapor deposition (UHVCVD).[21] We fabricated MOSCAPs in order to determine the gate's ability to control the underlying semiconductor inversion layer. If no gate control is observed in the MOS capacitor, then it is pointless to proceed with fabricating the MOSFET because it will not function. Therefore, the main focus in this work is the MOSCAP structure shown in the unshaded region of Fig. 1. Additional details regarding the growth and characterization of our $Si_{1-x}Ge_x$ buffer layers on the silicon substrates can be found elsewhere;[21] but briefly, it consists of four step-graded $Si_{1-x}Ge_x$ compositional layers of $\mathbf{x} \approx 0.20$, 0.25, 0.40, and 1.0, each with a thickness of about 15, 12, 25, and 30 nm, respectively. The final pure UHVCVD-grown Ge layer is fully relaxed with a surface roughness of ~0.6 nm RMS and a low defect density of $<10^7$ cm^{-2}.[21] After the growth of the $Si_{1-x}Ge_x$ buffer layers, the samples were moved in air to the MBE system where we

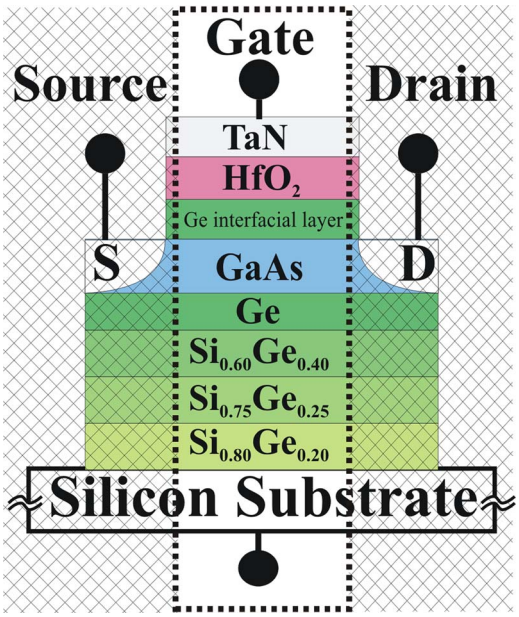

FIG. 1. Schematic illustration of our objective to integrate a high-κ III-V MOSFET on Si substrates. The first task is to determine the gate's ability to control the GaAs inversion region and therefore the unshaded region within the dotted lines shows the MOS capacitor test structure studied in this work.

employed an *in situ* substrate cleaning procedure prior to MBE growth based on the work of Sieg *et al.*, which involved a 650 °C anneal for 10 min.[15] We observed no change in the surface roughness upon *in situ* vacuum annealing of the $Si_{1-x}Ge_x$ buffer layers, which we suspect is due to the fully relaxed nature of our final pure Ge layer.[21] To further examine the thermal robustness of the $Si_{1-x}Ge_x$ buffer layers on the Si substrates, we also performed anneals in the MBE growth chamber for as long as 20 min, also at 650 °C. Again, there was no surface degradation (i.e., roughening or islanding) to suggest that our pure Ge layer on the Si substrate does possess the thermal stability required for the subsequent GaAs growth, which has a thermal growth budget significantly lower than 650 °C at 20 min.

Molecular-beam epitaxy growth of the III-V material was done in a Varian Gen-II™ MBE system. The same MBE growth chamber was also used to grow the Ge interfacial layers for an *in situ* termination of the growth structure prior to pulling the samples into air for the *ex situ* HfO_2 formation step. Solid-source thermal effusion cells were loaded with Ga and Ge, and a valved As cracker was used to increase the As_2/As_4 ratio from the sublimed solid As source. All MBE GaAs growths in this work were Si doped at $\sim 10^{16}$–10^{17} cm^{-3} to generate the *n*-type III-V material. *In situ* reflection high-energy electron diffraction (RHEED),[22] and *ex situ* atomic force microscopy (AFM) (Ref. 23) were both used to monitor the material's surface properties.

The growth of GaAs was done by both MBE and MEE growth techniques—where the main difference is that MBE involves a simultaneous flux of both Ga and As, whereas MEE alternates the Ga and As fluxes.[24] The MBE growth of

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GaAs was done at 580 °C with a nominal growth rate of 1 ML/s (ML denotes monolayer) and an As flux of 5.5×10^{-6} Torr. MEE growths were done using a Ga growth rate of 0.1 ML/s and the As flux was varied in the range of $(1-5) \times 10^{-7}$ Torr. For As fluxes in the range of $(3-5) \times 10^{-7}$ Torr, we found increased pitting ($>10^8$ cm^{-2}) and surface roughening (>1 nm rms) to occur; therefore, we used an As flux of $(1-2) \times 10^{-7}$ Torr to keep below $<10^8$ cm^{-2} and <1 nm rms, respectively, for all MEE growths reported in this work. When the Ga flux was on during the MEE growth, the As shutter and automated valve positioner for the As cracker were both kept closed, and both were subsequently opened for 15 s during the As flux. A 2 s pause was inserted in between the Ga and As fluxes to allow the background pressure in the growth chamber to drop. The MEE growth temperature for this work was varied between 375 and 400 °C. The thickness of the MEE-grown GaAs layers were 15 and 30 nm thick and were grown on the Si substrates using the ~80-nm-thick $Si_{1-x}Ge_x$ step-graded buffer layer. The shutter for the Si dopant cell was left open during the entire growth for both MBE and MEE growth methods, as well as during the 2 s pause with the MEE growth.

The Ge thermal effusion cell temperature was maintained at a Boralectric™ heater temperature of 1360 °C for a nominal Ge growth rate of ~0.025 ML/s, which corresponded to a beam-equivalent pressure of $\sim 1 \times 10^{-8}$ Torr. The Ge growth temperature was chosen to be at 200–300 °C to minimize surface roughening, as well as limiting diffusion between GaAs and the Ge interfacial layer. Although the likelihood of background As deposition—and a corresponding incorporation into the Ge interfacial layer—increases at lower Ge growth temperatures, we found no noticeable difference in the *C-V* characteristics between samples where Ge was grown at ~580 °C from samples with Ge grown at 200–300 °C. We thus accordingly chose to grow at 200–300 °C for said reasons.

III. RESULTS AND DISCUSSION

Smooth semiconductor surfaces are necessary for fabricating MOS capacitors with thin high-κ gate dielectrics. To achieve this, the common procedure reported in the literature involves a low temperature GaAs growth, followed by either an *in situ* anneal and/or high temperature GaAs growth to achieve the high-quality material.[8,9,11–15,24] Although this procedure may be useful for growing thicker films, it deviates from our objective to integrate III-V channel materials with a thin buffer layer on Si substrates.

Our low temperature (≤400 °C) MEE-grown GaAs layer did meet the prerequisite of a smooth semiconductor surface. Figure 2 shows an AFM image of a 30-nm-thick GaAs layer grown on a Si substrate, which has a surface roughness that is less than <1 nm rms with a peak-to-valley distance of ~2.5 nm. From a surface-roughness perspective, this surface is a promising candidate for the subsequent deposition of thin (6.5 nm) high-κ gate dielectrics.

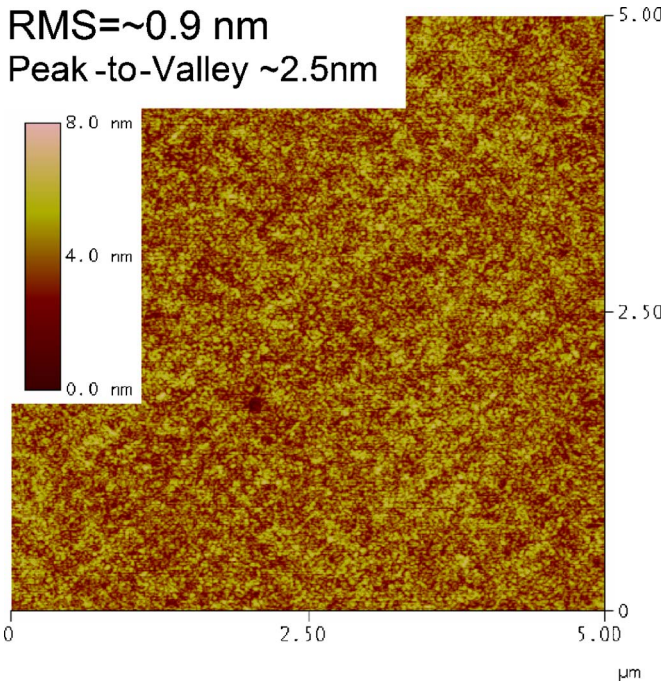

FIG. 2. AFM image of a 30-nm-thick GaAs layer grown on Si substrates using an 80-nm-thick $Si_{1-x}Ge_x$ step-graded buffer layer.

Yet, the material quality remains uncertain. This is because an elevated temperature process is usually necessary to achieve high-quality GaAs. But any high temperature process that we performed exceeding 400 °C based on what is typically reported in the literature (either an *in situ* anneal and/or further GaAs growth at elevated temperatures) caused our bare semiconductor surface to become extremely rough. Therefore to circumvent this predicament, we terminated the semiconductor growth while the surface remained smooth and subsequently proceeded directly to the high-κ dielectric formation process. Since HfO_2 is formed through a two-step process that involves an annealing step,[20] we are essentially performing a high temperature recovery of the GaAs capped with Hf simultaneously with the formation of the HfO_2.

Unfortunately, this method does not allow us to separate out the effects of the pre- and/or postanneal material properties of the MEE-grown GaAs. It is, however, not the focus of this work. Our primary objective in this work is to demonstrate the suitability of our GaAs-on-Si processing approach for future MOSFET applications. Therefore, the feasibility of our approach is first and foremost dependent on the capacitance-voltage (*C-V*) behavior of the fabricated MOS capacitors. If the *C-V* curves do not show any promising MOSFET-compatible device results, then the crystalline quality of the GaAs material is irrelevant because there will be a low likelihood of being able to fabricate high-κ III-V MOSFETs on Si substrates using our approach.

The growth involving GaAs-on-Si substrates is the first part of the challenge; the second part is integrating a high-κ gate dielectric with III-V channel materials. Figure 3 shows the *C-V* curves with and without a Ge interfacial layer in between HfO_2 and GaAs. This 1.5 nm Ge interfacial layer

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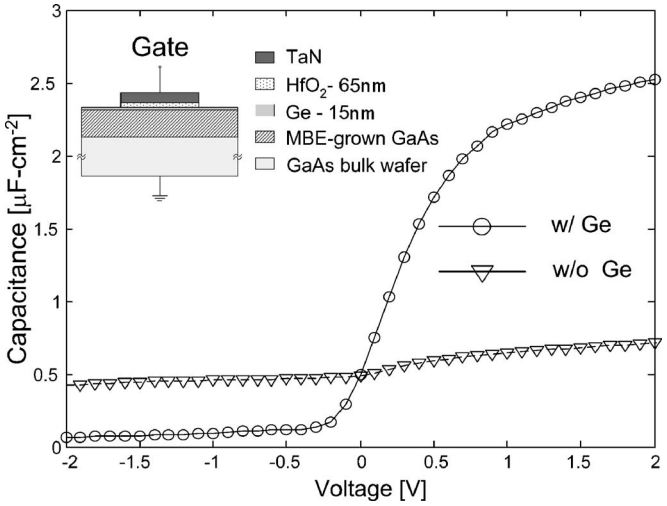

FIG. 3. Comparison of 1 MHz *C-V* curves between two samples grown with and without an *in-situ*-grown Ge interfacial layer. The inset diagram illustrates the schematic cross section of the fabricated MOSCAP on a GaAs substrate.

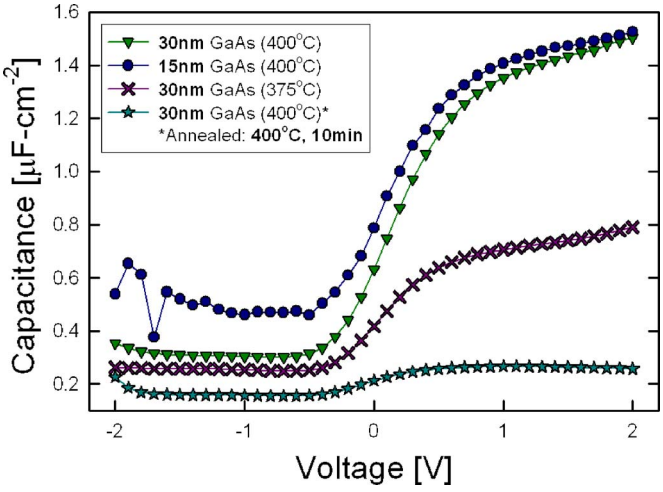

FIG. 4. *C-V* curves for various samples with GaAs grown on Si substrates.

was grown *in situ* after the MBE GaAs growth onto GaAs substrates. The benefits of this Ge interfacial layer was first demonstrated on GaAs substrates to avoid complications involving Si substrates. Due to the low Ge growth temperatures (~200–300 °C), we suspect the Ge layer to be amorphous. This suspicion is supported by real-time *in situ* RHEED monitoring where discrete diffraction patterns were no longer observable after ~10–15 s of Ge growth. Additional details involving our growth and characterization of the HfO_2/Ge/GaAs-based MOS capacitors on GaAs substrates can be found elsewhere.[20,25]

Once we established the successful nature of the Ge interfacial layer, we proceeded to implement this technique with the GaAs layers grown on Si substrates. Figure 4 shows the *C-V* curves of high-κ III-V MOSCAPs on Si substrates for various growth and processing conditions. All samples in Fig. 4 have a 1.5 nm Ge interfacial layer grown between the GaAs and HfO_2. The HfO_2 thickness for each sample is 6.5 nm. The best *C-V* results were observed with a 30-nm-thick GaAs layer grown at 400 °C. Growth temperatures >400 °C resulted in rough semiconductor surfaces that created electrical shorts with the gate. For a growth temperature of 400 °C, a comparison to samples with a thinner 15 nm GaAs layer shows the onset of anomalies in the depletion region of the *C-V* curve (at large negative gate biases). We suspect this is a result of the depletion region punching through to the underlying $Si_{1-x}Ge_x$ buffer layer. Samples that had a 30 nm GaAs layer but were grown at a lower growth temperature of 375 °C, demonstrated poorer *C-V* characteristics than samples grown at 400 °C. Therefore, we observed our optimal MEE growth temperature to be 400 °C. In an attempt to further improve the electrical quality of the 30 nm GaAs layer grown at our optimal 400 °C temperature, we performed an *in situ* anneal for 10 min at 400 °C immediately after the GaAs growth. The As overpressure was maintained at $\sim(1-2)\times10^{-7}$ Torr during the *in situ* anneal. We found that the *C-V* characteristics became worse, which we suspect is caused by an increased degradation of the semiconductor's surface to ultimately cause Fermi level pinning at the interface region between the semiconductor and the high-κ gate dielectric.[26]

IV. CONCLUSIONS

In conclusion, we have demonstrated the feasibility of high-κ III-V MOSCAPs on Si substrates. Our deviation from the conventional approach involves the use of thin $Si_{1-x}Ge_x$ step-graded buffer layers to separate the MEE-grown GaAs layer from the Si substrate. This buffer layer is only ~80 nm. We have also demonstrated the integration of a high-κ gate dielectric (HfO_2) with our GaAs-on-Si structure. The use of a thin ~1.5 nm Ge interfacial layer grown *in situ* following the GaAs growth improves that gate's ability to control the underlying III-V inversion region. To determine the extent of this gate control, and ultimately the device-compatibility of the GaAs material, MOSCAPs were fabricated and tested. The *C-V* characteristics of the MOSCAPs were measured for samples prepared under various growth and processing conditions. For this work, we have found that a 30 nm GaAs layer grown at 400 °C, without any subsequent *in situ* annealing process, resulted in the most promising MOSFET-compatible GaAs material. The demonstration of the MOSCAPs in this work is our first step toward future applications involving high-κ III-V MOSFETs on Si substrates.

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