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Optimization of the V_T-control method for low-power ultra-thin double-gate SOI logic circuits

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Abstract

Application of the V_T-control method is studied in ultra-thin double-gate (DG) SOI inverter, as the simplest building block of SOI logic circuits. Two control voltages, V_{CN} and V_{CP}, are applied to the back-gates of the n- and p-type transistors, respectively, to reduce the leakage current when the inverter is in the idle mode. Simulations with DESSIS disclose that both control voltages may be set at an optimum value for a given circuit activity, leading to the lowest possible gate power-delay product. Simulations have been performed for 10 nm gate-length technology at the end of the ITRS roadmap. These results indicate that the optimized V_T-control method is a promising way for realizing low-power SOI logic circuits. Furthermore, the scalability of this technique is verified by extending the simulations to other generations of the ITRS roadmap.

Keywords: Dynamic threshold voltage; Double-gate SOI; Low-power

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1. Introduction

Optimization of the standby power is becoming more critical as the transistor size is scaled down to nanometric dimensions. As a direct consequence of the scaling trend, the transistor off-current is being increased to accommodate for the performance scaling, as predicted by the ITRS roadmap [1]. Inherent demands of digital applications make it necessary that a digital block remains in an idle mode for a long period of time. This requirement puts forth the inquiry for more elaborate standby power optimization techniques, especially for scaled devices.

One of the well-known methods of reducing the standby power is to minimize the subthreshold leakage current when a transistor is in the idle mode [2]. This may be achieved by controlling the threshold voltage in the sense that increasing its level during the idle mode reduces the leakage current. Also, in some applications different blocks on the chip have different specifications for speed and power consumption. Dual threshold voltage scheme is usually employed to address this requirement, but it is more attractive to have a mechanism that enables the designers to optimize the threshold voltage of the transistors in different blocks.

Applying a proper voltage to the body contact has been proposed to dynamically adjust the threshold voltage of bulk MOS transistors [3]. Also, optimization of the threshold voltage adjusting technique has been studied for bulk MOSFET's [4]. However, this approach has to deal with the problem of charging and discharging the bulk capacitor, which aggravates the total delay of the circuit.

The bulk capacitor problem is eliminated in double-gate (DG) SOI structure and the back-gate may be successfully used to control the threshold voltage. Feasibility of this approach has been demonstrated by fabricating novel SOIAS structures, where the active substrate provides a potentially wide range of threshold voltage adjusting by means of proper back-gate biasing [5,6]. The V_T-control method has been further studied by simulating various DG SOI structures for a single NMOS device and the advantage of the V_T-control method in comparison with the conventional DG operation of these devices has been addressed [7].

In this work, we are concerned with optimizing the V_T-control method for an inverter gate, which is the simplest building block of a logic circuit. Fig. 1 shows a SOI inverter in both conventional double-gate and V_T-control configurations. In the DG configuration, the front and back gates are connected to each other, whereas in V_T-control method the back gate is connected to a different voltage rather than the gate voltage, in order to control the drain–source leakage current in the idle mode. Two independent control voltages, V_{CN} and V_{CP}, are applied to the back gates of the n- and p-type transistors, respectively. When the input is low, the standby power is dominated by the n-type transistor, so a negative control voltage may be applied as V_{CN} to reduce the leakage current drastically. Similarly, control voltage values higher than V_{DD} would be needed for V_{CP}. This may increase the complexity of the control and pulse generation blocks. However, the n^+–p^+ gates presented in [7] or metal gates with different work-functions may be employed to reduce the complexity by providing further pre-adjustment capability of the threshold voltage. This optimization approach was recently introduced in [8]. In this paper, we present this method in more details. In addition, the scalability of this approach is examined and verified by extending the simulations to a group of technology generations according to the ITRS roadmap.

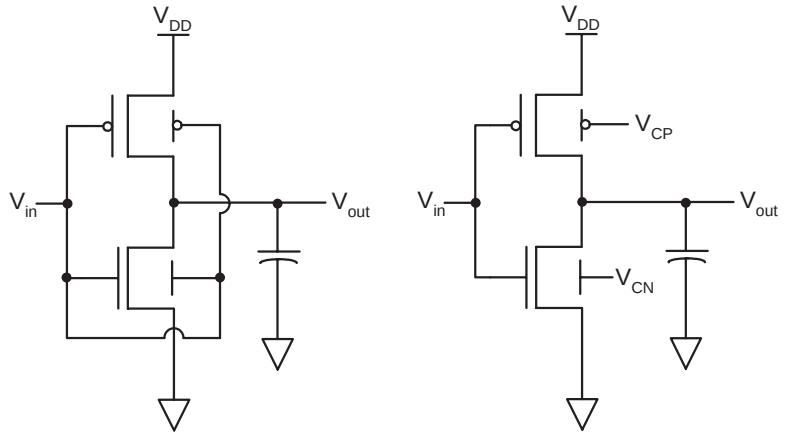

Fig. 1. An SOI inverter gate in: (a) conventional double-gate and (b) V_T-control configuration, where two control voltages are connected to the back gates of the transistors to control the leakage current in the idle mode.

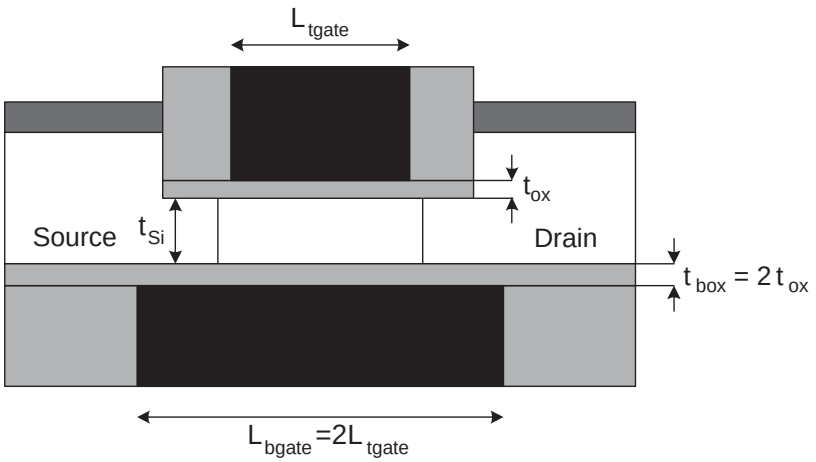

Fig. 2. The schematic structure of the ultra-thin double-gate SOI transistor used for the simulations.

2. Simulation

The DESSIS simulator [9] is employed to study the power consumption issue in 10 nm gate-length devices. The device structure given in Fig. 2 is considered for simulations [7]. The silicon thickness is chosen to be 3 nm in order to ensure the electrostatic integrity and controlled short channel effects; the 2 nm-thick back-gate oxide is selected twice as thick as the front-gate oxide for more reliable manufacturing; and the back-gate length is twice as that of the front-gate to alleviate the nano-scale alignment intricacies [7].

A power supply voltage of 0.6 V and a switching frequency of 28.8 MHz have been used for simulations as predicted by the ITRS roadmap [1]. V_{CN} and V_{CP} are swept in the (−0.6, 0) and (0.6, 1.2) range, respectively, to find the values that optimize the power-delay product figure of merit. Dynamic power consumption and the inverter delay are determined by calculating the charge transferred to the gate terminals when transistors are switching. This way, the Miller effect is taken into account automatically. As a rough estimate for the fan-out, it was assumed that the inverter drives three other inverters with the same structure.

3. Results and discussion

The simulated leakage current in the V_T-control method and DG configuration is compared in Fig. 3. As observed in the plots, the leakage current is considerably reduced both for NMOS and PMOS transistors in comparison with the DG configuration. A controlling range of about three orders of magnitude is achievable in the leakage current, indicating the potential capability of the V_T-control method in minimizing the standby power.

The total dynamic power resulting from charge-transfer to the top and bottom gates of the transistors is plotted versus V_{CN} and V_{CP} and compared with the DG configuration in Fig. 4. The values for V_T-control method are higher than DG but of the same order. However, from the previous plot, it can be predicted that the increase in the dynamic power consumption may be well compensated by the dramatically reduced leakage current, especially as the circuit activity is decreased.

The inverter delays during the 0 to 1 (0–1) and 1 to 0 (1–0) transitions are given in Fig. 5. The V_T-control method makes the gate delay longer in comparison with the DG configuration and the difference becomes more significant when the back gate bias is increased to reduce the standby power further. This is due to the lower drive current of the transistors in the V_T-control scheme compared to the conventional double-gate configuration. Note that the widths of the NMOS and PMOS transistors are scaled in order to give symmetric 0 to 1 and 1 to 0 transitions.

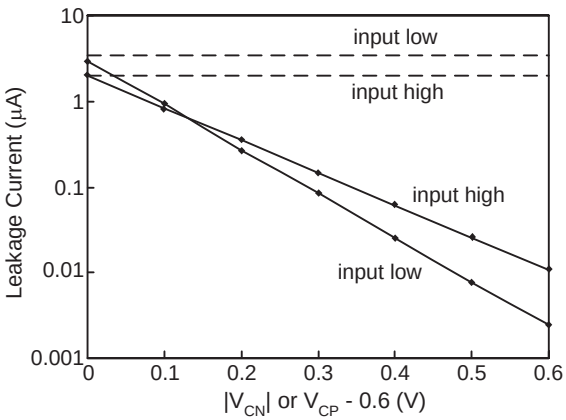

Fig. 3. The simulated leakage current as a function of the threshold control voltages. The corresponding values for the DG configuration are also plotted with dashed lines for comparison.

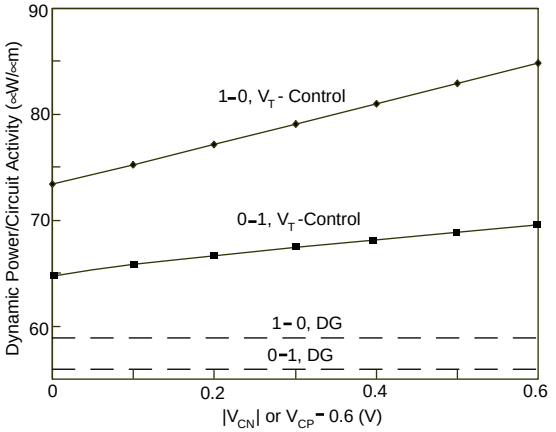

Fig. 4. Dynamic power consumption during 0–1 and 1–0 transition as a function of the control voltages. The data for DG configuration is also shown with dashed lines. The circuit activity was kept constant and equal to 0.1.

Fig. 6 shows the total power-delay products for the 0 to 1 and 1 to 0 transitions versus V_{CN} and V_{CP}, for various values of the circuit activity. For the comparison, the results for DG structure are shown in this figure. It can be seen that in the V_T-control method, the values of power-delay product are lower than those of DG configuration and the difference becomes more significant as the circuit activity is reduced. Thus, as could be predicted, the V_T-control method becomes more effective in lower circuit activities, which is the case for most of the typical low-power applications. In addition, as it appears from the same plots, each of the V_{CN} and V_{CP} control voltages reach an optimum point for a given circuit activity. These optimum values of V_{CN} and V_{CP} are plotted in Fig. 7. For values of circuit activity less than 0.01, the optimum control voltages approach $-V_{DD}$ and 2 V_{DD} for NMOS and PMOS, respectively. One can use different metal work-functions for the top and bottom gates [7] in order to set these optimum values at 0 and V_{DD}, respectively.

In Fig. 8, the ratio of the power-delay product in the optimum V_T-control method to that of DG is plotted versus the circuit activity. As was observed in Fig. 6, for low circuit activities, the value of the power-delay product strongly depends on choosing the appropriate values of V_{CN} and V_{CP}, which reveals the importance of determining the optimum values of these control voltages.

In order to examine the scalability of the optimized V_T-control method, similar simulations were carried out for devices with various gate lengths as specified by the ITRS roadmap. The results indicate that the proposed approach is highly scalable, as observed from the plots in Fig. 9. The normalized circuit activity α_n is defined as $\alpha f_0/f$, where f_0 is the switching frequency for the simulated 10 nm devices and is equal to 28.8 MHz. These plots propose that the α_n constant contours are almost linear and follow the supply voltage scaling trend. This means that the optimum values of the control voltages presented in Fig. 7 may be used for other technology nodes by scaling the vertical axis to V_{DD}, i.e. to $|V_{CN\,opt}|/V_{DD}$ and $|V_{CP\,opt}|/V_{DD}$, and generalizing the horizontal axis with α_n. In particular, when the circuit activity is small, one can set the control voltages at $-V_{DD}$ and $2V_{DD}$, for NMOS and PMOS transistors, respectively.

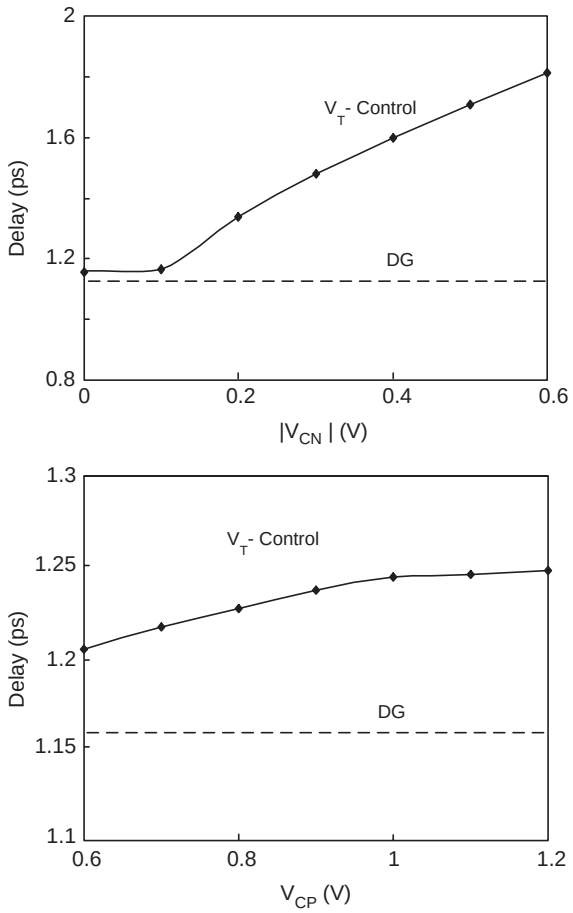

Fig. 5. The total gate delay for the V_T-control as a function of the control voltages. Dashed lines represent conventional DG.

4. Summary and conclusions

The application of the V_T-control method in ultra-thin double-gate (DG) SOI inverter, as the simplest building block of SOI logic circuits was presented. It was shown that for any given circuit activity, there are optimum values of control voltages in V_T-control method aimed to reduce power-delay product in DG SOI logic circuits. At each stage, the power consumption components and the total gate delay have been compared to the DG configuration. Our results revealed that the V_T-control method is very effective for low-power applications especially when the circuit activity is low and the circuit remains in the idle mode for long periods of time. This is due to the fact that the V_T-control method is principally concerned with reducing the standby power. Also, it was shown that for small values of circuit activity the optimum control voltages can be set independent of the circuit activity, leading to a simpler control circuitry. The approach can be also utilized to set the threshold voltage for different blocks on the chip based on their speed/power

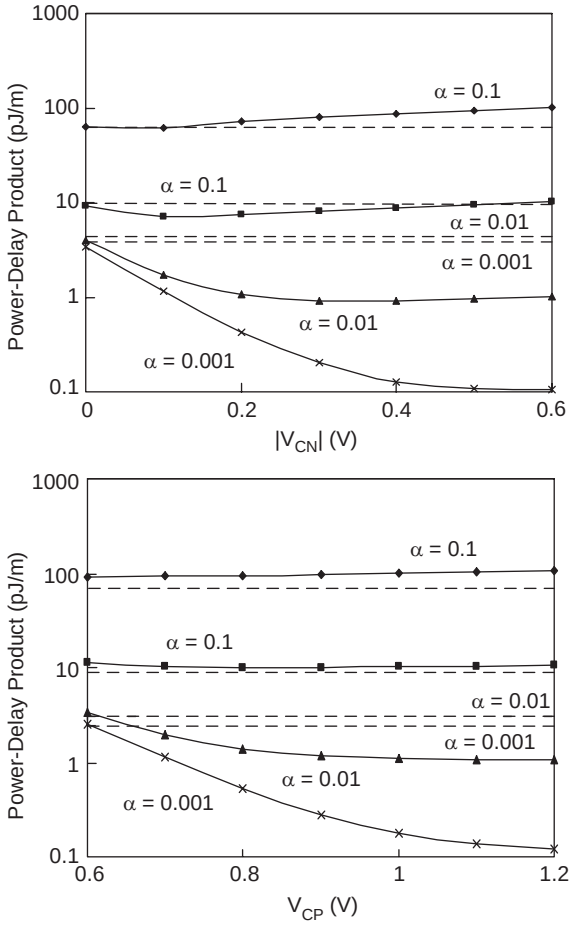

Fig. 6. The total power-delay product versus the control voltages for different values of the circuit activity. For any given value of the circuit activity there is an optimum value of the control voltage to minimize the power-delay product. The corresponding DG values are also shown with dashed lines.

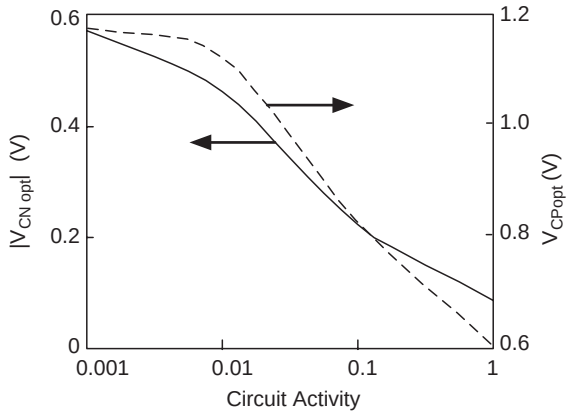

Fig. 7. Optimum values of the control voltages as a function of the circuit activity.

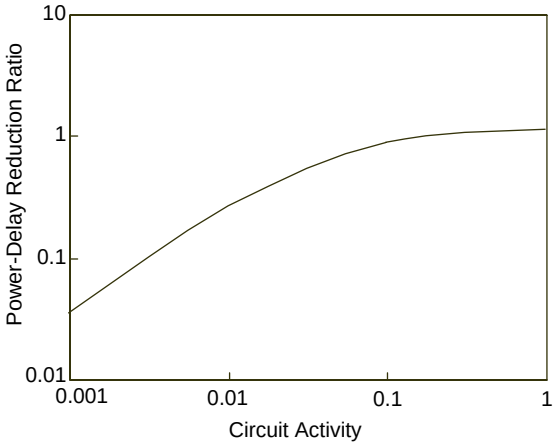

Fig. 8. The ratio of the power-delay product in the optimum V_T-control method to that in conventional DG configuration as a function of the circuit activity.

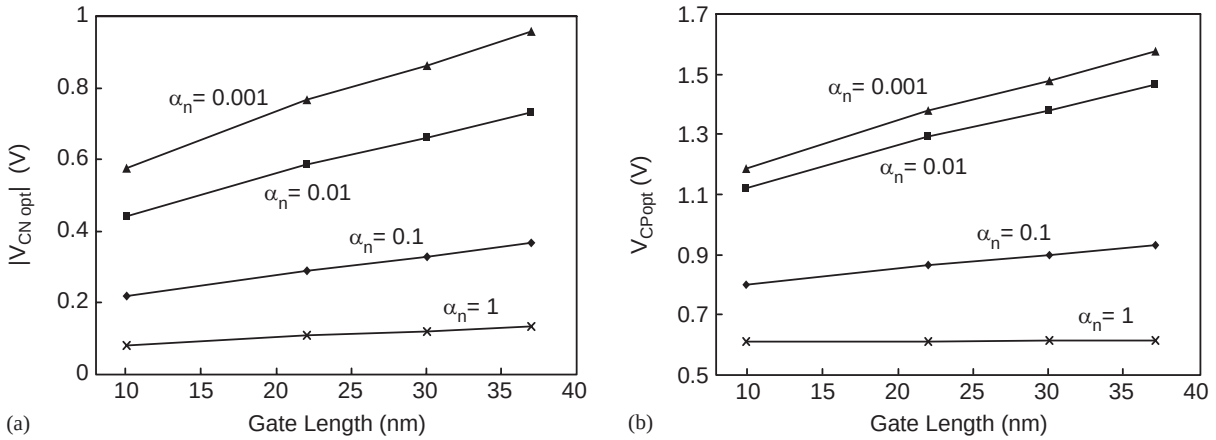

Fig. 9. Optimum values of the control voltages for: (a) NMOS and (b) PMOS transistors at different technology nodes and for different values of the normalized circuit activity.

trade-offs or to alleviate the process-induced fluctuations by adjusting the threshold voltage of different chips in different areas of a wafer to cancel the wafer-to-wafer and die-to-die variations [10].

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