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Physical and electrical characterizations of metal-oxide-semiconductor capacitors fabricated on GaAs substrates with different surface chemical treatments and Al$_2$O$_3$ gate dielectric

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The authors present experimental evidence on the impact of three different chemical surface treatments on the interface between the GaAs substrate and the aluminum oxide dielectric layer used in the fabrication of metal-oxide-semiconductor capacitors. The three different chemical surface treatments studied prior to atomic layer deposition (ALD) of the dielectric layer include (a) GaAs native oxide removal in a dilute HF solution only, (b) HF etch followed by a NH$_4$OH treatment, and (c) HF etch followed by a (NH$_4$)$_2$S treatment. Moreover, interfacial self-cleaning of nontreated GaAs wafers upon ALD of aluminum oxide using trimethyl aluminum precursor was examined. Transmission electron microscopy, electron energy loss spectroscopy (EELS) and capacitance-voltage (*C-V*) data showed slight differences among the nontreated, HF-only, and NH$_4$OH treated samples. However the (NH$_4$)$_2$S treated sample showed improved capacitance-voltage characteristics as well as an improved aluminum oxide/GaAs interface compared to the other three samples. Additionally, the characteristic oxygen *K* EELS peak suggests the presence of a thin additional layer close to the center of the high-κ layer containing oxygen, tantalum, and aluminum, as a consequence of probable plasma damage to the high-κ layer during the TaN metal gate deposition. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3256229]

I. INTRODUCTION

Electron devices featuring high-mobility channel materials are being contemplated as a way to keep up with Moore's law and drive complementary metal oxide semiconductors beyond the 22 nm node. Research on materials with enhanced mobility, such as SiGe,[1] Ge,[2] GeC,[3,4] and III-V (Refs. 5 and 6) structures, has received a lot of attention recently, based on the advent of advanced high-κ materials in production lines. III-V compound materials present several advantages over their Si counterparts, such as higher electron mobility and higher breakdown fields, which makes them suitable for high-speed *n*-channel devices and high power-temperature applications. However, in order for us to be able to take advantage of the superior properties of III-V materials over Si, we have to solve the problem caused by the lack of a high-quality native gate insulator and improve the currently poor quality interface between GaAs-based materials and conventional gate dielectrics. As a result of the extensive research on identifying the appropriate gate dielectric and

surface passivation treatment for GaAs-based materials, several techniques have been identified and are still being studied as possible solutions. Some of these are addition of a controlled interfacial passivation layer such as amorphous silicon or germanium,[7,8] *in situ* molecular beam epitaxy-grown Ga$_2$O$_3$(Gd$_2$O$_3$),[9] and atomic layer deposition (ALD) of Al$_2$O$_3$[10] and HfO$_2$,[10–12] all these with and without chemical surface passivation[8,11–14] treatments prior to the deposition of the gate dielectric layer. Experimental results from different research groups have reported on the effective prevention of the Fermi-level pinning at the interface between the GaAs substrate and the high-κ gate layer by the implementation of the earlier mentioned techniques.[7–14] Arsenic oxides at the interface between the GaAs and the high-κ layer are believed to be responsible for the Fermi-level pinning, therefore an interface free of this oxide is thought to show an unpinned Fermi-level. Interestingly, ALD of Al$_2$O$_3$ on GaAs-based substrates has been previously reported to remove these undesired arsenic oxides using trimethyl aluminum as the precursor material.[10,13]

In the present work, we report on the effect of different surface chemical treatments on the interface between the

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TABLE I. Summary of the surface treatments performed on the different samples prior to deposition of the aluminum oxide layer and the postdeposition anneal step followed.

Sample	Description	Postdeposition anneal
1	No. surface treatment	None
2	HF only	None
3	HF+NH$_4$OH	550 °C 5 min in N$_2$
4	HF+(NH$_4$)$_2$S	550 °C 5 min in N$_2$

GaAs substrates and the aluminum oxide layer, and the electrical characteristics of fabricated GaAs-substrate metal-oxide-semiconductor (MOS) capacitors.

II. EXPERIMENT

The MOS capacitors were fabricated on (100) *p*-type GaAs substrates with doping concentrations of $(0.5-1) \times 10^{18}$ cm^{-3}. In order to study the effect of the surface treatment, three different chemical treatments were carried out prior to aluminum oxide deposition. Table I below summarizes the surface treatments. The first sample analyzed had no treatment performed on it, the second sample only included the native oxide removal in HF (1%) solution for 1 min, while the third and fourth samples included the previously mentioned HF treatment followed by sample dip in either NH$_4$OH (10%) (sample 3) for 1 min or (NH$_4$)$_2$S (20%) (sample 4) for 10 min. All chemical surface treatments were carried out at room temperature.

After chemical treatment, the samples were immediately transferred to a commercial Savannah™ 200 ALD reactor for aluminum oxide deposition onto GaAs surface at 250 °C by alternating water and trimethyl aluminum precursors. Then the NH$_4$OH and (NH$_4$)$_2$S treated samples received a post-deposition anneal (PDA) performed at 550 °C for 5 min in N$_2$ ambient. Finally, a thick TaN layer was deposited as the metal gate using a dc magnetron sputtering system and was patterned using standard photolithography and reactive ion etching processes.

All cross sectional samples for transmission electron microscopy (TEM) analysis were prepared with the use of a Disco 321 DAD™ dicing saw, followed by the use of a focused ion beam (FIB) FEI FIB 200 to achieve an electron transparent thickness.

TEM studies were performed on a FEI Tecnai F30 microscope equipped with a field emission gun operating at 300 kV. The point-to-point resolution of the instrument in conventional high resolution TEM (HRTEM) mode is about 0.19 nm (C_s=1.2 mm). The electron energy loss spectroscopy (EELS) and high angle annular dark field (HAADF) data were recorded in scanning transmission electron microscopy mode while stepping a small focused electron probe of ~0.3 nm diameter across the stack. The EELS spectra were recorded using a postcolumn imaging filter (GATAN GIF-2001) with a $1k \times 1k$-yttrium aluminum garnet charge coupled device camera. The probe forming convergence semiangle (α) was 10 mrad and the spectrometer collection
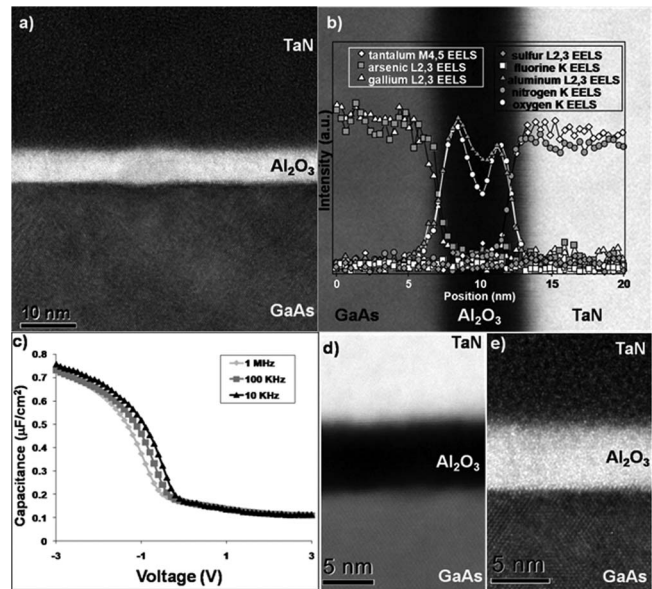

FIG. 1. (a) Cross sectional TEM micrograph showing the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. No clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed. (b) HAADF micrograph superimposed on their corresponding EELS line scan profile showing a clear area of overlap between the signals of the elements in the GaAs substrate and the aluminum oxide layer. (c) Frequency dispersion behavior of the GaAs MOS capacitor from the nontreated sample, showing a clear ΔV_{fb}. (d) High resolution-HAADF image of the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. (e) HRTEM image of the same region from (d), in both cases no clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed.

semiangle for EELS (β) was 20 mrad (2 mm GIF entrance aperture). HAADF collection semiangles for imaging were between 50 and 120 mrad using a detector positioned near the spectrometer entrance aperture to allow both image and spectrum collections with a camera length of approximately 40 mm. The capacitance-voltage curves were obtained at different frequencies (1 Mhz, 100 kHz, and 10 kHz) using an Agilent HP 4284A, 20Hz–1MHz Precision *LCR* meter.

III. RESULTS AND DISCUSSION

Figures 1(a)–1(e) show the TEM, HAADF, EELS, and capacitance-voltage results for the first sample without any surface treatment. In the bright-field TEM images [Fig. 1(a)] a rough GaAs-substrate surface can be observed. However, a sharp transition from the crystalline GaAs substrate to the amorphous aluminum oxide layer can be seen in the TEM images. No interfacial layer can be distinctly observed between the GaAs substrate and the aluminum oxide layer. The HAADF images [Figs. 1(b) and 1(d)] confirm the absence of a clear interfacial layer and also show a sharp transition from the crystalline GaAs substrate to the high-κ layer. It is known that the ALD growth of aluminum oxide on GaAs-based substrates using trimethyl aluminum as the aluminum precursor significantly diminishes the undesired arsenic oxides,[10,13,15,16] rendering better interfacial properties and thinner interfacial oxide layers. The EELS results [Fig. 1(b)]

show that at the interface between the GaAs substrate and the aluminum oxide, there is a region approximately 3 nm wide where the signals from the elements in the GaAs substrate and in the aluminum oxide layer overlap with each other. This can be attributed to two different factors. First, the surface roughness observed at the interface produces an overlap of the GaAs substrate and the aluminum oxide layer along the electron beam direction when it is transmitted through the sample. A very similar effect has been reported previously for TiN–HfSiO interfaces.[17] The second factor is the presence of an interfacial layer containing Ga, As, O, and Al. Gallium oxide, elemental arsenic, and some remnants of arsenic oxide (As_3O_5) have been reported to be observed at this interface in similar processed samples as suggested by x-ray photoelectron spectroscopy (XPS) results.[15,16] Even though the arsenic oxides are mostly removed after the ALD aluminum oxide deposition using trimethyl aluminum as the aluminum precursor, based on XPS observations (not shown), it appears that the Ga–O bonds remain relatively intact at the interface between these two layers,[15] leaving the gallium oxide layer mostly unchanged. The capacitance-voltage (CV) results [Fig. 1(c)] show a flatband voltage shift, ΔV_{fb} ($\Delta V_{fb} = V_{fb}[10$ KHz$] - V_{fb}[1$ MHz$]$), of approximately 430 mV, which can be attributed to slow interface traps produced by As-rich surface and/or a gallium oxide interfacial layer.

Figures 2 and 3 show the results for the sample after HF treatment only and HF followed by NH_4OH treatment, respectively. The NH_4OH treatment is used to provide a suitable surface for ALD growth since it is expected to leave the surface-OH terminated. As a consequence, self-limiting reaction and full surface coverage tend to occur in very early stages of the ALD process.[18] The TEM and HAADF images observed for these two samples are remarkably similar to the results observed for the nontreated sample. In all cases there is a reduction in the surface roughness observed in the GaAs-substrate surface, a sharp transition from the crystalline GaAs-substrate to the amorphous aluminum oxide layer, and no clear evidence of an interfacial layer between the GaAs substrate and the aluminum oxide layer. EELS results for all samples suggest a region approximately 3 nm wide where the signals from the elements in the GaAs substrate and in the aluminum oxide layer overlap with each other for the same reasons discussed earlier for the untreated sample. The CV characteristics for these two samples are similar in showing a ΔV_{fb}. However, the variations in this ΔV_{fb} were smaller for the sample with the HF-only treatment, approximately 375 mV, and yet even slightly smaller for the sample with HF followed by NH_4OH treatment, approximately 300 mV, compared to the nontreated sample.

The EELS and XPS results suggest that even after being removed by the HF treatment,[10] an oxide layer on the GaAs-substrate surface may form before the samples are introduced into the ALD reactor. This oxide layer formed is not easily removed by the ALD deposition of aluminum oxide using trimethyl aluminum as the aluminum precursor,[14–16] nor is the formation of this oxide inhibited by the NH_4OH surface
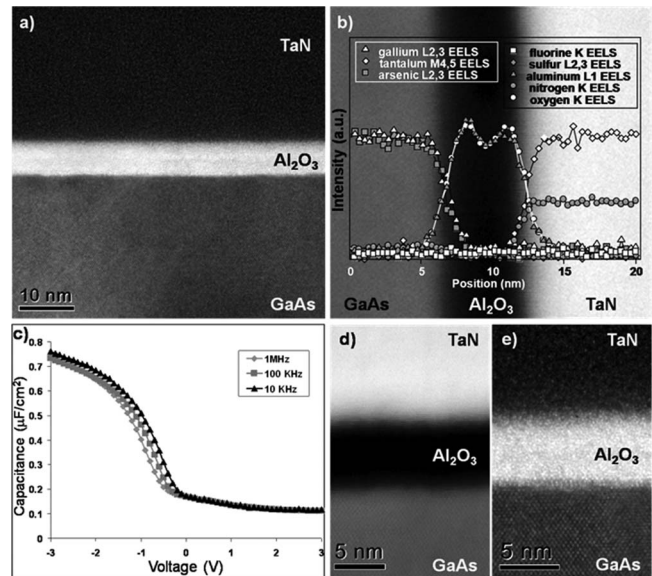

FIG. 2. (a) Cross sectional TEM micrograph showing the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. No clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed. (b) HAADF micrograph superimposed on their corresponding EELS line scan profile showing a clear area of overlap between the signals of the elements in the GaAs substrate and the aluminum oxide layer. (c) Frequency dispersion behavior of the GaAs MOS capacitor from the HF-only treated sample, showing a lower ΔV_{fb}. (d) High resolution-HAADF image of the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. (e) HRTEM image of the same region from (d), in both cases no clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed.

treatment on GaAs-based substrates.[16] The previous observations suggest that the regrown oxide observed in the samples analyzed in the current study is mostly gallium oxide since the growth of arsenic based oxides, i.e., As_2O_3 and As_3O_5,[16] is more likely to be inhibited. Furthermore, based on XPS observations,[15] the NH_4OH treated sample contains the highest Ga–O bonding from the three surface treated samples in the present study, suggesting a higher content of gallium oxides in this NH_4OH treated sample. Another possibility is that this gallium oxide interfacial layer is formed after the deposition of the aluminum oxide layer due to the interaction of the O atoms from the aluminum oxide layer and the Ga atoms from the GaAs substrate. In any case, the formation of gallium oxide is going to be always favored over the formation of arsenic oxide due to the lower standard Gibbs energy of formation of the gallium oxide species (Ga_2O_3 $= -998.3$ kJ/mol) than the arsenic oxide species (As_2O_5 $= -728.3$ kJ/mol).[19]

Figure 4 shows the results for the sample with HF followed by $(NH_4)_2S$ treatment. Sulfur passivation of III-V materials has been reported as an efficient way to improve the interfacial characteristics with gate dielectric materials,[8] and also to prevent the regrowth of native oxides after their removal.[20] In this case, the TEM and HAADF results suggest an improved interface between the GaAs substrate and the aluminum oxide layer compared to the previous three
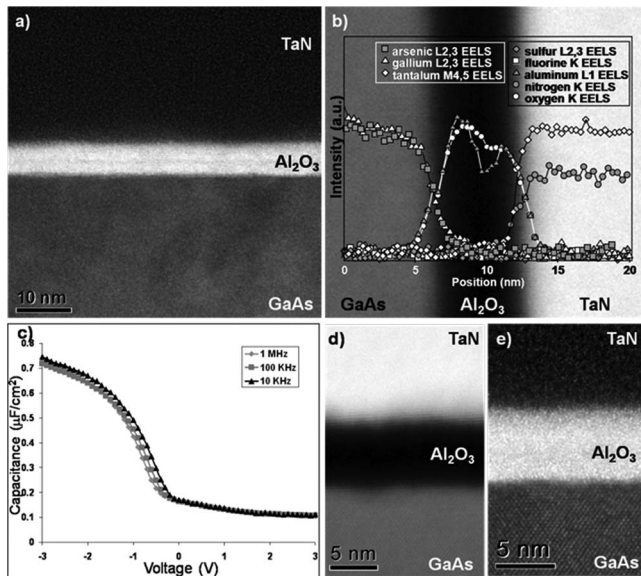
FIG. 3. (a) Cross sectional TEM micrograph showing the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. No clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed. (b) HAADF micrograph superimposed on their corresponding EELS line scan profile showing a clear area of overlap between the signals of the elements in the GaAs substrate and the aluminum oxide layer. (c) Frequency dispersion behavior of the GaAs MOS capacitor from the HF−NH$_4$OH treated sample, showing an even lower ΔV_{fb}. (d) High resolution-HAADF image of the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. (e) HRTEM image of the same region from (d), in both cases no clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed.
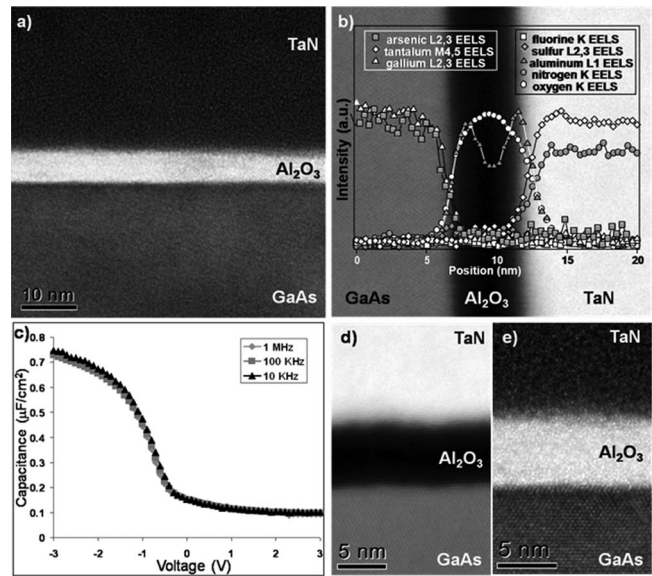

FIG. 4. (a) Cross sectional TEM micrograph showing the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. No clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed. (b) HAADF micrograph superimposed on their corresponding EELS line scan profile showing the smallest area of overlap between the signals of the elements in the GaAs substrate and the aluminum oxide layer. (c) Frequency dispersion behavior of the GaAs MOS capacitor from the HF−(NH$_4$)$_2$S treated sample, showing the lowest ΔV_{fb} from the four samples analyzed. (d) High resolution-HAADF image of the interface between the GaAs substrate, the aluminum oxide layer, and the TaN layer. (e) HRTEM image of the same region from (d), in both cases no clear interfacial layer and a sharp transition between the GaAs substrate and the aluminum oxide layer can be observed.

samples. The EELS results also show an improved interface between these two layers, based on the fact that the region of overlapping between the signals of the elements present in the GaAs substrate and the aluminum oxide has decreased substantially (the approximate thickness measured is 1 nm). We can also see a clear sulfur signal coming from this interface region. The CV results also showed the lowest ΔV_{fb} for this sample relative to the three previous samples, approximately 85 mV. The smallest ΔV_{fb} and the thinner overlap region suggest a thinner interfacial gallium oxide—elemental As layer compared to the previous three samples. XPS results also suggested a thinner gallium oxide layer at this interface for the sulfide-treated sample, based on the analysis of the Ga $2p_{3/2}$ peak of the XPS spectrum.[15] We believe that the (NH$_4$)$_2$S treatment reduces the amount of Ga atoms available to react with O atoms to form a gallium oxide layer resulting in a thinner gallium oxide—elemental As interfacial layer and into an improved interface between the GaAs substrate and the aluminum oxide layer, which in turn translates into better CV characteristics.

An interesting feature observed on the samples that received a PDA treatment is that the oxygen K EELS characteristic peak close to the center of the aluminum oxide layer showed a "double peak" rather than the characteristic single major peak normally observed around 532 eV. Figure 5(b) shows the characteristic oxygen K EELS peaks observed at

the center and edge of the amorphous aluminum oxide layer. The oxygen signal from the edge of the layer (shown by black diamond symbols) is similar to the oxygen K peak observed in SiO$_2$ whereas the oxygen K EELS peak near the center of the aluminum oxide layer (shown by gray square symbols) shows an extra peak. The appearance of this "extra" peak [marked by the black arrow in Fig. 5(b)] on the oxygen K EELS characteristic peak coincides with the region where the aluminum signal decreases close to the center of the aluminum oxide layer in the EELS signal profiles of Figs.
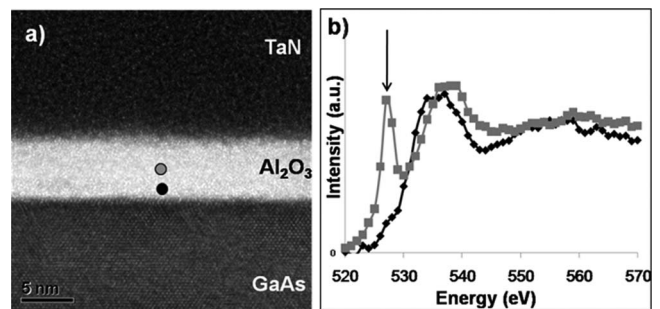

FIG. 5. (a) HRTEM micrograph showing the two different areas where the two EELS spectra were recorded. (b) EELS spectra showing the O K EELS characteristic peak from the black point (black diamonds) and the gray point (gray squares). An additional peak (marked by the black arrow) can be observed in the spectrum from the gray point, close to the center of the aluminum oxide layer.

1(b), 2(b), 3(b), and 4(b). The double peak at the oxygen K EELS characteristic peak has been attributed in other studies[21,22] to the crystal field splitting of the d orbitals of atoms with available empty d orbitals in coordination with the $2p$ orbitals of the oxygen atoms. In the samples analyzed in the current study the only element with available empty d orbitals is tantalum from the metal gate layer. We propose that the tantalum atoms that are first sputtered from the metal gate target are able to reach deeper into the aluminum oxide layer damaging the high-k layer and reside in the middle of this dielectric layer until the PDA takes place. During the anneal, they chemically interact with the surrounding oxygen and aluminum atoms, creating a thin tantalum-oxygen-aluminum layer resulting in the appearance of the double peak in the oxygen K characteristic EELS peak. A very low tantalum signal can be observed in the EELS signal profiles close to the center of the high-k layer, in the same region where the aluminum signal decreases. However the tantalum signal in this region is just slightly higher than the background noise level. These observations suggest plasma damage to the high-κ layer during the TaN metal gate deposition. Without performing the PDA the hysteresis from the bidirectional capacitance-voltage sweeps was measured to be approximately 450, 500, 580, and 620 mV for the $(NH_4)_2S$ treated, NH_4OH treated, HF-only, and the nontreated samples, respectively (data not shown). These large hysteresis values can provide additional evidence for plasma damage to the high-κ gate dielectric layer. However, the differences in the hysteresis values for the differently treated samples indicate the existence of comparatively lower slow interface traps for the sulfide-treated sample. Moreover, hysteresis value for the sulfide-treated sample was reduced to approximately 280 mV after PDA.

Standardless energy dispersive x-ray spectrometry analysis was performed on this sample to get an estimate of the atomic ratio between the aluminum and oxygen atoms inside the grown high-κ aluminum oxide layer. The results suggest an Al/O ratio of around 1.3, almost double the expected Al/O ratio of 0.66 for the stoichiometric Al_2O_3. This difference could be partly attributed to the possible damage of the high-κ layer during the TaN metal layer deposition, and the possible interactions between the gallium atoms from the GaAs substrate and the oxygen atoms from the aluminum oxide layer in the formation of the gallium oxide layer present in the interfacial layer observed in the EELS results between these two layers.

In summary, we have studied the effect of three different chemical surface treatments of GaAs substrate prior to ALD aluminum oxide deposition and we have compared them against a sample with no surface treatment. The samples with no surface treatment, HF only, and HF–NH_4OH presented very similar structural and electrical characteristics. Some surface roughness was observed at the interface between the GaAs substrate and the aluminum oxide, with the nontreated sample presenting the more evident surface roughness of these three samples. No clear interfacial layers could be discerned on the TEM and HAADF results for these three samples. However, the EELS results suggested the presence of a transitional layer (approximately 3 nm thick) where the signal of the elements composing the two layers could be observed overlapping. XPS results suggest the presence of elemental arsenic and Ga_2O_3 at this interface.[15] For all these three samples the capacitance-voltage results presented clear ΔV_{fb}, which suggest the presence of slow interface traps related to the transitional layer. The sample with $(NH_4)_2S$ surface treatment presented improved structural and electrical characteristics. A smaller surface roughness at the interface between the GaAs substrate and the aluminum oxide was observed, while TEM and HAADF did not show any clear indications of an interfacial layer at this interface. However, EELS results showed a much thinner transitional layer (approximately 1 nm thick), with a clear sulfur signal observed in this transitional layer. Finally, the capacitance-voltage characteristics presented the lowest ΔV_{fb} of the four samples analyzed in the present study, which indicated better interfacial properties obtained with the sulfur passivation treatment. EELS results suggested the presence of a thin tantalum-oxygen-aluminum layer close to the center of the aluminum oxide layer that unintentionally grows after the PDA as a possible consequence of plasma damage to the high-κ layer during the TaN metal gate deposition.

ACKNOWLEDGMENTS

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