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Protein-Assembled Nanocrystal-Based Vertical Flash Memory Devices with Al_2O_3 Integration

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This work presents vertical flash memory devices with protein-assembled PbSe nanocrystals as a floating gate and Al_2O_3 as a control oxide. The advantage of a vertical structure is that it improves cell density. Protein assembly improves uniformity of nanocrystals, which reduces threshold voltage variation among devices. The introduction of Al_2O_3 as a control oxide provided lower voltage/faster operation and hence less power consumption compared with the devices fabricated with SiO_2. The integration of Al_2O_3 appeared to be compatible with the protein assembly approach. In conclusion, Al_2O_3 has the potential to become the high-k control oxide due to its relatively high electron/hole barrier heights, and high permittivity.

Key words: High-k dielectric, nanocrystal memory devices, protein assembly, vertical structure

INTRODUCTION

As device dimensions are reduced, nanocrystal-based flash memory devices suffer various scaling problems, such as nonuniform deposition of nanocrystals, and low capacitive coupling between tunnel oxide and control gate resulting in slow operation. Nonuniform deposition causes variation in the number of nanocrystals among devices. Therefore, the threshold voltage deviates from device to device. Various methods have been proposed in the literature to improve nanocrystal uniformity.[1–3] One of the methods proposed nanocrystal assembly using a protein called Chaperonin 60 or GroEL.[2] In this method, nanocrystals are assembled on an oxide surface using GroEL. Nanocrystal assembly using GroEL on the vertical sidewalls has also been demonstrated.[4] This result implies that the mechanics of the method depends more on van der Waals force than gravity.[4] The advantages of a vertical structure are that it improves cell density and provides greater surface area for nanocrystal deposition on sidewalls than a planar structure of similar dimensions. Hence, threshold voltage variation might be further reduced.

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For low-power and fast operation of flash devices, direct tunneling or Fowler–Nordheim (FN) tunneling are used as program or erase (P/E) mechanisms. The continued scaling of flash devices requires the use of new materials as control oxide to extend the direct tunneling (DT) regime or improve the programming window in the FN regime while the tunnel oxide is still SiO_2. Introduction of a high-k material as a control oxide improves capacitive coupling between control gate and tunnel oxide as well as the P/E efficiency due to high dielectric permittivity of the materials.[5,6] For most high-k materials, the improvements of higher permittivity are diminished by poor retention resulting from the low conduction band offset of these materials. On the other hand, high permittivity and larger conduction/valence band offsets make Al_2O_3 a promising candidate as a control oxide for memory operation.

There have been several reports in the literature on high-k control oxides in flash memories but most of them either followed an oxide–nitride–oxide (ONO) structure with a nanocrystal floating gate or an interpoly dielectric (IPD) structure with a polysilicon (poly-Si) floating gate.[5,7] However, the effect of the interface between nanocrystal and high-k is not well understood. Besides, there are few reports on high-k integration of the GroEL assembly

method. The objective of this work is to study the effect of Al_2O_3 integration in GroEL-assembled PbSe nanocrystal memory devices through electrical characterization. The P/E characteristics of the devices with Al_2O_3 as a control oxide show improvements over the devices with SiO_2 as a control oxide.

FABRICATION METHOD

Heavily doped ($\sim 10^{18}$ cm^{-3}) p-type silicon (100) wafers were etched by reactive-ion etching (RIE) to form vertical mesas of different widths. Sacrificial oxidation was done on the sidewalls to reduce the damage from RIE. A ~5-nm-thick SiO_2 was thermally grown as a tunnel oxide at 850°C. Lead selenide (PbSe) nanocrystals (6 nm in diameter as specified by the vendor) were deposited employing a protein-assembly method.[2,4] Using this method, first the wafer was floated on the 0.1 mg/mL GroEL solution for 10 min with the oxide side down for protein orientation on the surface. Then the wafer was blow-dried with N_2 and a nanocrystal-containing solution was drop-casted on the protein-coated wafer. The extra solvent was dried in air. After this, the template was removed by annealing in the atmospheric ambient at 300°C for about 10 min. A ~20-nm-thick control oxide was deposited using atomic layer deposition (ALD) of Al_2O_3. Low-pressure chemical vapor deposition (LPCVD) of ~150-nm-thick poly-Si completed the gate stack. The gate area was then etched by RIE and ion implantation was done for n^+ source, drain, and gate. The next step was SiO_2 deposition as isolation oxide at 520°C by LPCVD. This step also served as the first step in activation annealing for source/drain. The second step of annealing was done at 650°C for 60 s in nitrogen ambient in a rapid thermal annealing (RTA) chamber.[8] Contact holes were patterned and Al was deposited as the contact metal using physical vapor deposition (PVD).

Figure 1 shows a schematic of a cross-sectional view, and Fig. 2 shows a scanning electron micrograph (SEM) of a top view of the vertical MOSFETs. The electrical characterization was carried out on the devices with 30-μm-wide sidewalls.

RESULTS AND DISCUSSION

In general, flash devices have similar dielectrics as both the tunnel and control oxides. The effective field across the tunnel oxide is increased with the introduction of high-k dielectric as a control oxide and SiO_2 as a tunnel oxide. This effect results directly from Gauss's law and may be given as

$$F_1 = \frac{\varepsilon_2 V_G}{4t_2 + \varepsilon_2 t_1}, \quad F_2 = \frac{4V_G}{4t_2 + \varepsilon_2 t_1}, \tag{1}$$

where $\varepsilon_{1,2}$ is the dielectric constant, $t_{1,2}$ is the thickness, $F_{1,2}$ is the electric field across tunnel and control oxides, respectively, and V_G is the pulse

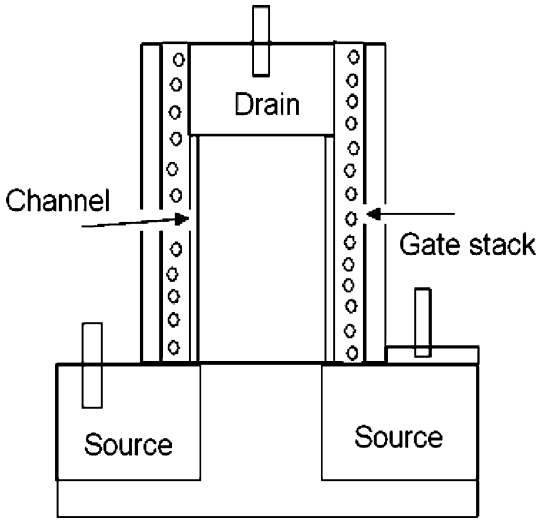

Fig. 1. Schematic of a cross-sectional view of the fabricated vertical MOSFET structure.

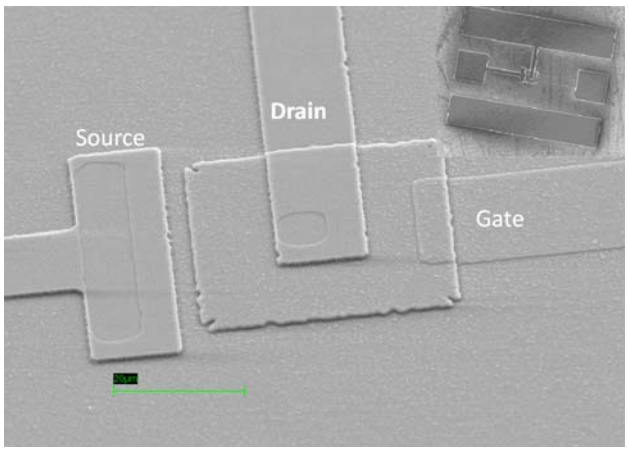

Fig. 2. SEM of a top view of the fabricated vertical MOSFET structure.

amplitude.[6] The higher dielectric permittivity of Al_2O_3 improves cell coupling capacitance. In this work, a twofold memory window was obtained in the devices with Al_2O_3 compared with those with SiO_2 as control oxide at the same gate pulse. In the literature about 0.3 V memory window was reported at a gate pulse amplitude of ±9 V and pulse duration of 100 ms for similar vertical MOSFETs with SiO_2 as control oxide.[4] In this work, a 0.7 V window is observed under the same program/erase (P/E) conditions. The difference in ε_1 and ε_2 provides different injection and emission currents through the tunnel and control oxides which helps to enhance the memory window.

Figure 3 shows memory window variation with pulse amplitude. The memory window increases with pulse amplitude. Figure 4 indicates that P/E time exponentially decreases with increasing pulse amplitude. From Figs. 3 and 4, FN tunneling is estimated to occur at 7 V. Fowler–Nordheim

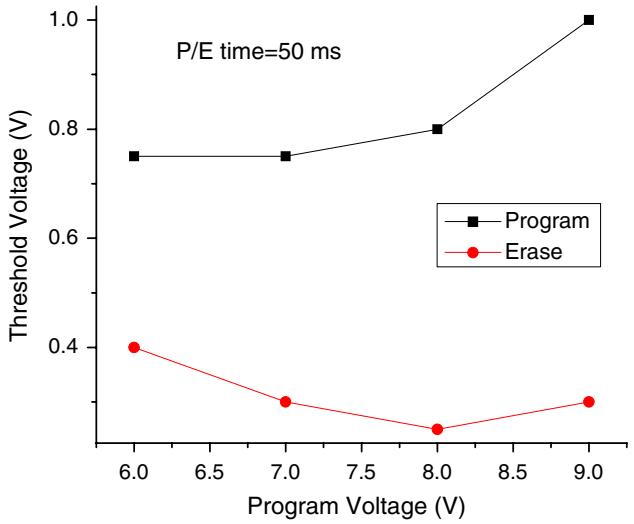

Fig. 3. V_{th} versus program/erase voltages. The memory window increases with pulse amplitude until the leakage currents become comparable at high voltages.

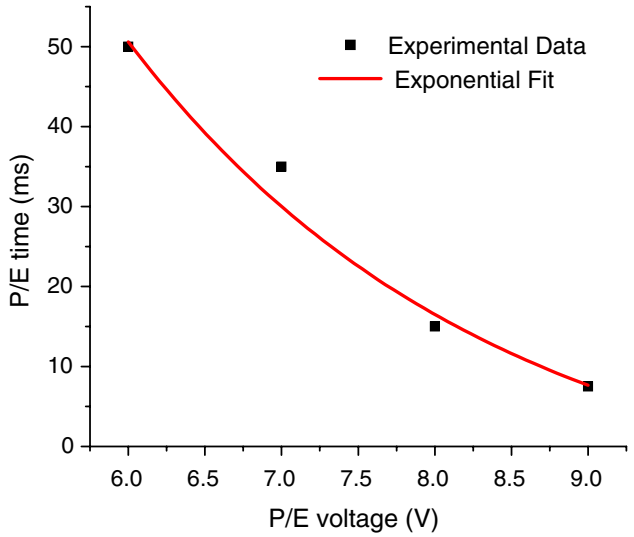

Fig. 4. Programming speed increases exponentially with pulse amplitude.

tunneling occurs at low voltages as a result of higher F_1 obtained with Al_2O_3 control oxide. For pulse amplitudes less than 7 V, DT is the programming mechanism.

Figure 5 shows the memory window at different pulse amplitudes and pulse durations. Memory operation deteriorates at pulse amplitudes of 9 V. For $|V_G| \geq 9$ V, tunneling currents through both the oxides become comparable and the memory window reduces. The effect is more pronounced during erase as shown in Figs. 3 and 5. During erase, a negative V_G causes accumulation of electrons at the poly-Si/oxide interface. As V_G becomes more negative, more electrons are available to tunnel through the control oxide to the nanocrystals/substrate. Some of these electrons are trapped in

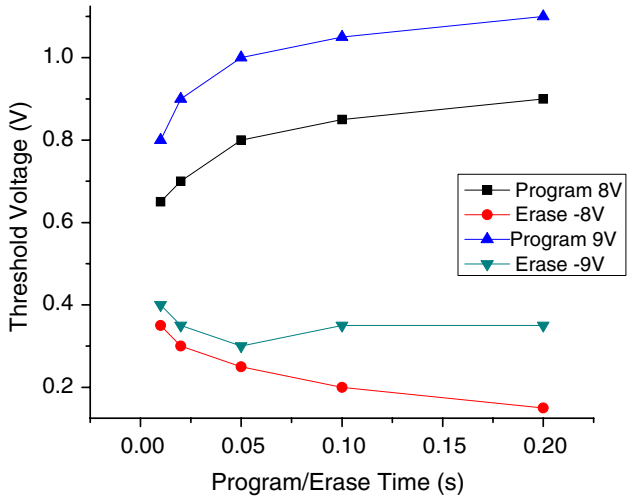

Fig. 5. V_{th} versus program/erase time. At 9 V high leakage current through control oxide reduces the memory window.

the nanocrystals or oxides, and as a result the threshold voltage (V_{th}) increases, which degrades the memory window.

Reasonable conduction/valence band offsets of control oxide are necessary for retention as well as memory window maintenance. If the band offset is small, injection from gate or emission from nanocrystals to gate will be high. This tunneling will degrade the memory window and retention. For most high-k materials, the improvement of higher permittivity is diminished by low conduction/valence band offsets. The smaller the band offset, the narrower the operating range of memory devices due to the overlapping of injection/emission currents through oxides.[9] In order to use high-k materials with small band offsets, the thickness of the control oxide has to be large enough to prevent electron tunneling across the control gate. This limitation not only reduces scalability but also increases the effective oxide thickness (EOT) of the gate structure. Table I presents a comparison among different high-k materials in terms of ε_r and band offsets. Al_2O_3 has high permittivity and a higher conduction band offset than other common high-k materials,[10] so the coupling capacitance is improved for Al_2O_3 without degrading the memory window and retention.

The memory window obtained in a nanocrystal flash memory is a function of tunnel oxide, control oxide, gate material, and importantly, nanocrystal material. Uniform spherical nanocrystals with narrow size distributions are the most suitable for protein synthesis. Lead selenide is one of the few commercially available materials that have a suitable morphology for protein synthesis and a charge trapping capability for memory operation. However, the memory window reported with PbSe is poor compared with some other nanocrystals.[2,4] Lead selenide has a conduction band offset of 0.1 eV with Si substrate.[2] Quantum confinement

Table I. Comparison Between Dielectric Permittivity ε_r, Conduction Band Offset φ_c, Valence Band Offset φ_v, and Energy Band Gap E_g of Different Dielectric Materials[10]

	ε_r	φ_c (eV)	φ_v (eV)	E_g (eV)
SiO_2	3.9	3.5	4.4	9
Al_2O_3	9	2.8	4.9	8.8
HfO_2	25	1.5	3.4	6
ZrO_2	20	1.4	3.3	5.8
TiO_2	80–100	1.2	–	3.05
Ta_2O_5	25	0.3	3.0	4.4

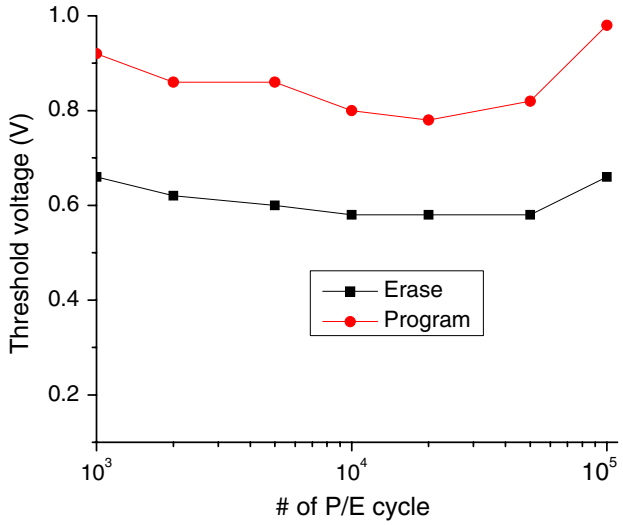

Fig. 6. Endurance test at ±5 V pulse amplitude, 150 ms pulse duration.

effect raises energy bands upwards, which results in small memory window and slow programming.[11] Metal nanocrystals would give better performance as a floating gate due to high electron density and less quantum effect. However, in this work, PbSe nanocrystal material was not optimized for better performance because the focus was on the high-k integration of protein-assembled nanocrystal devices.

Figure 6 shows the endurance characteristics of the fabricated memory devices. The devices maintain a reasonable memory window up to 10^5 cycles of P/E operation at pulse amplitudes of ±5 V and pulse duration of 150 ms. The endurance characteristics show positive charge trapping and hence a V_{th} shift. A positive V_{th} shift has also been reported in the literature for nanocrystal-based planar memory structures with Al_2O_3 as a control oxide.[7] Future work should focus on reducing the V_{th} shift during endurance by improving high-k quality. The devices without nanocrystals show ~0.15 V hysteresis at ±5 V, 150 ms operation. This fact indicates that Al_2O_3 is likely forming trap sites, although we do not see severe device degradation. Less than 50%

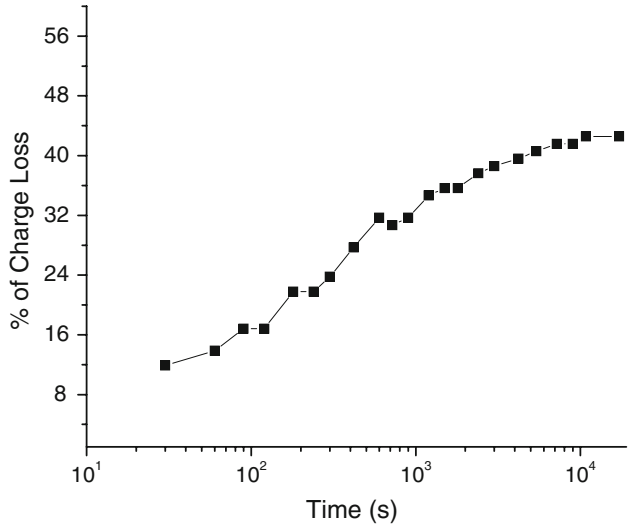

Fig. 7. Room-temperature retention test after programming the device at 7 V, 1 s.

charge loss is observed during room-temperature retention testing, as shown in Fig. 7. Initially, a high number of electrons are stored in the nanocrystals, which results in high fields across the oxides. Consequently, charge loss occurs quickly. Moreover, the quantum confinement effect shifts conduction band energy upwards in nanocrystals and the conduction band offset with Al_2O_3 decreases.[11] Both of these effects cause degraded retention. In order to improve retention, the thickness of Al_2O_3 should be optimized.

Program/erase, endurance, and retention characteristics of protein-assembled nanocrystal-based vertical memory devices with Al_2O_3 as control oxide follow the common trend of memory devices. Device performance and ellipsometry data (not shown) verify that Al_2O_3 was deposited on the nanocrystal surface. The twofold memory window improvement over SiO_2 devices conforms to the theoretical estimation that improvement in F_1 results in increased memory window. The devices without nanocrystals show a small memory window (0.15 V). From this, it can be deduced that few additional trap sites are contributing to the memory operation.

SUMMARY

Aluminum oxide is a potential control oxide in flash memory devices because of its high dielectric permittivity and higher conduction band offset than other high-k materials. We report the programming performance of protein-assembled nanocrystal-based vertical flash devices with Al_2O_3 as a control oxide. These devices showed enhanced programming windows compared with the devices with SiO_2 as a control oxide. Al_2O_3 integration appears to be compatible with the protein assembly process. However, the threshold voltage shift during endurance indicates stress-induced trap generation in the oxides.

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