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Citation: Applied Physics Letters **94**, 063117 (2009); doi: 10.1063/1.3079410
View online: http://dx.doi.org/10.1063/1.3079410
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/94/6?ver=pdfcov
Published by the AIP Publishing

Realization of dual-gated $Ge-Si_xGe_{1-x}$ core-shell nanowire field effect transistors with highly doped source and drain

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(Received 22 November 2008; accepted 16 January 2009; published online 12 February 2009)

We demonstrate dual-gated germanium (Ge)-silicon germanium (Si_xGe_{1-x}) core-shell nanowire (NW) field effect transistors (FETs) with highly *doped* source (S) and drain (D). A high-κ HfO_2 gate oxide was deposited on the NW by atomic layer deposition, followed by TaN gate metal deposition. The S and D regions of NW were then doped using low energy (3 keV) boron (B) ion implantation with a dose of 10^{15} cm^{-2}. The electrical characteristics of these devices exhibit up to two orders of magnitude higher current and an improved ON/OFF current ratio by comparison to dual-gated NW FET with *undoped* S/D. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3079410]

As the dimensions of complementary metal-oxide-semiconductor (CMOS) devices reach the tens of nanometers scale, device scaling is hindered by short channel effects and variability in device fabrication.[1,2] Semiconductor nanowire (NW) field effect transistors (FETs) have gained interest as an alternative device structure[3–5] primarily because a reduced short channel effect can be achieved in NW FETs in the gate-all-around device geometry.[6] Most of the reported electrical characteristics of NW FETs to date are based on devices with metal (Schottky) contacts.[7–9] In these devices, the performance, namely, ON current and ON/OFF current ratio, can be significantly limited by the metal-semiconductor Schottky barrier and the contact resistance at source (S) and drain (D) regions. In addition, an ambipolar behavior is usually observed in these devices.

In order to realize high performance NW FETs, achieving a high doping level, typically of $\sim 10^{20}$ cm^{-3} or higher, in the S/D regions is necessary. Highly doped S/D allows efficient carrier injection into NWs and a low contact resistance.[10] To date, NW FETs with highly doped S/D have been reported for Si NWs using either ion implantation[11,12] or axial doping modulation for NWs grown via the vapor-liquid-solid (VLS) mechanism.[13] Ge NW FETs and $Ge-Si_xGe_{1-x}$ core-shell NW FETs are of interest because of higher mobility than Si and CMOS compatibility. Particularly, Ge–Si core-shell NWs provide a high mobility one-dimensional hole gas[14] as well as a better interface for high-κ gate oxide deposition.[15] Here we demonstrate a high performance dual-gated $Ge-Si_xGe_{1-x}$ core-shell NW FET with highly *doped* S/D realized by low energy ion implantation. Such devices show two orders of magnitude higher current compared to NW FETs with nominally *undoped* S/D, as well as an improved ON/OFF current ratio.

Our $Ge-Si_xGe_{1-x}$ NWs were grown on Si (111) substrates in an ultrahigh vacuum chemical vapor deposition chamber via the VLS growth mechanism and using Au as catalyst. The Ge core was first grown at a total pressure of 5 Torr and a temperature of 285 °C using 60 SCCM (SCCM denotes standard cubic centimeters per minute at STP) GeH_4 (10% diluted in He). The Si_xGe_{1-x} shell was *epitaxially* grown in the *same* growth chamber by coflowing SiH_4 and GeH_4 at a growth chamber temperature of 400 °C. The Si_xGe_{1-x} shell had a thickness of ~ 4 nm and an approximate Si content of $x=0.3$, as evidenced by transmission electron microscopy and energy dispersive x-ray spectroscopy.

The process flow for the fabrication of the NW FETs investigated here is outlined in Fig. 1. After growth, the NWs were suspended in an ethanol solution and dispersed onto a dielectric substrate [Fig. 1(a)] consisting of a 10 nm thick HfO_2 layer grown on a *n*-type Si (100) wafer, which can serve as back-gate. The NW dispersed sample was first dipped in ~1% hydrofluoric (HF) acid for 20 s and cleaned with the de-ionized water. The sample was then annealed at 500 °C for 5 min in an NH_3 ambient, a process typically used to reduce the density of uncompensated Ge surface states.[16] This was followed by atomic layer deposition (ALD) of HfO_2 dielectric film with a nominal thickness of 8.5 nm, as shown in Fig. 1(b). Next, a 100 nm thick TaN metal gate (*G*) electrode was defined using e-beam lithography (EBL), sputtering, and lift-off. The HfO_2 layer deposited on the S and D regions of the NW-FET was etched using a ~3% HF solution. Using the self-aligned process described above, two types of devices were then fabricated. In one set of devices, metal S/D contacts were realized using EBL, 100 nm nickel (Ni) deposition, and lift-off as shown in Fig. 1(d). As such, the S/D metal contacts were defined onto nominally undoped sections of the NW.

In a second set of devices, once the gate area was defined, the sample was subsequently ion-implanted with B. The implantation was done at a dose of 1×10^{15} cm^{-2}, with an ion energy of 3 keV, at a tilt angle of 32°, and rotating 360° during the implantation [Fig. 1(c)]. All devices underwent a 5 min 600 °C rapid thermal anneal in an N_2 ambient to activate the implanted B dopants in the S/D areas of the NW-FET.[17] As such, the NW sections not covered by the gate became highly doped, while the relatively thick TaN film prevented the B ions to reach the NW. Ni S/D contacts were fabricated using EBL, metal deposition, and lift-off as shown in Fig. 1(d). After contact metal deposition, the devices were annealed at 300 °C for a minute. Figure 1(e) shows a scanning electron micrograph (SEM) of the fabricated device.

We first address the electrical characteristics of dual-gated NW FETs without B-doping in the S/D regions (Fig.

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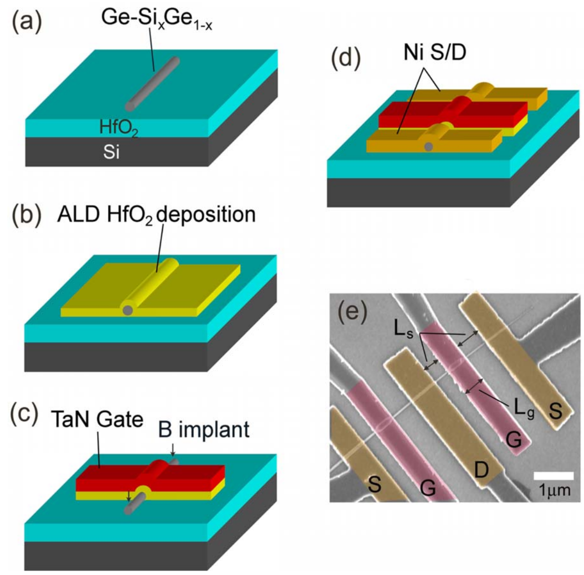

FIG. 1. (Color online) (a) Schematic representation of a Ge–Si$_x$Ge$_{1-x}$ core-shell NW dispersed on a HfO$_2$/Si substrate. (b) ALD of HfO$_2$ on the NW. (c) Gate metal (TaN) deposition and HfO$_2$ layer etching, followed by B ion implantation (d) B activation anneal and Ni deposition on the S/D regions. (e) SEM of a NW dual-gated FET device with Ni contacts. The red regions G represent the gates, and the yellow regions represent the S/D.

2). In Fig. 2(a), we show the output characteristics, namely, the drain current (I_d) versus the applied drain bias (V_d) measured at different values of the top-gate bias (V_g) and for two values of the back-gate bias, $V_{bg}=0$ V and $V_{bg}=-1.5$ V. The NW has a diameter of 60 nm, a gate channel length of $L_g=720$ nm, and a section not covered by the top-gate of length $L_s=830$ nm, where L_s is defined by the total length of NW sections between S/D to G contacts [Fig. 1(e)]. Figure 2(b) data show the I_d-V_g data for two values of the back-gate bias (V_{bg}). We define the ON-state (I_{on}) and OFF-state (I_{off}) current as the drain current measured at $V_d=V_{dd}=-1.0$ V and at top-gate biases $V_g=V_T+0.7V_{dd}$ (ON-state) and $V_{off}=V_T-0.3V_{dd}$ (OFF-state) respectively; V_T represents the threshold voltage of the device, defined by linearly extrapolating I_d versus V_g, measured at $V_d=-0.05$ V, to zero I_d.

Two observations are apparent from the data of Fig. 2(a). First, the ON current is very low: at $V_{bg}=0$ V the device shows a maximum current of 120 nA at $V_d=V_g=-2.0$ V and an ON current $I_{on}=40$ nA. The low I_{on} value translates into a very low I_{on}/I_{off} ratio, equal to 20 for the data in Fig. 2 at $V_{bg}=0$ V. The low I_{on} is largely limited by the resistance of the NW sections not covered by the top-gate, which acts as a series resistance (R_s), combined with the metal to NW contact resistance (R_c) at the S/D. The measured channel resistance (R_m) is the sum of R_c, R_s, and the top-gated channel resistance (R_{ch}). In order to roughly estimate the fraction of R_c and R_s in R_m, we estimate R_{ch} by assuming a typical mobility (μ) value of ~ 80 cm^2/V s, determined by a four-point gate dependent measurement on the same intrinsic Ge–Si$_x$Ge$_{1-x}$ core-shell NWs. The expected value of R_{ch} at $V_g=-1.0$ V using $R_{ch}=L_g[C_{ox}(V_g-V_T)\mu]^{-1}$ is ~ 46 kΩ; C_{ox} represents the NW capacitance per unit length. For this estimate, the capacitance value of $C_{ox}=1.56$ nF/m was calculated using a finite element method (Ansoft Q3D Extractor®). On the other hand, the extracted R_m value at $V_g=-1.0$ V is 6.2 MΩ. Clearly, the intrinsic channel resistance

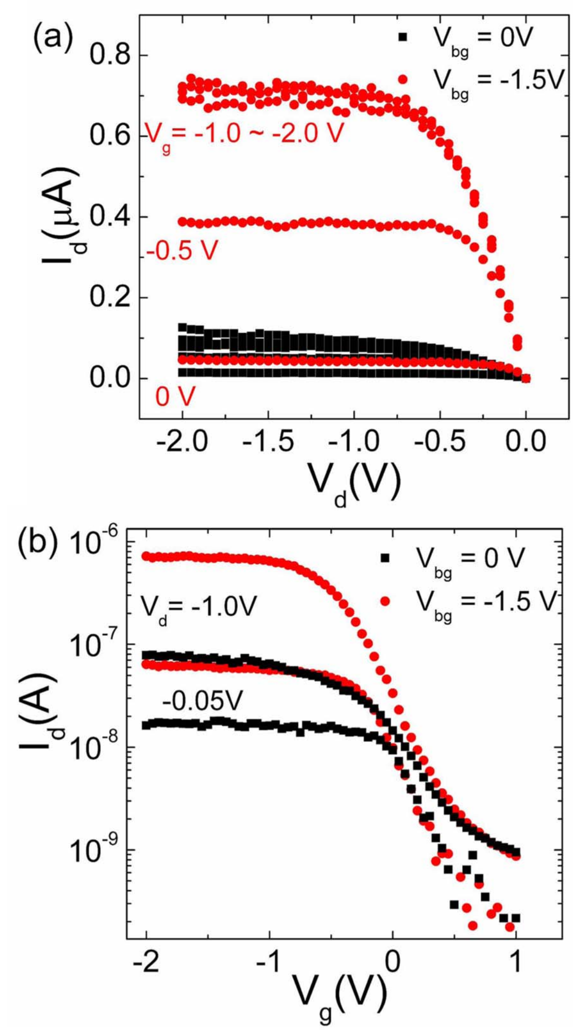

FIG. 2. (Color online) Electrical characteristics of a Ge–Si$_x$Ge$_{1-x}$ core-shell NW FET with undoped S/D, and with a channel length $L_g=720$ nm. (a) I_d vs V_d data measured at different V_g values. (b) I_d vs V_g data measured at different V_d values. The data in both panels were measured at two back-gate biases: $V_{bg}=0$ V (square, black symbols) and $V_{bg}=-1.5$ V (round, red symbols).

represents only a small fraction of the total device resistance, which is primarily dominated by the contact and series resistances, which, in turn, are large because the S/D areas are nominally undoped.

Second, the device performance can be significantly changed by applying a back-gate bias. A negative V_{bg} value increases the hole concentration in the NW sections not covered by the top-gate, thereby reducing R_c and R_s. The data of Fig. 2 show a tenfold increase in ON current for $V_{bg}=-1.5$ V compared to $V_{bg}=0$ V, and a corresponding increase in I_{on}/I_{off} to 130. The subthreshold slope (SS), defined as $SS=-[d(\log_{10} I_d)/dV_g]^{-1}$ at $V_d=-0.05$ V, decreases from 420 mV/decade for $V_{bg}=0$ V to 360 mV/decade for $V_{bg}=-1.5$ V. The overall performance enhancement is primarily due to reduced R_s and R_c with applied V_{bg}, resulting in an increase in I_d.[18] This observation confirms that the performance of NW FETs with undoped S/D is significantly limited by the contact and series resistances.

In Fig. 3(a), we show the output (main panel) and subthreshold (inset) characteristics for a NW FET, where the NW sections not covered by the top-gate were B-doped us-

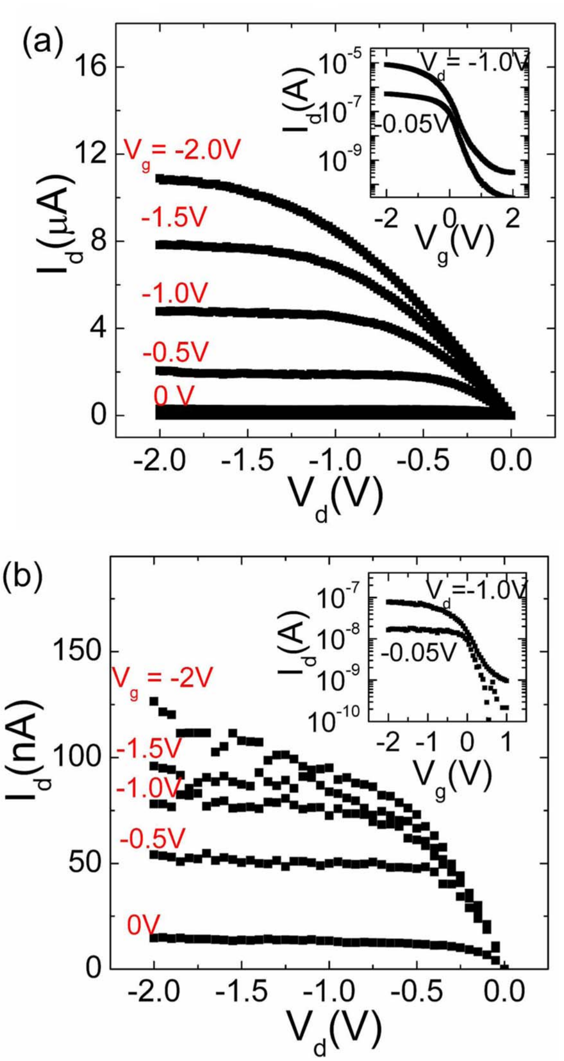

FIG. 3. (Color online) (a) I_d vs V_d data measured at different V_g values for a Ge–Si_xGe_{1-x} core-shell NW FET with doped S/D. Inset: I_d vs V_g measured at different V_d values for the same device. (b) The I_d vs V_d data of Fig. 2 measured at $V_{bg}=0$ V for a Ge–Si_xGe_{1-x} core-shell NW FET with undoped S/D are shown for comparison. Inset: I_d vs V_g data of the same device. The devices of panels (a) and (b) have similar channel lengths, $L_g=720$ nm.

ing low (3 keV) energy ion implantation at a dose of 1×10^{15} cm^{-2}. The NW diameter is 36 nm, and the device dimensions are $L_g=720$ nm and $L_s=850$ nm. The implant-induced damage in the Ge crystal structure can be removed after a short anneal at 400 °C, thanks to a faster defect removal and regrowth velocity than Si.[19] For the above implant conditions, we expect a doping concentration of $10^{19}-10^{20}$ cm^{-3} in the NW sections not covered by the top-gate and a corresponding resistivity (ρ) of $2.56\times10^{-3}\pm1.9\times10^{-4}$ Ω cm.[17] Furthermore, the high B-doping level also translates into low Ni/NW specific contact resistivity values of $1.1\times10^{-9}\pm2.2\times10^{-10}$ Ω cm^2 and corresponding R_c values of 300 ± 200 Ω.[17] Based on these data, the estimated value of external resistance R_s+R_c for the NW FET with B-doped S/D in Fig. 3(a) is 21.7 ± 1.8 kΩ. The NW FET with doped S/D in Fig. 3(a) shows a maximum current of $I_{max}=11$ μA measured at $V_g=-2.0$ V and a subthreshold slope of SS=270 mV/decade. The SS value is relatively high compared to the thermal limit of 60 mV/decade and could stem from a high interface trap density. The ON current has a value $I_{on}=2$ μA at $V_d=-1.0$ V, corresponding to an I_{on}/I_{off} ratio of ~200. For comparison, in Fig. 3(b) we show the output (main panel) and subthreshold (inset) characteristics for the NW FET with undoped S/D at $V_{bg}=0$ V, examined in Fig. 2. Note that the two devices in Fig. 3 have similar L_g and L_s dimensions. Compared with the undoped S/D NW FET in Fig. 3(b), the I_{max} of the top-gated device with B-doped S/D is two orders of magnitude larger, and the I_{on}/I_{off} ratio shows a tenfold increase. Clearly, the device performance is enhanced after S/D B-doping. The device resistance R_m measured at $V_g=-1.0$ V in the linear (small V_d) regime is 130 kΩ. Using $R_m=R_c+R_s+R_{ch}$ along with estimates for R_c and R_s, R_{ch} is estimated to be ~108 kΩ. Thus, R_c and R_s are small relative to R_{ch}, and the operation of our Ge–Si_xGe_{1-x} NW-FET is now primarily limited by R_{ch} rather than R_c and R_s. The corresponding effective mobility, extracted using the calculated gate capacitance per unit length of $C_{ox}=0.95$ nF/m, is $\mu_{eff}=60$ cm^2/V s.

In summary, we demonstrate a dual-gated Ge–Si_xGe_{1-x} core-shell NW-FET with B-doped S/D using ion implantation. The device shows an enhanced performance with respect to NW FETs with undoped S/D, thanks to reduced series and contact resistances combined with efficient carrier injection from the doped S/D.

We acknowledge I.B.M. T. J. Watson Research Center for support. This work was funded by DARPA under Contract Nos. HR0011-08-1-0050 and N66001-07-12013.

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