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Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric

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We fabricate and characterize dual-gated graphene field-effect transistors using Al_2O_3 as top-gate dielectric. We use a thin Al film as a nucleation layer to enable the atomic layer deposition of Al_2O_3. Our devices show mobility values of over 8000 $cm^2/V\,s$ at room temperature, a finding which indicates that the top-gate stack does not significantly increase the carrier scattering and consequently degrade the device characteristics. We propose a device model to fit the experimental data using a single mobility value. © *2009 American Institute of Physics*.
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Graphene, a monolayer to few layers of sp^2 bonded carbon in a honeycomb lattice, has been studied intensively since its discovery in 2004 (Ref. 1) due to its unique electron physics, as well as possible applications to electronic devices. Graphene's high intrinsic carrier mobility (over 200 000 $cm^2/V\,s$ at low temperature for suspended samples),[2] combined with its mechanical and thermodynamic stability,[3] makes it a promising material for nanoelectronic devices.

The fabrication of graphene-based field-effect transistors (FETs) requires a uniform gate dielectric deposition technique on graphene with high dielectric constant (κ) and reduced interface states density. It is well known that the existence of a mechanically and chemically stable native oxide for silicon, SiO_2, has been key to the success of silicon-based microelectronics. Highly insulating SiO_2 grows on Si by thermal oxidation,[4] and the interface between Si and SiO_2 has almost close-to-ideal properties.[5] Atomic layer deposition (ALD) is a well developed technique used for growing high-*k* gate dielectric layers, thanks to its precise control over the film thickness and uniformity.[6] However, the direct deposition of high-*k* dielectric materials, such as Al_2O_3 and HfO_2, on graphene using H_2O-based ALD is not possible because of the hydrophobic nature of graphene basal plane.[7] Given that a perfect graphite surface is chemically inert,[8] attempts to grow ALD Al_2O_3 layer on a *clean* highly oriented pyrolytic graphite surface lead to a selective growth at the steps between graphite layers, where the broken carbon bonds along the terraces serve as one-dimensional nucleation center for the initial ALD process.[9] Therefore, the deposition of high-*k* dielectric materials on graphene has been relatively limited so far.

Previous studies used surface treatments of the graphene surface in order to allow ALD growth. Examples include NO_2 functionalization,[10] O_3 functionalization,[7] and perylene tetracarboxylic acid coating,[11] or simply nucleating the dielectric growth from impurities on graphene without prior cleaning.[12] The carrier mobility on top-gated graphene devices is significantly degraded after Al_2O_3 dielectric deposition using NO_2 functionalization.[10] In addition, Lemme *et al.*[13] showed a significant degradation in graphene carrier mobility with more than an 85% decrease for both electrons and holes when an evaporated SiO_2 layer was used as a top-gate dielectric.

Here we report the realization of a top-gated graphene FET with a high-*k* dielectric layer grown by ALD and with minimal carrier mobility degradation with respect to a graphene layer without a top dielectric. In order to deposit the Al_2O_3 dielectric, we introduce a thin nucleation layer of oxidized Al between the graphene layer and the dielectric. The electrical characteristics of top-gated FETs fabricated using this technique indicate a high, above 8000 $cm^2/V\,s$, carrier mobility at room temperature after top-gate processing. We develop a simple device model including the effect of quantum capacitance, which agrees well with the observed transport characteristics and provides the extracted value of mobility, initial charge density, and contact resistance of devices.

The key idea enabling the high-*k* dielectric layer growth on graphene by ALD is to provide intentional nucleation sites on the inert surface of graphene. Prior to the Al_2O_3 layer growth by ALD, we deposit a 1–2 nm thick Al layer on the graphene surface by e-beam evaporation [Fig. 1(a)]. After the Al deposition, the samples are taken out in air and transferred to the ALD chamber for the deposition of Al_2O_3 using trimethyl aluminum as the Al source and H_2O as oxidizer. Based on x-ray photoelectron spectroscopy and electrical measurement results, the Al nucleation layer is completely oxidized as soon as the sample is exposed in air to be transferred to ALD chamber.[14] In addition, the initial stage of ALD growth starts with an H_2O oxidizing cycle at elevated temperatures to further complete the oxidation step.[15]

The graphene monolayer flakes used in this work are exfoliated from bulk natural graphite crystals by the micromechanical cleavage. The substrate consists of a highly doped *n*-type Si (100) wafer with an arsenic doping concentration of $N_D > 10^{20}$ cm^{-3}, on which a 300 nm thick SiO_2 layer is grown by thermal oxidation. The low resistivity sub-

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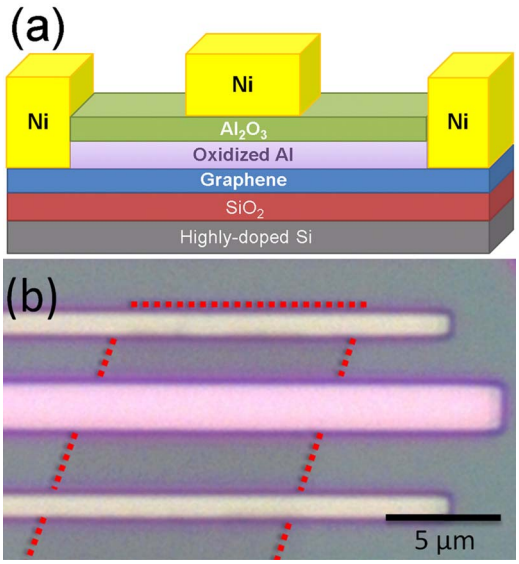

FIG. 1. (Color online) (a) Schematic of dual-gated graphene FET structure. (b) Optical microscope image of a graphene FET.

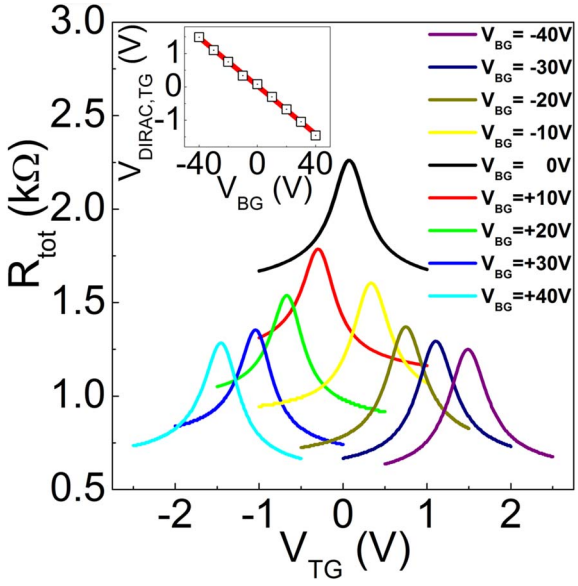

FIG. 2. (Color online) R_{tot} vs V_{TG} data measured at different V_{BG} values. The inset shows the position of $V_{Dirac,TG}$ at different V_{BG}.

strate allows global back-gate operation. The thickness of the exfoliated layers was measured by a combination of optical contrast of the graphene samples,[16] thickness measurement by atomic force microscopy, and Raman spectroscopy[17] to ensure that monolayer flakes are selected for device fabrications. We define metal contacts on the sample using electron beam lithography followed by a 50 nm thick metal (Ni) layer evaporation and a lift-off process. After annealing in a hydrogen atmosphere at 200 °C, which allows the removal of contaminants such as resist residues,[18] the device is transferred to an e-beam evaporator vacuum chamber to deposit the Al nucleation layer. Then, the samples are moved to the ALD chamber and go through 167 cycles of Al_2O_3 deposition, resulting in a 15 nm thick Al_2O_3 film deposition. A 50 nm thick Ni top-gate electrode is subsequently fabricated using e-beam lithography, metal deposition, and lift-off. An example of optical microscope image of a FET with 6.6 μm source-drain separation and 2.4 μm top-gate length is shown in Fig. 1(b).

The transport characteristics of the device are measured at room temperature in a vacuum probe station. The top-gate electrode and the Si substrate are used as a local gate and global back-gate, respectively, and control the carrier concentration and polarity in the graphene layer. Figure 2 shows the total device resistance (R_{tot}) as a function of top-gate voltage measured at different back-gate biases from −40 to 40 V and at a drain bias of V_D=0.1 V. Without an applied back-gate bias (V_{BG}=0 V) the sample resistance reaches a maximum (Dirac point) at $V_{Dirac,TG}$=0.08 V. This observation indicates that there is little unintentional doping of the graphene sample[19] after the top-gate stack deposition. As $|V_{TG}$-$V_{Dirac,TG}|$ increases, the electron or hole concentration in the graphene channel increases and R_{tot} decreases, resulting in Λ-shaped traces. The top-gate hysteresis is smaller than 0.05V, and the leakage current through the Al_2O_3 top-gate dielectric is less than 0.75 pA/μm^2. These observations indicate a high dielectric quality and a low ($<$9.4 $\times 10^{10}$ cm^{-2}) interface state density.

Figure 2 data show R_{tot} versus V_{TG} measured at different V_{BG} values. An applied V_{BG} bias changes the position of the Dirac point and also shifts vertically the measured resistance values. The change in the Dirac point position can be explained as follows: a positive (negative) V_{BG} bias induces a finite concentration of electrons (holes) in the active area, proportional to the back-gate capacitance (C_{BG}). In order to restore the device to the Dirac point, where the carrier concentration is minimum, a negative (positive) applied V_{TG} is required. The vertical shift is caused by the resistance change in the un-top-gated regions of the graphene flake. The position of the minimum conductivity points in terms of V_{TG} and V_{BG} is shown in the inset of Fig. 2. The slope represents the ratio between the top-gate and back-gate capacitances, $C_{TG}/C_{BG} \approx 28$. Using the back-gate capacitance value of C_{BG}=11 nF/cm^2, the top-gate capacitance is estimated to be C_{TG}=306 nF/cm^2, corresponding to a relative dielectric constant of 6.0 for the Al_2O_3 film.

We now present a model for the device characteristics in Fig. 2. The carrier concentrations (electrons or holes) in the graphene channel regions n_{tot} can be approximated by

$$n_{tot} = \sqrt{n_0^2 + n[V_{TG}^*]^2}, \tag{1}$$

where n_0 represents the density of carriers at the minimum conductivity, Dirac point. The residual carrier concentration n_0, which for an ideal, disorder-free graphene layer should be zero, is generated by charged impurities[20] located either in the dielectric or at the graphene/dielectric interface. $n[V_{TG}^*]$ represents the carrier concentration induced by the top-gate bias away from the Dirac point, $V_{TG}^* = V_{TG} - V_{TG,Dirac}$. The expression for $n[V_{TG}^*]$ is obtained from the following equation relating V_{TG}, C_{ox}, and the quantum capacitance of the two-dimensional electrons in the graphene channel:

$$V_{TG} - V_{TG,Dirac} = \frac{e}{C_{ox}} n + \frac{\hbar v_F \sqrt{\pi n}}{e}. \tag{2}$$

The total device resistance R_{tot} is given by

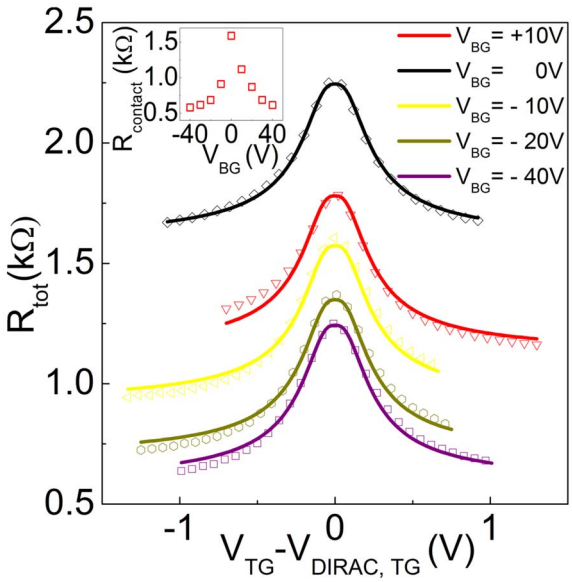

FIG. 3. (Color online) R_{tot} vs V_{TG}-$V_{Dirac,TG}$ at selected V_{BG} values (symbols) along with modeling results for each data set (lines). The inset shows the extracted contact resistance $R_{contact}$ vs V_{BG}.

$$R_{tot} = R_{contact} + R_{channel} = R_{contact} + \frac{N_{sq}}{n_{tot} e \mu} = R_{contact} + \frac{N_{sq}}{\sqrt{n_0^2 + n[V_{TG}^*]^2} e \mu}, \quad (3)$$

where $R_{channel}$ is the resistance of the graphene channel covered by top-gate electrode, the contact resistance $R_{contact}$ consists of the uncovered graphene section resistance and the metal/graphene contact resistance, and N_{sq} represents the number of squares of the top-gated area.

By fitting this model to the measured data of Fig. 2, we can extract the relevant parameters, n_0, μ, and $R_{contact}$. In Fig. 3 we show the measured (R_{tot}) versus V_{TG} (symbols), along with the model of Eq. (3) (solid lines). The modeling results agree well with the experimental data. Indeed, the data set of Fig. 3 can be fitted with a single value of the residual concentration $n_0 = 2.3 \times 10^{11}$ cm^{-2}, of the mobility $\mu = 8600$ cm^2/V s, and with different contact resistances, which depend on the applied V_{BG} (Fig. 3 inset).

We now discuss the extracted μ and n_0 values in our device in comparison with existing theoretical studies on graphene transport. Adam *et al.*[20] studied graphene transport in the diffusive limit using the Boltzmann transport formalism and calculated μ and n_0 as a function of a single parameter, the impurity concentration (n_{imp}) at the graphene/dielectric interface:[21] $\mu \cong 33e/(hn_{imp})$, and $n_0 \approx 0.2 \times n_{imp}$. According to the model of Adam *et al.*,[20,21] the extracted mobility value in our device $\mu = 8600$ cm^2/V s corresponds to an impurity concentration $n_{imp} \cong 1.0 \times 10^{12}$ cm^{-2}, which in turn would result in a residual carrier concentration $n_0 \approx 1.9 \times 10^{11}$ cm^{-2}, in good agreement with our experimental data. Lastly we discuss the temperature dependence of the transport data in our device. From 300 down to 77 K the carrier mobility is rather insensitive to temperature, showing a modest ~10% increase. This observation suggests that phonon scattering is relatively small and that the mobility is primarily determined by fixed impurity scattering.[22]

In summary, we fabricated a top-gated monolayer graphene device with an Al_2O_3 gate dielectric on its surface by ALD. The device characteristics are investigated in the dual-gate operation mode. Our data show that the overlaying Al_2O_3 layer does not substantially degrade the electrical properties of the graphene device. Our model, including quantum capacitance of graphene, agrees very well with our experimental results, and extracted mobility values are above 8000 cm^2/V s at room temperature. These results are very promising both for high speed FETs and also to enable non-conventional device designs in graphene.

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