

Scaling Properties of Ge–Si_xGe_{1–x} Core–Shell Nanowire Field-Effect Transistors

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Abstract—We demonstrate the fabrication of high-performance Ge–Si_xGe_{1–x} core–shell nanowire (NW) field-effect transistors with highly doped source (S) and drain (D) and systematically investigate their scaling properties. Highly doped S and D regions are realized by low-energy boron implantation, which enables efficient carrier injection with a contact resistance much lower than the NW resistance. We extract key device parameters, such as intrinsic channel resistance, carrier mobility, effective channel length, and external contact resistance, as well as benchmark the device switching speed and ON/OFF current ratio.

Index Terms—Core–shell, field-effect transistor (FET), nanowire (NW), silicon–germanium.

I. INTRODUCTION

RECENT years have witnessed remarkable progress in emerging research materials, such as semiconductor nanowires (NWs) or carbon nanotubes, as alternatives to conventional CMOS technology [1]–[5]. A key question with regard to such devices, relevant to both benchmarking potential application and gaining insight into fundamental electronic properties, is device performance scaling with channel length. For carbon nanotubes, it has experimentally been established that the nanotube resistance linearly scales with length for channel lengths larger than a few micrometers, where diffusive transport applies, and is independent of length for channel lengths smaller than 1 μm , in the ballistic transport regime [4]. Here, we present the first scaling study of high-performance germanium (Ge)—silicon–germanium (Si_xGe_{1–x}) core–shell NW FETs with highly doped source (S) and drain (D). The highly doped ($> 10^{20} \text{ cm}^{-3}$) S and D, which are realized using boron (B) ion implantation, enable efficient carrier injection with a contact resistance much lower than the NW resistance. The NW FET resistance linearly scales with the channel length down to 300 nm, indicating that the transport in these NWs is diffusive at room temperature.

Semiconductor NWs enable the realization of novel device geometries, such as gate-all-around FETs, which allow for more energy-efficient electronics at a given switching speed,

thanks to better electrostatic control of the channel [6]–[9]. Germanium and Ge–Si core–shell NWs have attracted interest as a platform for aggressively scaled FETs, due to Ge’s higher carrier mobility than Si and its compatibility with CMOS technology [10]–[12]. A main, albeit mundane, obstacle that has often impeded both an accurate electrical characterization and the realization of high-performance devices using nanomaterials is carrier injection. Generally, NW FETs employ metal contacts at the S and D terminals [13], [14], which limit the device performance because of the Schottky barrier existing at the metal–semiconductor interface. Moreover, ambipolar behavior is usually observed in such devices. The contact material that provides low contact resistance and unipolar carrier injection should be highly conductive, with a Fermi level aligned with the NW conduction or valence band, depending on the carrier type to be injected. A highly doped section of the same NW satisfies these conditions. NW doping with axial modulation can be achieved via the vapor–solid–liquid (VLS) growth mechanism [15], thermal diffusion from a dopant-containing molecule [16], and ion implantation [17]–[20]. Ion implantation allows for accurate axial doping control along the NW and is widely used in existing CMOS technology. Here, we employ low-energy ion implantation to realize NW FETs with highly doped S and D.

II. FABRICATION OF Ge–Si_xGe_{1–x} CORE–SHELL NW FETs

Our samples consist of Ge–Si_xGe_{1–x} epitaxial core–shell NWs. The core–shell NWs were grown in an ultrahigh-vacuum (UHV) chemical vapor deposition (CVD) chamber, via the VLS mechanism and using Au as a catalyst. First, the Ge core was grown at a total pressure of 5 torr and a wafer temperature of 285 °C using 60 sccm GeH₄ (10% diluted in He). Next, an epitaxial Si_xGe_{1–x} shell was grown in UHV conditions in the same chamber, by coflowing 7 sccm SiH₄ and 60 sccm of GeH₄ at a wafer temperature of 400 °C. Using transmission electron microscopy coupled with energy-dispersive X-ray spectroscopy we deduce the Si_xGe_{1–x} shell thickness of ~ 4 nm and a Si content in the shell of $x = 0.3$ [Fig. 1(b)]. The role of the Si_xGe_{1–x} shell is twofold. First, it acts as a passivation layer for the Ge surface, which is known to have a high density of interface traps in contact with a dielectric, and enables the realization of inversion layers in germanium. Second, due to a positive band offset between Si_xGe_{1–x} and the Ge valence band, it serves as a barrier and confines the holes in the Ge core. The UHV CVD *in situ* shell growth allows for the Si_xGe_{1–x} shell thickness and content to be

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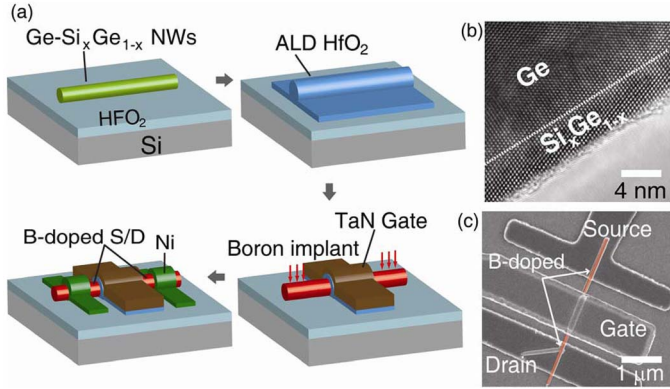


Fig. 1. Top-gated Ge-Si_xGe_{1-x} NW FET. (a) Schematic representation of a top-gated Ge-Si_xGe_{1-x} NW FET and fabrication flow. (b) Transmission electron micrograph of a Ge-Si_xGe_{1-x} core-shell NW, evincing a single-crystal shell epitaxially grown on the Ge core. (c) Scanning electron micrograph showing a top-gated NW FET device. The red regions represent the highly boron-doped NW sections.

engineered with minimum impurity incorporation. In particular, here we chose a reduced Si content, i.e., $x = 0.3$, to minimize the strain in the Ge-Si_xGe_{1-x} core-shell heterostructure while still maintaining the aforementioned interface passivation and hole confinement.

Fig. 1 shows a schematic of the top-gated NW FET with highly doped S and D [Fig. 1(a)], along with a transmission electron micrograph of the Ge-Si_xGe_{1-x} NW [Fig. 1(b)] and a scanning electron micrograph of the device [Fig. 1(c)]. The fabrication process flow is briefly described in the following. Post growth, the Ge-Si_xGe_{1-x} core-shell NWs were suspended in ethanol and dispersed onto a HfO₂ (10 nm)/Si (100 n-type) substrate. The wafer with dispersed NWs was then cleaned with a 2% hydrofluoric acid (HF) solution for 20 s and deionized water for 20 s for two cycles, before the gate oxide deposition. Next, a 9-nm-thick HfO₂ layer was deposited by atomic layer deposition at 250 °C. The equivalent oxide thickness of the deposited gate oxide was ~ 3.9 nm, evinced by the capacitance-voltage measurement on planar capacitors processed in parallel with the device. The gate electrode was defined by e-beam lithography (EBL), followed by 120 nm of tantalum nitride (TaN) deposition and liftoff. To remove resist residues, the device was cleaned with O₂ plasma for 10 s (50 W). The HfO₂ layer deposited on the S/D areas of the device was etched by diluted HF ($\sim 3\%$). Once the NW FET gate areas are defined, the samples are ion implanted with boron, which results in highly doped NW areas *outside* the TaN metal gate. The relatively thick TaN metal gate prevents the NW FET channel from B penetration. B-ion implantation was done at an ion energy of 3 keV, with a dose of 10^{15} cm⁻², and rotating 360° with 32° tilt during ion implantation. The devices then underwent a rapid thermal annealing process at 600 °C 5 min in an N₂ ambient to activate the implanted dopants. We expect that the implant-induced crystal damage in NWs be removed after activation annealing due to Ge's faster defect removal and regrowth velocity compared with Si [21]. Subsequently, the S/D contacts were defined by EBL, metal (Ni) deposition, and liftoff. A 1-min annealing process at 300 °C completes the NW FET fabrication. Based on a systematic study of the electronic properties (doping concentration and

mobility) of B-implanted Ge-Si_xGe_{1-x} core-shell NWs, we expect a doping concentration of 10^{19} - 10^{20} cm⁻³ in the B-ion-implanted sections of the NW, a NW resistivity of $2.6 \times 10^{-3} \pm 1.9 \times 10^{-4}$ Ω · cm, and a Ni-NW specific contact resistivity of $1.1 \times 10^{-9} \pm 2.2 \times 10^{-10}$ Ω · cm², corresponding to contact resistances of 300 ± 200 Ω [19]. This step is the key to enable efficient unipolar hole injection in the NW FETs, as well as low external contact resistance. To probe the scaling properties of Ge-Si_xGe_{1-x} NW FETs, we fabricated devices with different channel lengths, ranging from 300 nm to 1 μm.

III. RESULTS AND DISCUSSION

To characterize the devices, we measure either the drain current (I_d) as a function of the drain bias (V_d) at a constant gate bias (V_g) (output characteristics) or I_d versus V_g at constant V_d values (transfer characteristics). Fig. 2 shows I_d versus V_d and I_d versus V_g data, measured for several Ge-Si_xGe_{1-x} NW FETs with different channel lengths (L_g), from $L_g = 300$ nm to $L_g = 1$ μm. The NW diameters in these devices are similar, i.e., $d = 52 \pm 4$ nm. The drain current data normalized to the NW diameter d , namely, the output current per footprint, are shown on the right axis of the I_d - V_d graphs to facilitate a comparison of the device characteristics. Two observations are apparent from the data in Fig. 2. First, the device characteristics clearly show unipolar behavior, in comparison with Schottky metal-semiconductor contact devices, which typically exhibit ambipolar behavior. Second, the maximum attainable I_d and transconductance values proportionally increase with decreasing L_g . As L_g decreases from 1 μm to 300 nm, the maximum I_d measured at $V_d = V_g = -2.0$ V increases to 12, 22, and 45 μA, corresponding to the normalized currents of 240, 420, and 800 μA · μm⁻¹. The I_d - V_g transfer characteristics measured at $V_d = -1.0$ V show peak transconductance values g_m of 6.1, 11.5, and 19.6 μS with decreasing L_g from 1 μm to 300 nm. We note that the gate leakage current is below 10 pA in all measurements.

A main finding of our study is summarized in Fig. 3. Here we show the total NW FET resistance R_m , measured at small V_d as a function of the geometric channel length L_g , and at different gate overdrive values $|V_g - V_t|$, from 0.5 to 2.0 V. V_t represents the NW FET threshold gate voltage at which the inversion charge density in the channel is zero. The hole density per unit length p in the NW FETs is related to the gate bias via: $p = C_{ox} \cdot |V_g - V_t| \cdot e^{-1}$, where C_{ox} is the top-gate capacitance per unit length, and e is the electron charge. Fig. 3(a) shows that R_m , which is the sum of the channel resistance R_{ch} and the external S-D contact resistance R_{SD} , is *linear* as a function of L_g for all $|V_g - V_t|$ values. While this is simply a restatement of Ohm's law, the data indicate that transport is diffusive in the Ge-Si_xGe_{1-x} core-shell NWs at room temperature and allows us to decouple the channel and external contact resistances. The linear fits to R_m versus L_g data at various $|V_g - V_t|$ values have a common intercept, which represents the external contact resistance R_{SD} and the channel length reduction ΔL , namely, the difference between the geometric gate length L_g and the effective channel length L_{eff} [22]. The data in Fig. 3(a) correspond to $R_{SD} = 12.7$ kΩ and $\Delta L = 43$ nm. We note that R_{SD} represents the sum of the

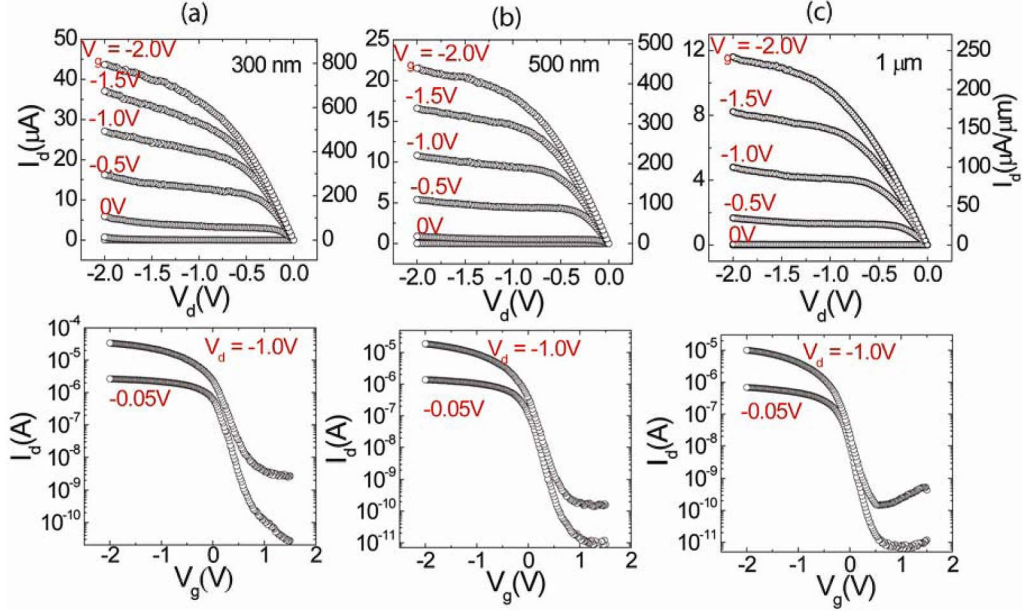


Fig. 2. Electrical characteristics of Ge-Si_xGe_{1-x} core-shell NW FETs at different gate lengths L_g . (a) $L_g = 300$ nm, $d = 55$ nm. (b) $L_g = 500$ nm, $d = 49$ nm. (c) $L_g = 1$ μ m, $d = 48$ nm. In each panel, the top (bottom) graphs show I_d versus V_d (I_d versus V_g) data, measured at constant V_g (V_d) values, as shown. The right y -axis of the top graphs show I_d normalized to the NW diameter.

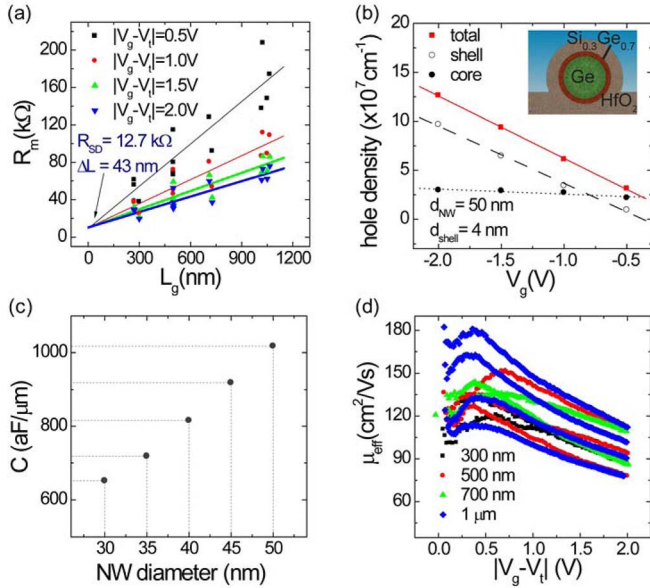


Fig. 3. Channel length resistance scaling and effective mobility extraction. (a) Measured device resistance R_m at $V_d = -0.05$ V versus L_g . The common intercept determines both the S-D external resistance $R_{SD} = 12.7$ k Ω and the effective channel length reduction $\Delta L = 43$ nm. (b) Total hole density versus gate voltage. The total hole density is the sum of the hole densities in the NW core and shell. (Inset) Schematic representation of the Ω -shape gate of Ge-Si_xGe_{1-x} NW FET). (c) Capacitance versus NW diameter. The capacitance values were calculated using the relation $C_{ox} = e \cdot (dp/dV_g)$. (d) Effective mobility of the Ge-Si_xGe_{1-x} core-shell NW FETs for four different channel lengths as a function of gate overdrive.

NW resistances of the highly doped section not covered by the top gate and the metal-NW contact resistance.

To determine the effective mobility in our NW FETs the C_{ox} values are first self-consistently calculated using Sentaurus TCAD simulation (Synopsys). The device structure used in simulations is shown in Fig. 3(b) (inset). It consists of a Ge core

of varying size, a 4-nm-thick Si_{0.3}Ge_{0.7} shell, and with a HfO₂ dielectric/TaN metal stack corresponding to the actual device. Applying a negative gate bias initially induces holes in the Ge core, and at a sufficiently large gate bias, holes start to populate the Si_{0.3}Ge_{0.7} shell.

Fig. 3(b) shows an example of the hole densities in the core and shell calculated for a Ge-Si_{0.3}Ge_{0.7} core-shell with a 50-nm diameter and a 4-nm-thick shell. We assumed an offset of 0.2 eV between Si_{0.3}Ge_{0.7} and Ge valence bands [23], [24]. Fig. 3(c) provides the results of the Ω -shape NW FET gate capacitance calculation. The total hole density per unit length in a Ge-Si_xGe_{1-x} NW for a given gate voltage is the sum of the carrier densities in the NW core and shell [Fig. 3(b)]. The p -values are related to C_{ox} and V_t by $e \cdot p = C_{ox} \cdot |V_g - V_t|$, where e is the electron charge. Thus, the total capacitance per unit length is extracted from the equation $C_{ox} = e \cdot (dp/dV_g)$. Fig. 3(c) shows the C_{ox} values calculated for NWs with different diameters. Using the intrinsic channel resistance $R_{ch} = R_m - R_{SD}$ determined from Fig. 3(a), along with C_{ox} , we then extract the *intrinsic* carrier mobility in the Ge-Si_xGe_{1-x} core-shell NWs. The mobility value is calculated using $\mu_{eff} = L_{eff} \cdot [R_{ch} C_{ox} (V_t - V_g - 0.5V_d)]^{-1}$, with $V_d = -0.05$ V. The data in Fig. 3(d) show μ_{eff} as a function of $|V_g - V_t|$. The results in Fig. 3(d) reveal that the peak hole mobility ranges from 100 to 180 cm² · (V · s)⁻¹, which are values that are up to threefold higher than those of the Si p -MOSFETs with HfO₂ gate dielectric [25].

Two main figures of merit for logic devices are the ON- and OFF-state currents. The ON-state current I_{ON} determines the FET switching speed, whereas I_{OFF} determines the passive power consumed by a logic gate (e.g., an inverter). A high-speed low-power device should possess high I_{ON} and I_{ON}/I_{OFF} . To gauge these performance metrics for our Ge-Si_xGe_{1-x} core-shell NW FETs, we define the ON-state

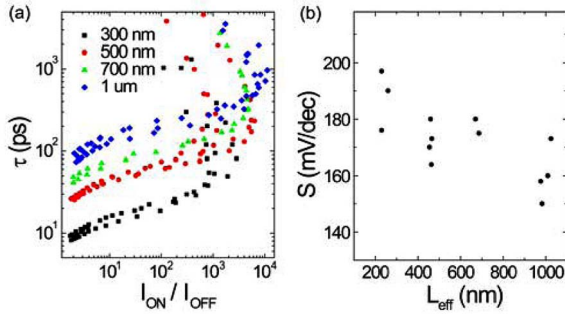


Fig. 4. Intrinsic gate delay and subthreshold slope. (a) Intrinsic gate delay versus I_{ON}/I_{OFF} ratio for different L_g values. (b) Subthreshold slope versus effective gate length.

current I_{ON} as the measured I_d at a gate bias $V_{ON} = V_t + (2/3)V_{dd}$, as well as the OFF-state current I_{OFF} as the measured I_d at $V_g = V_{OFF} = V_t - (1/3)V_{dd}$; the drain bias in both cases is $V_d = V_{dd} = -1.0$ V. To estimate the switching speed in our devices, we employ the intrinsic gate delay τ , which is defined as $\tau = CV/I$, where C is the gate capacitance, $V = V_{dd} = -1.0$ V, and $I = I_{ON}$ [26]. Fig. 4(a) shows the relation between τ and the I_{ON}/I_{OFF} ratio. Here, we define a window of $V_{ON} - V_{OFF} = V_{dd} = -1$ V along the V_g axis to determine I_{ON} and I_{OFF} . This graph illustrates the tradeoff between I_{ON}/I_{OFF} and τ , and it shows that τ decreases as L_g is scaled down. The I_{ON}/I_{OFF} ratio reaches a maximum of up to 10^4 , which is a tenfold higher value than previous results in Ge–Si core–shell NW FETs [12]. The subthreshold slope S , which is defined as $S = -[d(\log I_d)/dV_g]^{-1}$, for different channel lengths is shown in Fig. 4(b). These data show S values ranging from 150 to 190 $\text{mV} \cdot \text{dec}^{-1}$. The measured S values are higher than the thermal limit of 60 $\text{mV} \cdot \text{dec}^{-1}$, a finding that may be explained by a finite trap density at the dielectric–semiconductor interface. The S value increases as L_g is reduced, likely because of the short-channel effect. Finally, we note that the device performance can further be improved by optimizing the device fabrication process, namely, by reducing the nongated S and D regions, as well as by improving the dielectric quality.

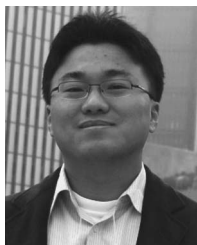
IV. CONCLUSION

We have demonstrated high-performance Ge–Si_xGe_{1-x} core–shell NW FETs with highly doped S/D and systematically investigated their scaling properties. Our data allow us to extract key device parameters, such as intrinsic channel resistance, carrier mobility, effective channel length, and external contact resistance, as well as to benchmark the device switching speed and ON/OFF current ratio.

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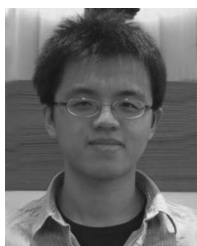
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