Thin-film tunneling transistors on flexible plastic substrates based on stress-assisted lateral growth of polycrystalline germanium

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Thin-film tunneling transistors on flexible plastic substrates based on stress-assisted lateral growth of polycrystalline germanium

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Stress-assisted Cu-induced lateral growth of polycrystalline germanium (poly-Ge) at temperatures as low as 150 °C has been exploited to fabricate thin-film tunneling transistors on flexible plastic substrates. Applying external compressive stress during annealing, leads to the lateral growth of poly-Ge from Cu-seeded drain/source regions, progressing into the channel area. A potential barrier is formed midway in the channel where the two lateral growth frontiers, emanating from source and drain seeded areas, meet each other. As confirmed by electrical measurements, the barrier is controlled by the gate bias. An ON/OFF ratio of 10^4 has been measured for these transistors, which shows the potential of these devices for switching applications. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1779946]

Thin-film transistors (TFTs) are the main driving components in display fabrication technology. The driving efficiency of these transistors is a prerequisite directly affecting the conjoint operation of the display and the peripheral switching circuitry. In general, polycrystalline TFTs are preferred to amorphous devices, since the driving current is dependent on carrier mobility in semiconductor material, which is improved by crystallization. On the other hand, the crystallization step adds to the complexity and also the cost of the process, as high thermal budget annealing or similar steps may be required. Therefore, special attention should be paid to low-temperature crystallization techniques. In addition, reducing the crystallization temperature puts forth the chance of employing a variety of low-temperature low-cost plastic substrates, inducing an ever-increasing tendency in large-area electronics, especially in flexible display applications.

Miscellaneous approaches have been pursued for lowering the crystallization temperature of semiconductors, including the metal-induced crystallization (MIC),[1] metal-induced lateral crystallization (MILC),[2] and excimer laser annealing (ELA);[3] however, the reduced crystallization temperatures are still too high for many flexible substrates. In general, we believe that for such applications germanium is more promising than silicon due to its inherently lower crystallization temperature and higher carrier mobility. In the previous works, Al (Refs. 4–6) and Cu-induced[7,8] crystallization of Ge have been studied. Though achieving reasonably low crystallization temperatures, Al incorporation degrades the semiconductor properties due to metal contamination; on the other hand, Cu-MIC of Ge needs temperatures as high as 400 °C. We have recently devised a stress-assisted Cu-induced crystallization technique that reduces the crystallization temperature of Ge to a minimum of 130 °C, as well as maintaining a sufficiently low metal contamination.[9] In this technique, mechanical compressive stress is externally applied to the flexible plastic substrate during annealing by inward bending of the substrate. We have fabricated record high-mobility depletion mode polycrystalline Ge (poly-Ge) TFTs on plastic with an upper process temperature of 130 °C, exploiting the mentioned technique.[10]

In this letter, we report the fabrication of poly-Ge tunneling TFTs on flexible plastic substrates, employing stress-assisted Cu-induced lateral crystallization of Ge. Although MILC of Si has been reported with Ni, Au, or Cu as the metal seeds,[2,11–13] no kind of lateral growth has been reported for Ge. We have observed that lateral growth of Ge is possible only in the presence of compressive stress and eliminating the mechanical treatment could not be compensated for by increasing the annealing temperature. In general, MILC offers a lower metal contamination and a higher quality of polycrystalline material with respect to device fabrication, in comparison with MIC. The major improvement offered by MILC is attributed to the capability of this technique for growing polycrystalline material with grain boundaries in a direction longitudinal to that of the desired current flow, whereas in MIC, the grain boundaries are randomly distributed.[14,15]

Sample preparation was performed by electron-beam (e-beam) deposition of a 1000 Å thick amorphous Ge (*a*-Ge) layer at a base pressure of 10^{-6} Torr and a substrate temperature of 100 °C, followed by e-beam deposition of a 2000 Å thick SiO_2 passivation layer at the same conditions. Flexible 100 μm thick polyethylene terephthalate (PET) films were used as substrates, which maintain their flexibility at temperatures below 180 °C. After patterning the SiO_2 layer by means of standard photolithography, a 100 Å Cu layer is deposited by thermal evaporation. This approach guarantees that during deposition, Cu cannot diffuse into the Ge layer at areas covered by SiO_2. The sacrificial SiO_2 layer is then removed by lift off, leaving the Cu-seeded islands on the *a*-Ge layer. The prepared samples are then subject to thermomechanical post-treatment at an annealing temperature of 150 °C. A 0.05% equivalent compressive strain is applied during annealing by bending the flexible PET substrates inward.

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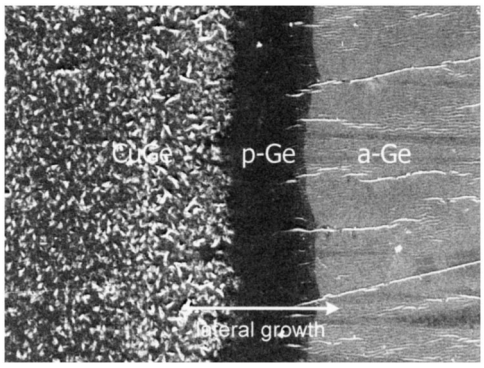

FIG. 1. SEM micrograph of the sample after being etched in an ammonia solution. The three regions of Cu-seeded Ge, 20 μm wide lateral growth strip and the remaining *a*-Ge are discernible in the graph.

Lateral growth of poly-Ge has been studied by scanning electron microscopy (SEM) analysis. The three distinct regions of the sample, CuGe, *p*-Ge, and *a*-Ge, can be delineated by etching with a thin ammonia solution for 10–20 s as shown in Fig. 1. Based on these images a growth rate of 2.5 μm/h was observed in the direction of the external stress axis. As seen in Fig. 1, accumulated stress leads to the formation of buckling sites in the *a*-Ge region, which could be minimized by the proper patterning of the *a*-Ge layer prior to thermomechanical post-treatment.[9]

The bright- and dark-field images of the lateral-growth region are given in Figs. 2(a) and 2(b), respectively. From these images, one can see that crystallites are placed in a parallel fashion. This direction of preferred growth is believed to be due to the lateral progress of the growth of germanium. The selected area diffraction pattern (SADP) of this region exhibits strong polycrystalline rings as given in the inset of Fig. 2(a).

The schematic of the TFTs fabricated on the basis of this material study is given in Fig. 3. The drain and source regions are the Cu-seeded areas from which the lateral growth emanates and progresses into the channel, as shown by the two arrows in Fig. 3. The two frontiers of lateral growth meet each other midway in the channel, also schematically sketched by a border in Fig. 3. We believe that a potential barrier is formed at this border due to the lattice mismatch as well as imperfections that may possibly lead to local depleted areas at this location. As a result, carriers need to tunnel across this potential barrier in order to form the drain–source current. This barrier can be controlled by the gate bias. Electrical measurements verify these speculations. The drain–source current is plotted versus the gate–source voltage for a constant drain–source bias of 5 V in Fig. 4(a). An ON/OFF ratio of about 10^4 is observed in the characteristic. The fast transition from the OFF to ON state is the best indication of the tunneling mechanism. Variations of the drain–source current versus the drain–source voltage are plotted for various values of the gate–source voltage in Fig. 4(b). It is observed that in the ON state, the drain–source current has a small dependency on the gate–source voltage, which could be explained by tunneling. We believe that, in essence, the basic operation of these tunneling transistors and the barrier control exerted by gate bias voltage is the same as the tunneling structure proposed by Sasajima *et al.*,[16,17] in which the gate bias controls the tunneling current through a 16 nm insulator locating between metallic drain and source

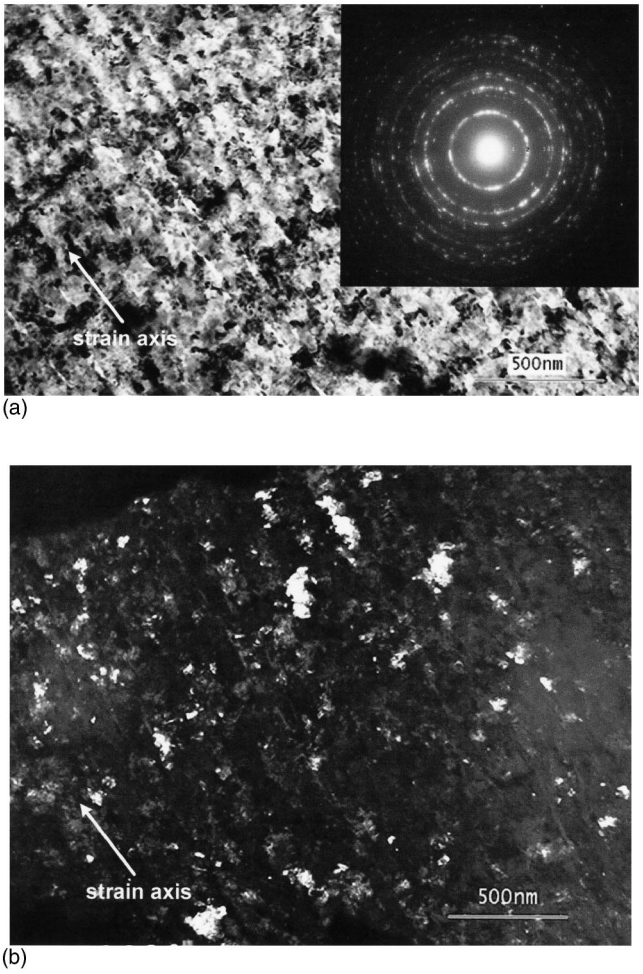

FIG. 2. Plan-view (a) bright- and (b) dark-field images of the lateral growth region, indicating that crystallites are placed in a parallel fashion. The inset of image (a) presents the SADP of the laterally grown poly-Ge strip.

regions. It is also worth mentioning that such a physical border may also form in the channel of TFTs fabricated by Ni-MILC of Si, resulting in mobility degradation and increase of the leakage current.[18,19] It has been argued that such a border is a long transverse grain boundary perpendicular to the lateral growth direction.[20] However, since no predominant tunneling behavior is observed in the Ni-MILC polycrystalline-Si TFTs, it may be concluded that this potential barrier is not sufficiently high and/or wide for the tunneling behavior to show up. In contrast, discernible tunneling

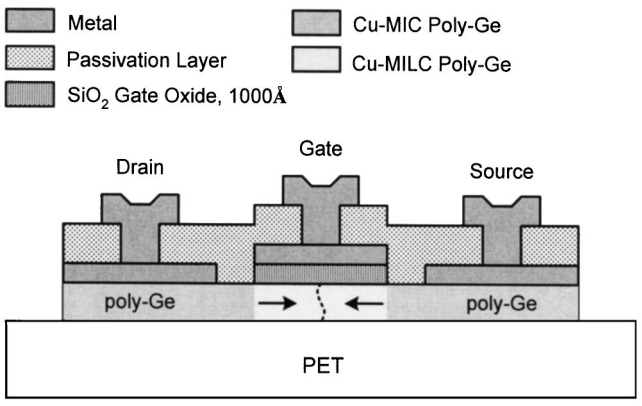

FIG. 3. The schematic cross section of the fabricated TFTs, showing the direction of the lateral growth and the border formed in the channel.

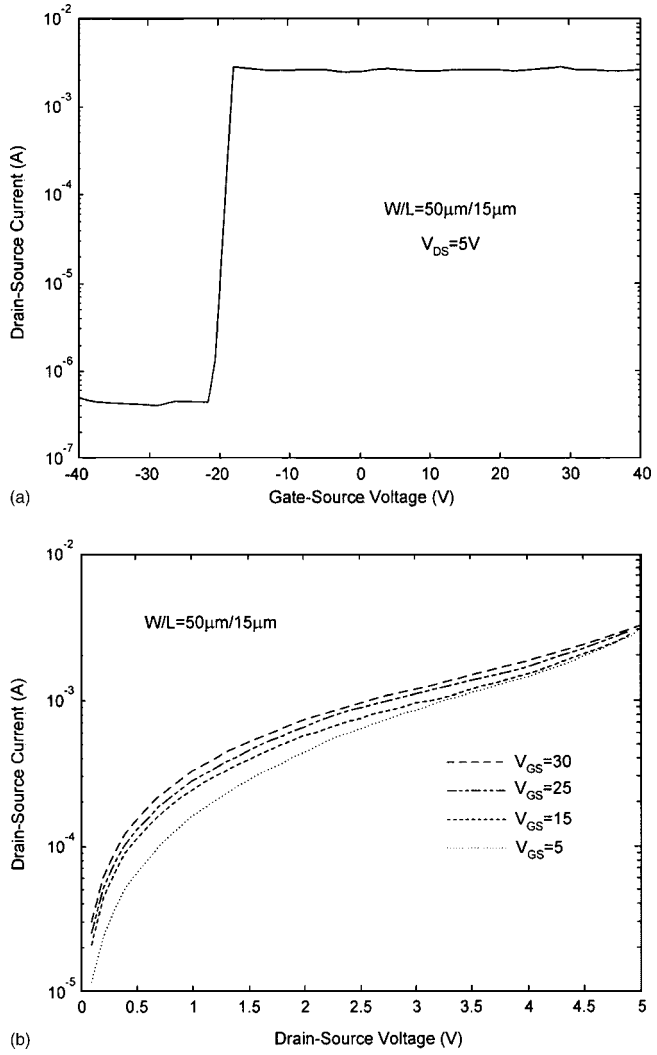

FIG. 4. (a) The I_D-V_{GS} characteristic of the TFTs at $V_{DS}=5$ V and (b) the I_D-V_{DS} characteristics for various values of gate–source bias.

effects are exhibited in stress-assisted Cu-MILC of germanium, implying the existence of a significant potential barrier. We speculate that this barrier boosting is motivated by the external stress, which may lead to the formation of a more defective transverse grain boundary at the border with potentially enhanced localized depleted areas and the partial disintegration of the Ge layer at this location. Further verification and characterization of the tunneling phenomenon is currently under study.

In summary, we have realized thin-film tunneling transistors on flexible PET substrates, taking advantage of the stress-assisted Cu-induced lateral growth of poly-Ge. The tunneling phenomenon occurs through the potential barrier formed in a channel where the two frontiers of lateral growth initiated from drain and source meet each other. An ON/OFF ratio of 10^4 and high driving current of 2 mA in the ON state show the potential of these devices for switching applications especially in flexible display technology.

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