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Unpinned metal gate/high-κ GaAs capacitors: Fabrication and characterization

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Fabrication of GaAs metal-oxide-semiconductor capacitors (MOSCAPs) with an unpinned interface is reported. The MOSCAP structure consists of a few monolayers of germanium grown in a molecular beam epitaxy (MBE) system in order to terminate an MBE-grown silicon-doped (100) GaAs layer. An *ex situ* HfO_2 high-κ dielectric with an equivalent oxide thickness of 12 Å was deposited by using a dc magnetron sputtering system. A midgap interface state density (D_{it}) of 5×10^{11} eV^{-1} cm^{-2} was measured using the high-frequency conductance technique. A rapid thermal annealing study was performed in order to examine the integrity of the gate stack at different temperatures. In addition, a forming gas anneal at 400 °C appears to significantly reduce the midgap D_{it} revealed by probing the frequency dispersion behavior of the MOSCAPs. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2234837]

Recently, GaAs-based structures have attracted a lot of interest in complementary metal-oxide semiconductor (CMOS) technology. The latest update released by International Technology Roadmap for Semiconductors (ITRS) has proposed III-V-based metal-oxide-semiconductor field-effect transistors (MOSFETs) as a potential candidate for "nonclassical" CMOS in order to extend scaling beyond the 45 nm technology node.[1] However, the lack of a compatible dielectric layer analogous to that of Si has been the main impediment to GaAs MOSFET technology. A poor dielectric interface due to a large D_{it} leads to Fermi-level pinning. Hence, a great deal of effort has been made to realize an unpinned oxide interface with GaAs. Recently, Passlack and coworkers have demonstrated *in situ* deposition of thermodynamically stable Ga_2O_3 and Ga_2O_3 (Gd_2O_3) dielectric films onto the GaAs surface in an ultrahigh-vacuum multichamber molecular beam epitaxy (UHV-MBE) system with a low D_{it}.[2,3] Furthermore, results on the fabricated enhancement-mode and depletion-mode MOSFETs by the same group tend to substantiate the viability of the *in-situ*-deposited oxide for MOSFET applications.[4,5] Alternatively, depletion-mode GaAs MOSFETs utilizing atomic layer deposition of an Al_2O_3 dielectric film provide a platform for introduction of *ex situ* deposited high-κ dielectrics into GaAs MOSFET technology.[6,7]

Among the developed high-κ dielectrics, HfO_2 appears to be a promising candidate for replacing SiO_2 in the current mainstream silicon technology as the oxide physical thickness approaches its practical limit. Furthermore, employing HfO_2 as a non-native dielectric has enabled fabrication of Ge MOSFETs with enhanced carrier mobility.[8,9] However, one drawback of HfO_2 is charge carrier mobility degradation due to remote Coulomb scattering.[10] It has been long believed that one can achieve an unpinned Fermi level at the oxide/GaAs interface by employing an interfacial buffer layer such as silicon between the insulator and GaAs layers.[11] Adopting this paradigm, we have demonstrated the fabrication of MOS capacitors with a sufficiently low D_{it} by employing an *in situ* termination of MBE-grown GaAs film by a very thin layer of Ge, followed by an *ex situ* deposition of HfO_2 dielectric. This approach eliminates the need for the *in situ* MBE deposition of high-κ dielectrics.

The inset of Fig. 1(a) shows a schematic cross section of a GaAs metal-oxide-semiconductor capacitor (MOSCAP) fabricated on an *n*-type MBE-grown GaAs layer. The growth of GaAs and Ge films was carried out by a Varian Gen 2 UHV-MBE system. The starting *n*-type (100) GaAs substrates were subjected to an *in situ* thermal oxide desorption at 580 °C. Then, a 500 nm Si-doped GaAs layer ($\sim 5 \times 10^{16}$ cm^{-3}) was grown at ~560 °C with a growth rate of 1 ML/s (monolayer per second). A streaky reflection high energy electron diffraction (RHEED) pattern indicates an atomically ordered and smooth GaAs surface.[12] Subsequently an *in situ* deposition of a 15 Å undoped Ge layer was performed at 300 °C. The RHEED patterns suggest that the Ge cap layer is amorphous. Atomic force microscopy (AFM) confirms the smoothness of the surface, giving rms roughness of 2 Å. After Ge deposition, the samples were removed from the MBE chamber and immediately transferred into a reactive dc magnetron sputtering system to deposit HfO_2 layer with a physical thickness of 65 Å verified by ellipsometry. Next, a postdeposition rapid thermal annealing (RTA) step was performed at 500 °C for 8 min in N_2 ambient in order to oxidize the dielectric layer, followed by a 2000 Å thick TaN metal-gate deposition. The MOS capacitor fabrication process was completed by a standard photolithography step and reactive ion etching of the TaN layer in CF_4 plasma ambient.

In order to probe the effect of the Ge interfacial buffer layer on MOSCAP characteristics, a control GaAs sample was prepared which underwent identical processing steps except the Ge cap layer deposition. Figure 1(a) illustrates the capacitance-voltage (*C-V*) curves of two identically processed samples with and without a Ge cap layer. For the sample without the Ge cap layer, the *C-V* curve is approximately flat, indicating a high D_{it} which, in turn, gives rise to the Fermi-level pinning effect, thereby causing this anomalous MOSCAP behavior. As it is apparent from Fig. 1(a), in the inversion region (negative gate bias regime) the value of minimum capacitance (C_{min}) for the sample without Ge in-

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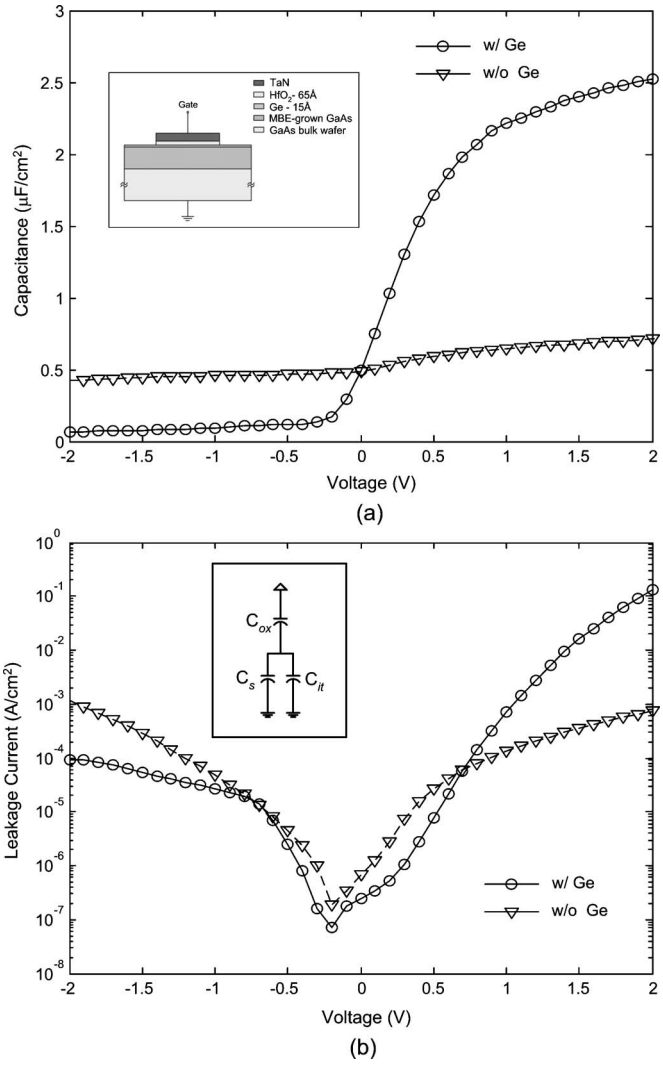

FIG. 1. Comparison of the samples with and without Ge interfacial buffer layer: (a) *C-V* characteristic and (b) leakage current density. The inset of (a) shows the schematic cross section of fabricated MOSCAP. The inset of (b) illustrates the generic *C-V* circuit model for a MOS structure.

terfacial layer is larger than that with Ge cap layer, whereas the MOSCAPs were fabricated on substrates with identical doping concentrations. According to the generic *C-V* circuit model for MOS structures,[13] these results imply that in the negative bias regime there exists a capacitor parallel to the substrate capacitor (C_s) which gives rise to this capacitance increase and is attributed to the interface trap capacitance (C_{it}) [see the inset of Fig. 1(b)]. The D_{it} appears to be significantly diminished by employing a thin Ge interfacial buffer layer, resulting in normal *C-V* characteristics at both accumulation and inversion. A comparatively low leakage current density of 3×10^{-4} A/cm^2 was achieved at 1 V for the sample with Ge film given in Fig. 1(b). *C-V* hysteresis of 270 mV was observed using a bidirectional *C-V* sweep (Fig. 2), which implies less-than-ideal quality of our sputtered high-κ dielectric possibly due to the presence of charge tapping sites. Further investigation is currently under way to improve the quality of this high-κ dielectric.

The inset of Fig. 2 shows the D_{it} measured using the conductance method. A standard *LCR* meter was used to measure conductance as a function of frequency with a signal level of 5 mV. A midgap D_{it} of 5×10^{11} eV^{-1} cm^{-2} was

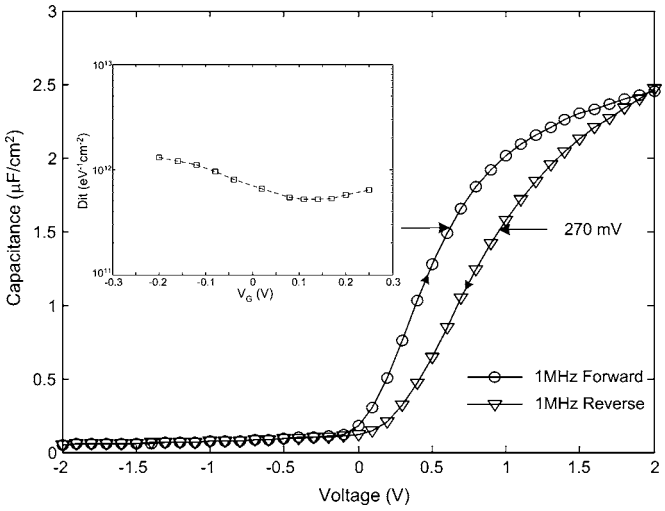

FIG. 2. The bidirectional *C-V* sweep presents a hysteresis of 270 mV. The inset shows the D_{it} measured using the high-frequency conductance technique.

evaluated from the $G_p(\omega)/\omega$ curve using the following expression:[14]

$$D_{\mathrm{it}} = \left(\frac{G_p}{\omega}\right)_{f_p} [qf_D(\sigma_S)A]^{-1}, \tag{1}$$

where f_D is a universal function of σ_s, A is the MOSCAP area, and f_p is the frequency at which $G_p(\omega)/\omega$ peak occurs. An equivalent oxide thickness of 12 Å was also extracted by using the NCSU CVC program.[15]

Next, the frequency dispersion behavior of MOSCAPs was examined. Distortion of the 100 kHz high-frequency *C-V* curve from the 1 MHz curve indicates the presence of midgap interface states as shown in Fig. 3(a). It is believed that midgap interface states drastically hinder the formation of an inversion layer due to the Fermi-level pinning effect. Figure 3(b) shows the *C-V* characteristics of the sample after a forming gas anneal at 400 °C for 30 min. This annealing step appears to be effective in reducing the midgap D_{it}. The voltage offset at the flatband due to the frequency dispersion effect was 50 mV after performing this annealing step. In order to further investigate the integrity of the gate stack during the rapid thermal annealing step, MOSCAPs were subjected to different annealing temperatures for 10 s in nitrogen ambient. In literature, Be^+ has been extensively reported as an appropriate *p*-type impurity in GaAs. However, different annealing temperatures have been reported for Be activation ranging from 700 to 850 °C.[4,16] The leakage current density has been monitored at different annealing temperatures shown in the inset of Fig. 3(a). Comparing the leakage current density of the annealed samples to that of the as-deposited samples reveals that the integrity of the gate dielectric is preserved upon performing the rapid thermal anneal at 700 °C. Further work for realization of enhancement-mode *p*-type MOSFET (*p*MOSFET) is currently in progress.

In summary, we have demonstrated unpinned Fermi-level GaAs MOSCAPs, accomplished by an *in situ* deposition of Ge cap layer onto a silicon-doped MBE-grown GaAs film. HfO_2 was deposited as the gate dielectric with an equivalent oxide thickness (EOT) of 12 Å. The D_{it} was 5×10^{11} eV^{-1} cm^{-2} as determined by the high-frequency conductance method. A forming gas anneal can effectively miti-

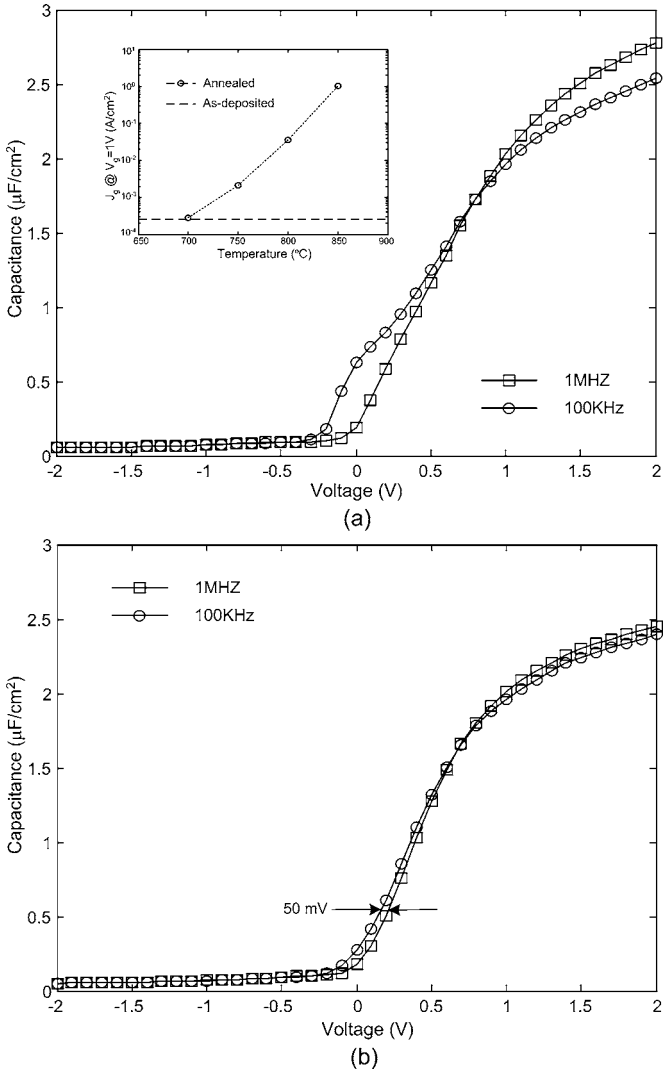

FIG. 3. Frequency dispersion behavior of the MOSCAP (a) as deposited and (b) after forming gas anneal at 400 °C for 30 min. The voltage offset at flatband was measured to be 50 mV after annealing step. Leakage current density at different annealing temperatures is given in the inset of (a), suggesting 700 °C as an appropriate temperature for Be^+ activation anneal.

gate the density of midgap interface states which are known to be the origin of the *C-V* curve distortion at different frequencies. A rapid thermal anneal study was also performed at different temperatures, which showed that the gate stack integrity is maintained up to 700 °C.

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