Vertical Flash Memory Cell With Nanocrystal Floating Gate for Ultradense Integration and Good Retention

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***Abstract*—We demonstrate a new vertical (3-D) Flash memory transistor cell with nanocrystals as the floating gate on the sidewalls that can form a high-retention ultrahigh density memory array. This scalable vertical cell architecture can allow a theoretical maximum array density of $1/(4F^2)$, where F is the minimum lithographic pitch, thus circumventing the integration density limitations of conventional planar Flash memory arrays. Discrete SiGe nanocrystals that are grown by conformal chemical vapor deposition process on the pillar sidewalls form the floating gate and render excellent retention properties at room temperature and at 85 °C. The cell shows a large memory window of ∼1 V and endurance of more than 10^5 cycles.**

***Index Terms*—Flash, memory, nanocrystal, pillar, retention, sidewall, vertical.**

I. Introduction

CONVENTIONAL planar Flash memory technology is widely considered to be facing serious challenges with integration density beyond the 45-nm technology node due to its large cell size, high applied voltages/fields for program/erase operations, and requirements on dielectric quality [1]. The fundamental physical limitations that are imposed by the high voltages in a scaled planar Flash transistor make it attractive to explore various 3-D cell architectures that can allow higher integration densities without compromising electrical reliability [2]. A pillar-shaped cell design is particularly suited to this end as it allows fabricating an inherently scalable cross-point array. Fabricated at the intersection of the bitlines and wordlines, each vertical cell can occupy an area nearly as small as $4F^2$ (F is the minimum lithographic pitch), with the array integration density scaling limited generally by the available lithographic capability [3]–[7].

Scaling the dielectric film thicknesses must be done concomitantly with scaling transistor dimensions to mitigate short-channel effects, which however compromises charge retention in an aggressively scaled memory cell with a continuous polysilicon floating gate. The use of nanocrystals as the floating gate circumvents charge-leakage issues because discrete nanocrystals provide immunity to local oxide defects, and Coulomb blockade and confinement effects on the stored electrons aid in the retention [8]. The use of thinner dielectrics also enables lower power operation and/or higher program/erase speed by virtue of stronger electrical coupling between the control gate, floating gate, and channel. In turn, the lower power requirements also allow reduction of memory module dimensions by almost half [9]. Additionally, integration of nanocrystal Flash to standard CMOS processing has been shown to require only 4 additional mask steps compared to the 11 steps that are required by continuous-gate Flash, rendering the former more attractive for CMOS/embedded process integration [9].

The motivation behind this letter is therefore to explore and demonstrate the vertical structure and nanocrystal charge storage in the same cell to circumvent the integration density limitations of planar Flash memory technology. First, the separate advantages of the twin concepts that are outlined previously are amalgamated in the vertical nanocrystal floating-gate Flash cell. Moreover, when scaled to dimensions of sub-100 nm, despite the smaller overall cell size, the device can benefit from enhanced drive current by virtue of larger channel width and fully depleted body, implying a faster read operation. The larger width would also help lower cell-to-cell variability of the threshold voltage, which is a manufacturing concern for planar nanocrystal Flash [10]. A larger memory window and enhanced retention properties resulting from the "classical bottleneck effect" and quantum confinement effects of an ultranarrow channel are also expected benefits in a scaled implementation of this design [11]. Finally, doping profile engineering and/or SiGe incorporation in the channel for channel-initiated secondary electron programming are potential advantages, making this cell design attractive for future scaling of Flash memory technology [12].

II. Fabrication

Photolithographic patterning and reactive ion etching (RIE) vertical rectangular mesas on p-type ⟨100⟩-oriented Si wafers formed the basis of the gate-all-around transistors with sidewall channel (Fig. 1). Various channel lengths were defined by the time of etch (and subsequent implantation energy), while the gate area was lithographically defined. RIE sidewall damage was minimized with sacrificial (in the range of 4–10 nm)

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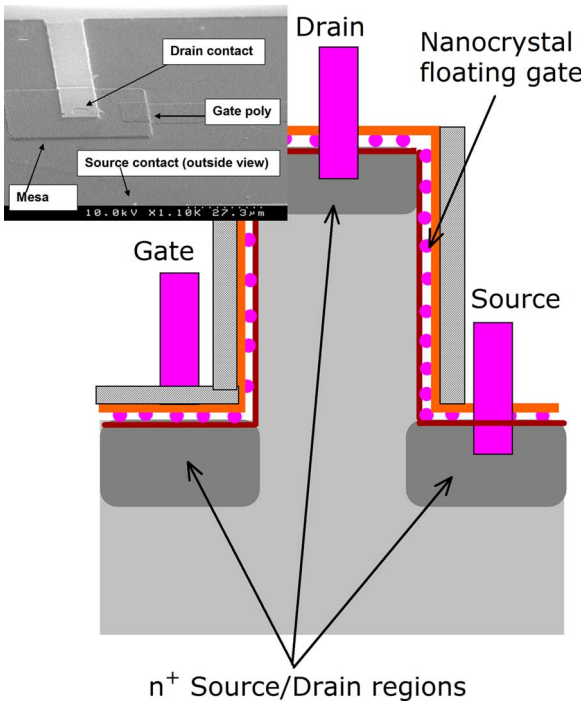

Fig. 1. Schematic side view of the vertical Flash transistor. (inset) Scanning electron micrograph of a cell (isometric view).

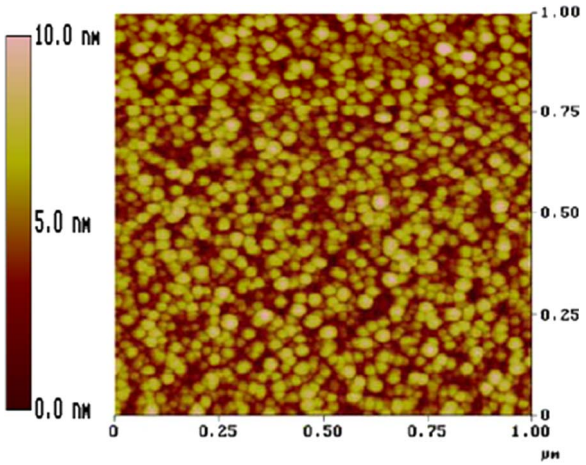

Fig. 2. $1 \times 1\ \mu m^2$ AFM scan of SiGe nanocrystals on planar oxidized Si surface. The nanocrystal size, density, and distribution are expected to be similar on the oxidized sidewalls as they are self-assembled by Volmer–Weber growth in a conformal CVD process (obviously, gravitational forces are irrelevant here).

thermal oxidation and dilute-HF etch step, followed by sacrificial protective low-pressure chemical vapor deposition (LPCVD) of silicon nitride layer on sidewalls. The wafers were then implanted with phosphorus (in the range of 15–20 keV with 7° tilt and 90° rotation) to form the drain at the top of the mesa and the self-aligned source at the base. The subsequent conformal growth of the gate stack on the sidewalls included a 4.5-nm thermal (tunnel) oxide, rapid thermal chemical vapor deposition (CVD)-grown SiGe nanocrystals, followed by 15 nm of LPCVD control oxide. The self-assembled nanocrystals/quantum-dots, which are characterized on the planar surface with atomic force microscopy (AFM)

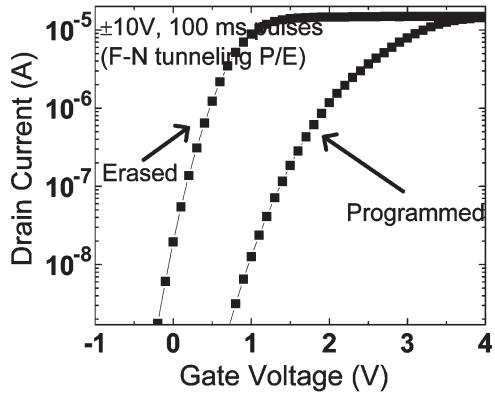

Fig. 3. Transconductance in programmed/erased states (±10-V 100-ms Fowler–Nordheim (F–N) tunneling program/erase) (Mesa height = 0.9 μm, width = 30 μm, $T_{\mathrm{Tox}} = 4.5$ nm, $T_{\mathrm{Cox}} = 15$ nm).

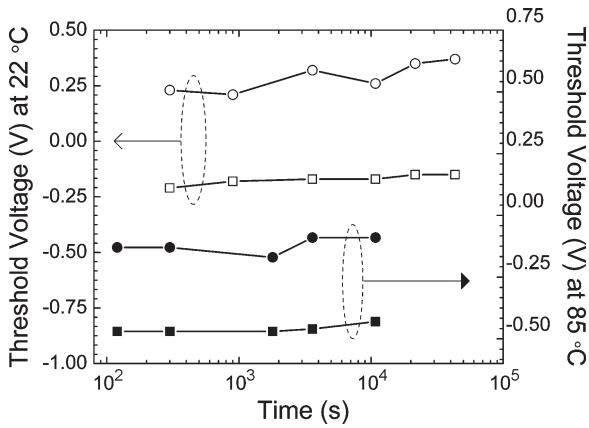

Fig. 4. Memory retention characteristics of virgin devices (solid symbols/left axis) at room temperature and (hollow symbols/right axis) at 85 °C, with ±8-V 100-ms F–N tunneling program/erase.

(Fig. 2) had diameters in the range of 7–10 nm and a density of $\sim 10^{11}$ cm^{-2}, and contained 16% Ge in Si. With a narrower band gap compared to Si, SiGe provides a deeper quantum well for the stored charge while allowing a low-thermal budget (120 s at 520°) and fully silicon-compatible growth process [13]. The gate polysilicon layer was deposited by LPCVD, implanted, and etched to form the gate electrode. After depositing an isolation oxide, electrical contacts to the drain at the mesa top, the source at the mesa base, the substrate on the back side of the wafer, and the gate on the sidewalls were finally formed by aluminum sputtering.

III. Results and Discussion

The transconductance of a Flash memory transistor is presented in Fig. 3. The devices were programmed and erased with ±10-V 100-ms pulses, whereby a large memory window = 1 V is observed. Memory (charge) retention characteristics at room temperature and at 85°C are presented in Fig. 4, where a stable and wide memory window is seen to be maintained. Fig. 5 shows that the device endures for more than 10^5 cycles, although the memory window degrades beyond 10^4 cycles and gradually closes up. Control devices that are fabricated without the nanocrystals showed a much smaller (~0.1 V) hysteresis,

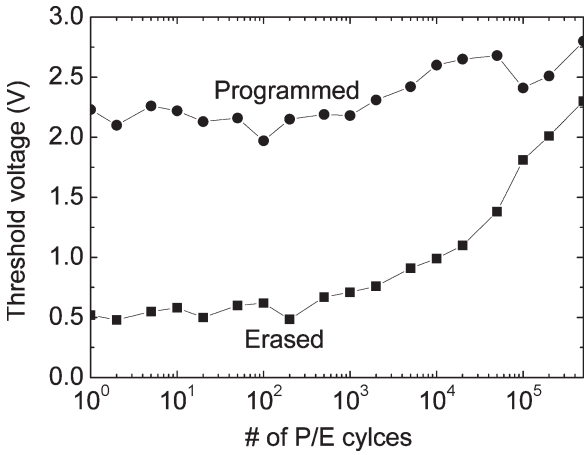

Fig. 5. Endurance of more than 10^5 cycles ($\pm$10-V 100-ms F–N tunneling program/erase). The relatively higher pulse amplitude that was applied, while maximally stressing the device, was most likely also responsible for electron trapping in the control oxide, causing the relatively higher threshold voltages.

implying that charge storage is indeed in the nanocrystals. As Puzzilli and Irrera have shown, the memory window movement and closure is most likely caused by gradual oxide degradation from generation and filling of traps with the tunneling program/erase stress of "standard cycling," during endurance testing [14], [15]. Optimization of control oxide quality and the pulsing scheme of endurance testing can possibly yield superior endurance characteristics.

IV. Conclusion

A vertical Flash memory architecture with nanocrystal floating gate is demonstrated as a possible pathway for continuing integration density enhancement of Flash memory technology. The vertical transistor design with its inherent advantages over the planar device is particularly suitable for Flash memory applications where a bank of identically sized cells is fabricated to form a regular array. The nanocrystal floating gate complements the dimensional scaling by providing excellent retention properties in spite of thinner dielectrics in the gate stack, helping circumvent the dimensional-scaling limitations of conventional planar Flash memory technology.

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