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Vertical flash memory with protein-mediated assembly of nanocrystal floating gate

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The authors propose and demonstrate a vertical flash memory device incorporating protein-mediated ordering of nanocrystal floating gate to help circumvent density scaling and/or performance limitations of planar flash memory with continuous floating gate. The scalability of the vertical architecture can allow the theoretical maximum array density of $1/4F^2$ (F: minimum lithographic pitch), thus circumventing the integration density limitations of planar flash transistor arrays. The nanocrystal floating gate renders reasonable retention, while the protein-mediated ordering of nanocrystals allows scalability and manufacturability. With tunneling program/erase, a memory window of 0.5 V, endurance $>10^5$ cycles, and retention beyond 10^5 s is reported. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2711528]

Flash memory technology has reached a critical juncture in terms of facing multiple challenges to its continued integration density scaling and reliability owing to its large cell size, high applied voltages for program/erase operations, and requirements on dielectric quality.[1] The fundamental physical limitations imposed by the electrostatics in a scaled planar memory transistor make it attractive to explore various three-dimensional cell architectures for enabling higher integration densities without compromising on electrical reliability.[2] A pillar-shaped vertical cell design described here (Fig. 1) is particularly suited to that end as it allows fabricating an inherently scalable cross-point array with each cell fabricated at the intersection of the bit lines and word lines, the cell thus occupying an area as small as $4F^2$ (F: minimum lithographic pitch), and limited generally by the available lithographic capability.[3] Further, the gate-all-around design of the pillar structure can allow maximum electrical coupling between the control gate and channel in a fully depleted body.[4]

Scaling the dielectric film thickness must be done concomitantly with scaling transistor dimensions to maintain adequate electrostatic control over the transistor channel (i.e., prevent short-channel effects), which, however, compromises charge retention in an aggressively scaled memory cell that has a continuous, polycrystalline silicon (polysilicon) floating gate.[5] The use of nanocrystals as the floating gate circumvents the charge-leakage issues by virtue of discreteness of nanocrystals and Coulomb blockade and confinement effects on the stored electrons.[6] Furthermore, stronger electrical coupling between the control gate, floating gate, and channel that is possible with the use of thinner dielectrics enables higher program/erase speed and/or lower power in nanocrystal flash.[7]

Traditional methods of nanocrystal formation on amorphous substrates with physical or chemical vapor deposition (CVD) proceed by the thermodynamics of annealing and atomistic nucleation dictated by surface kinetics, respectively. Owing to a lack of microscopic reproducibility of these processes, poor spatial ordering and size non-uniformity of nanocrystals are unavoidable. Thus, in a massively integrated array, a scaled memory cell is faced with relatively large fluctuation of electrons in its smaller ensemble of nanocrystals, which, in turn, causes a cell-to-cell variation of threshold voltages.[7,8] For manufacturability, minimizing the variation of threshold voltage across cells by controlling size, ordering, and density of nanocrystals is critical.[8,9] Toward that goal, we demonstrate the use of a protein-mediated self-assembly technique to deposit a regularly ordered array of uniformly sized, preformed nanocrystals on the oxidized sidewalls of the vertical flash cell.

Commercially available hydrophobically functionalized nanocrystals in a colloidal solution can be ordered into a regular array (Fig. 2) by exploiting properties of chaperonin protein molecules that self-assemble through noncovalent interactions.[10] Floating a wafer with oxidized silicon (SiO_2)

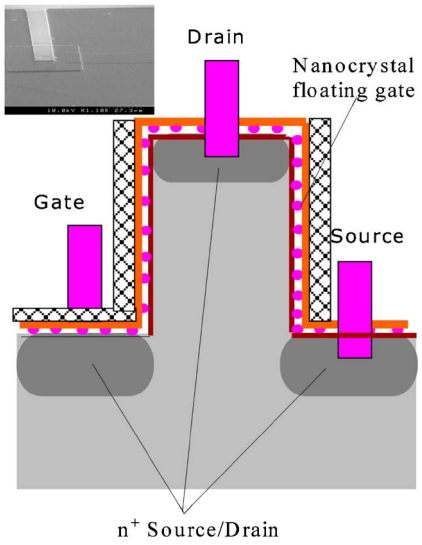

FIG. 1. (Color online) Schematic side view of vertical flash transistor and isometric scanning electron micrograph of a fabricated device (inset) showing the mesa with drain contact on its top and the polysilicon gate contact running to the right.

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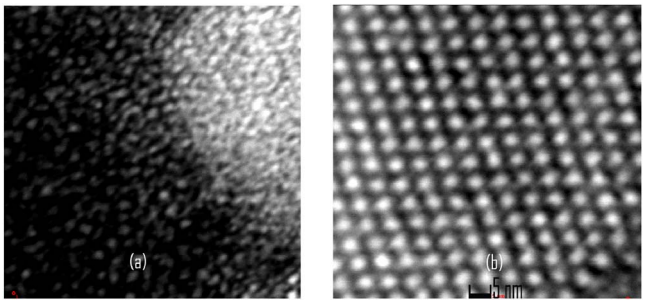

FIG. 2. (Color online) Scanning tunneling electron micrographs showing nanocrystals deposited (a) without and (b) with protein-mediated ordering of PbSe nanocrystals on a planar surface to produce a reasonably ordered array of nanocrystals. While it is difficult to obtain a micrograph from the vertical sidewall, one may expect the densities to be similar on the sidewalls considering the lack of a role of gravitational forces in the self-assembly process.

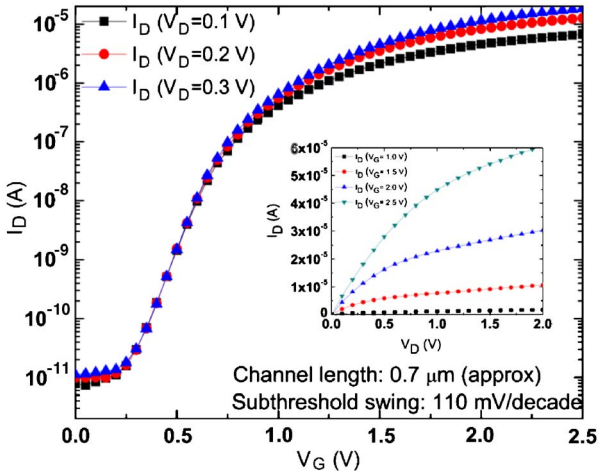

FIG. 3. (Color online) Vertical transistor transconductance and drain characteristics (inset) demonstrating the transistor functionality.

surface in phenyltriethoxysilane (PTS) solution causes formation of a self-assembled monolayer with the silane group at one end of PTS molecules covalently bonded to the SiO_2 surface. On subsequently floating the wafer in a chaperonin protein solution, the phenyl group at the other end of PTS molecules binds to the bottom side of the chaperonin cavities by hydrophobic-hydrophobic interactions. Consequently, the top side of the protein molecules is oriented to provide the ordered template for capturing nanocrystals. The donut-shaped chaperonin 60 (GroEL) protein used in this work has a cylindrical cavity diameter of 4.6 nm, wall thickness of 4.5 nm, and interior cavity surface that is hydrophobic. Consequently, preformed nanocrystals functionalized with hydrophobic molecules are trapped site specifically inside the protein cavities through hydrophobic-hydrophobic interaction. The devices are then annealed at 300 °C in air to oxidize the protein scaffold to carbon dioxide and water vapor. Calculations based on 100×100 nm^2 area squares and averaging indicate nanocrystal densities of $\approx10^{12}$ cm^{-2}. Detailed fabrication steps and mechanism of this self-assembly process are published elsewhere.[10,11] While the presence of Mg^{2+} and K^+ ions and adenosine triphosphate produce conformational changes in the chaperonin molecule altering its cavity size, the same can also be effected by genetically engineering the molecule.[12] Therefore, altering the chaperonin cavity size can be potentially used as a size filter for captured nanocrystals. The nanocrystal density is often tailored by choosing a protein molecule with suitable dimensions.[13]

The flash transistors were fabricated by reactive ion etching (RIE) vertical mesas from ⟨100⟩ *p*-type silicon wafers, followed by sacrificial oxidation, and its dissolution in dilute hydrogen fluoride to minimize sidewall damage/roughness from RIE. Conformal processes of dielectric deposition subsequently defined the gate-stack layers wrapping around the mesa, including 5 nm of thermal SiO_2 tunnel oxide, lead selenide (PbSe) nanocrystals 5 and 8 nm in diameter, and 20 nm of plasma-enhanced CVD SiO_2, finally capped with low-pressure CVD polysilicon. After an anisotropic RIE to define the polysilicon gate, the devices were implanted with phosphorus to form the drain at the mesa top and self-aligned source at the base, while also doping the gate polysilicon. Synopsys Taurus process simulations were used to optimize the implantation parameters (30 keV energy, 5×10^{15} cm^{-2} dose, 15° tilt, and 90° rotation) for suitably doping the source, drain, and sidewall gate with a single implantation step. Rapid thermal annealing for 60 s at 850 °C was used to activate the dopants, and contacts to the source, drain, and gate were formed by aluminum sputtering.

Figure 3 shows the transconductance and drain characteristics of the fabricated short-channel transistors. The memory characteristics were tested with tunneling program/erase by applying ±9 V, 100 ms gate pulses, resulting in a memory window (threshold shift) that saturated at ≈0.5 V. When plugged into[6]

$$\Delta V_T = \frac{qn_{\mathrm{nc}}x}{\varepsilon_{\mathrm{ox}}}\left(t_{\mathrm{control}} + 0.5\frac{\varepsilon_{\mathrm{ox}}t_{\mathrm{nc}}}{\varepsilon_{\mathrm{nc}}}\right) \tag{1}$$

along with a nanocrystal density $n_{\mathrm{nc}}=10^{12}$ cm^{-2}, $t_{\mathrm{nc}}=5$ nm, $\varepsilon_{\mathrm{nc}}(\mathrm{PbSe})=100\varepsilon_0$, $\varepsilon_{\mathrm{ox}}(SiO_2)=3.9\varepsilon_0$, $t_{\mathrm{control}}=20$ nm, and electronic charge q, it yields $x=0.54$ as the approximate number of electrons stored per nanocrystal, implying that a fraction of the nanocrystals are storing charge in these non-optimized devices. Control devices without nanocrystals did not exhibit a memory window, as was the case when nanocrystals with 8 nm diameter were deposited, the latter indicating that a 4.6 nm protein cavity size is inadequate to capture/scaffold the larger 8 nm nanocrystals on the vertical sidewalls. Stable retention of the memory cells beyond 10^5 s at room temperature is presented in Fig. 4, while fig. 5 shows endurance beyond 10^5 cycles.

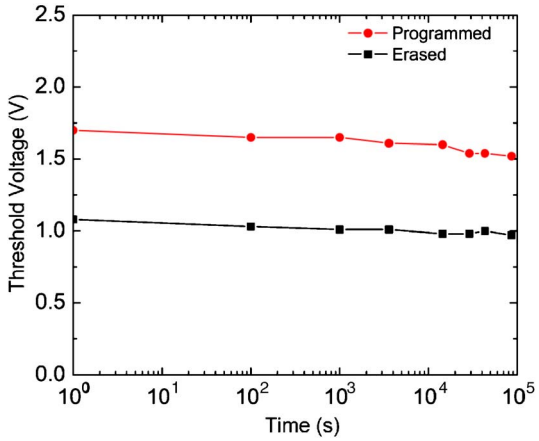

FIG. 4. (Color online) Retention characteristics at room temperature.

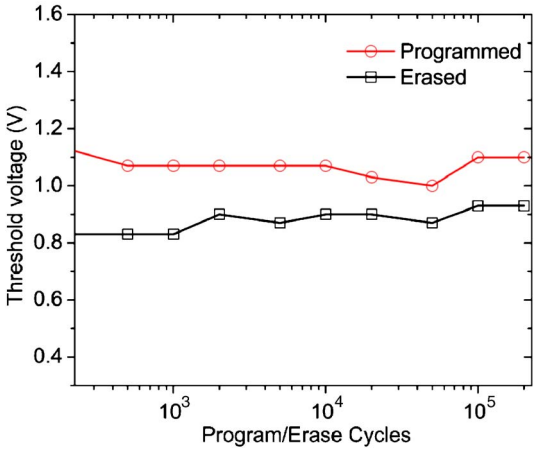

FIG. 5. (Color online) Endurance characteristics with ±9 V, 100 ms gate pulses for tunneling program/erase.

Deposition of preformed nanocrystals most likely precludes the occurrence of deep traps usually resulting from defect sites of CVD-grown nanocrystals, which also contribute to charge storage.[14,15] Consequently, electrons are stored in a quantum well of uniform depth (the nanocrystal conduction band) which, together with the uniform nanocrystal size and ordering, ensures a rather uniform threshold shift across cells. The semiconductor PbSe nanocrystals, available commercially with 4.5–9 nm diameters, were chosen for their compatibility with standard silicon processing, including thermal budget considerations of transistor fabrication. However, a wide variety of nanocrystal material systems, including other semiconductors and metals, have also been ordered into a regular array using similar protein-mediated assembly techniques.[10–13]

In conclusion, we have proposed and demonstrated a vertical flash memory device incorporating a nanocrystal floating gate ordered by protein-mediated self-assembly process. With this device design, the theoretical maximum array density, good retention characteristics of nanocrystal flash and control over nanocrystal ordering, size uniformity, and density are achievable.

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