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ABSTRACT

The development of a scalable and cost-effective nanofabrication method is of key importance for future advances in nanoelectronics. Thermal scanning probe lithography (t-SPL) is a growing nanopatterning method with potential for parallelization, offering unique capabilities that make it an attractive candidate for industrial nanomanufacturing. Here, we demonstrate the possibility to apply t-SPL for the fabrication of graphene devices. In particular, we use t-SPL to produce high performing graphene-based field effect transistors (FETs). The here described t-SPL process includes the fabrication of high-quality metal contacts, as well as patterning and etching of graphene to define the active region of the device. The electrical measurements on the t-SPL fabricated FETs indicate a symmetric conductance at the Dirac point and a low specific contact resistance without the use of any contact engineering strategy. The entire t-SPL nanofabrication process is performed without the need for masks, and in ambient conditions. Furthermore, thanks to the t-SPL *in situ* simultaneous patterning and imaging capability, no markers are required. These features substantially decrease fabrication time and cost.

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An important objective of the microelectronics industry is to fabricate high-performance miniaturized devices on a large scale at a low cost and with a high throughput. The exploration of new materials, fabrication methods, and device architectures underpins this objective. Of particular interest in recent years has been the study of electronic devices where the active material is monolayer graphene, due to its intriguing properties, including remarkable carrier transport,[1] high thermal conductivity,[2] and outstanding mechanical stability.[3] These properties have made graphene a promising candidate for a wide range of applications from flexible electronics to high-speed electronics.

The fabrication of graphene functional devices generally requires multiple patterning steps for defining the device active region and patterning metal contacts on graphene. Currently, electron-beam lithography (EBL) is the dominant technique for prototyping high-performance nanoscale devices out of graphene,[4–8] producing better quality devices than photolithography (PL).[9–11] However, the use of a focused electron beam in EBL is a major limitation in terms of cost, the electron beam induced sample damage and potential for parallelization to increase the throughput.

In recent years, novel nano-patterning techniques have been explored for fabricating nanoscale devices.[12–15] Among those, thermal scanning probe lithography (t-SPL) is an attractive choice for multiple reasons.[12,16–20] First, t-SPL is a maskless technique and is capable of patterning nanoscale features with sub-10 nm resolution.[17,21] Second, the entire t-SPL nano-patterning process can take place in atmospheric condition or N_2, which is a considerable advantage for achieving a cost-effective nano-patterning process. Third, t-SPL has a throughput comparable to EBL when using only one probe ($\sim 10^5\ \mu m^2\ h^{-1}$),[22] but by multiplexing with thermal nanoprobe arrays,[23] it could reach a much larger throughput. Finally, and more importantly, a recent study has demonstrated that t-SPL can pattern high-performing and low-resistance metal contacts on monolayer MoS_2.[24] However, the application of t-SPL for the fabrication of graphene devices remains largely unexplored. The objective of this study is, hence, to study the effectiveness of t-SPL for fabricating graphene devices.

Here, we report the application of t-SPL performed in ambient conditions for the fabrication of graphene field-effect transistors (GFETs). In particular, we study the electrical properties of monolayer graphene using a bottom-gated device structure with no

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encapsulation layer. In this device structure, monolayer graphene in both channel and contact regions is in direct contact with the t-SPL resist during all the lithographic steps. Despite this, and without the use of contact engineering (see the supplementary material for details), we find that the GFETs fabricated using t-SPL exhibit a relatively low specific contact resistance of 600 Ω·μm. This value is within the typical range of specific contact resistance (100 Ω·μm –800 Ω·μm) for monolayer graphene devices built using EBL, including those employing contact engineering.[4,8,25–28]

Our experiments began with the mechanical exfoliation of monolayer graphene from a bulk graphite crystal. Graphene monolayers were exfoliated onto a heavily doped silicon substrate covered with 285 nm of thermally grown SiO_2, which serves as the global back-gate in the final device structure. Monolayer graphene flakes were identified under an optical microscope and then verified using Raman spectroscopy. We then annealed the sample in an Ar/H_2 ambient at 500 °C for 1 h. This annealing step removes the residual tape contaminants on the substrate. The cleanliness of the oxide surface is important for spin-coating the substrate with a uniform resist layer for performing nano-patterning using t-SPL. As we describe below, we used a commercial t-SPL system for all nano-patterning steps in the device fabrication process.

The first step in our device fabrication process was to define and etch the active region within the monolayer graphene flake. Figure 1 shows the schematic illustration and optical images of this processing step. For t-SPL nano-patterning, we used a two-polymer stack resist, consisting of a 210 nm thick PMGI (polymethylglutarimide) layer and a 15 nm thick thermosensitive polymer film, namely, PPA (polyphthalaldehyde). These layers were deposited sequentially onto the substrate through spin coating [Figs. 1(a) and 1(f)]. We then performed t-SPL to define the active region of interest. During the nano-patterning process, a heated nano-probe (typically heated to 200 °C at the probe-resist contact) thermally decomposes and evaporates PPA. The precise movement of the probe transfers a computer-generated pattern into the PPA film [Fig. 1(b)]. The decomposed PPA quickly evaporates without being re-deposited onto the surface of the sample. The pattern was then chemically etched into the underlying PMGI using a diluted TMAH (tetramethylammonium hydroxide) solution, as shown in Figs. 1(c) and 1(g), which exposes the unwanted monolayer graphene regions for removal. We used a brief oxygen plasma treatment (see the experimental method) for removing the exposed graphene regions, resulting in a rectangular active device region [Figs. 1(e) and 1(h)]. The PPA/PMGI stack resist during the oxygen plasma etching process serves as a hard mask for protecting the underneath monolayer graphene in the active region. Hence, it must be sufficiently thick to survive the plasma etch process. However, patterning high-resolution features using t-SPL requires the use of a thin PPA film (see Fig. S1 of the supplementary material), suggesting that the PMGI film must be made thick enough to protect the active device region. In Fig. 1(i), we show how the thickness of PPA and PMGI changes due to exposure to the oxygen plasma. For this experiment, we produced two sample groups. Each sample group consisted of multiple substrates coated with either PPA or PMGI. The initial thickness of the film within each sample group was identical. However, each substrate within the group was subjected to a different etching time. Each data point in Fig. 1(i) represents one substrate. The data show that a thin PPA film (with ~12 nm initial thickness) withstood less than 15 s of exposure to oxygen plasma. In contrast, only 12 nm of the PMGI film was consumed after 25 s of etching under the same conditions, which is adequately long for etching monolayer graphene. This experiment explains the rationale for choosing the above-mentioned thicknesses for PMGI and PPA when patterning the active region of the graphene device. The resolution of the current pattern-etch transfer process is discussed in the supplementary material, where nanoscale etched graphene nano-ribbons are presented (Figs. S1 and S2).

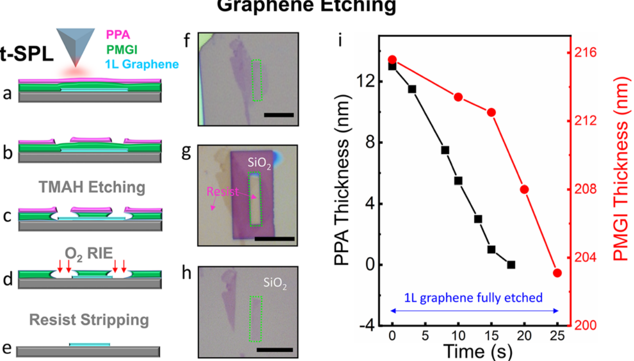

FIG. 1. Optimization of the t-SPL nano-patterning process for defining graphene regions. (a)–(e) Schematic illustration of the t-SPL process for patterning graphene active regions. (f) Optical microscope image of the starting graphene flake after coating with the PPA/PMGI resist. The green dotted box shows the target active region. (g) The same graphene flake after t-SPL patterning and chemical etching of the PMGI layer. (h) Final rectangular graphene ribbon obtained after 25 s oxygen plasma etching. The graphene ribbon has a length and width of 11.5 μm and 2.5 μm, respectively. Scale bars are 10 μm. (i) Etching rates of PPA and PMGI with oxygen plasma. Each data point represents one new substrate.

The second step in device fabrication after defining the active region on monolayer graphene was to pattern the metal electrodes. Figures 2(a)–2(e) show schematic illustrations of the fabrication steps. First, a two-polymer stack of PPA/PMGI (15 nm PPA/210 nm PMGI) was spin-coated on monolayer graphene. Then, we used a heated t-SPL nano-probe to pattern the metal electrode regions in the PPA film. Subsequently, the patterns were transferred into the underlying PMGI through chemical etching in diluted TMAH [see Figs. 2(b) and 2(c)], which also produces the required undercut. In this process, the top thin PPA ensures high-resolution patterning, while the underlying PMGI layer eases the metal lift-off process. Finally, we deposited a stack of Cr/Au (10 nm/20 nm) metals using electron-beam evaporation, followed by the metal lift-off. Figure 2(h) shows an example of the optical image of the final graphene device structure. To demonstrate the capability of t-SPL to fabricate graphene field-effect transistors (GFETs) at the nanoscale, we fabricated metal contacts on graphene with a minimum channel length of 60 nm [Fig. S2(c)]. It is noteworthy that such a small spacing between metal contacts results from the pattern amplification due to the development of PMGI and partial non-line-of-sight metal deposition. With proper optimization of pattern amplification, PPA/PMGI thickness, wet etching duration, RIE etch conditions, probe size, pattern depth, and eventually using a different process without PMGI, sub-10 nm graphene nanoribbons

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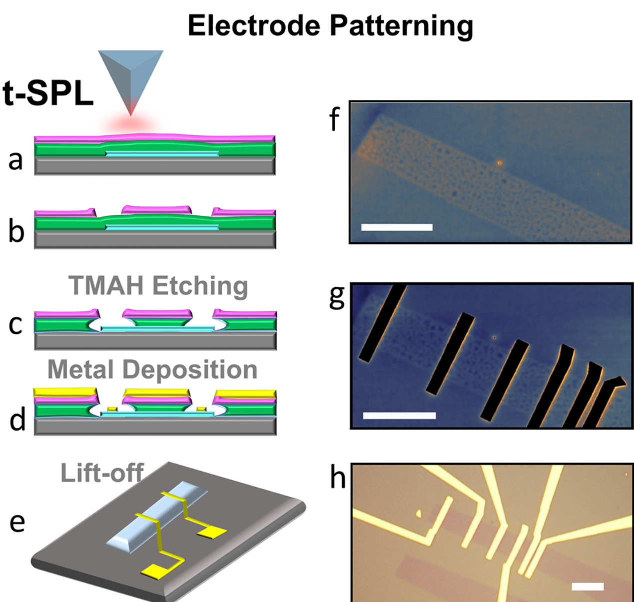

FIG. 2. t-SPL metal electrode patterning on graphene. (a)–(e) Schematic illustrations of the t-SPL patterning process for the fabrication of metal electrodes for GFETs. (f) *in situ* t-SPL imaging of monolayer graphene (rectangular ribbon with a length and width of 80 μm and 6.7 μm, respectively) after spin-coating the PPA/PMGI resist. (g) *in situ* t-SPL imaging of the structure, showing the patterned electrode features in the PPA layer. (h) Example of the optical image of a back-gated graphene device after lift-off. The spacings between electrodes are 0.6 μm, 2.3 μm, 4.3 μm, 6.1 μm, and 8.2 μm. Scale bars are 10 μm.

and channel lengths can be obtained using the process described in this work.

The t-SPL technique provides *in situ* simultaneous patterning and imaging, a capability that distinguishes t-SPL from other fabrication methods such as EBL or PL and provides important benefits, including the fact that there is no need for alignment marks.[29,30] Furthermore, the here-shown graphene devices have been fabricated in the ambient environment without the need for ultra-high vacuum (UHV). Indeed, before nano-patterning, a cold t-SPL probe produces a thermal image of the monolayer graphene active region underneath the resist to determine the target patterning location [Fig. 2(f)]. A second benefit of *in situ* imaging is the ability to inspect the quality of the patterned features simultaneously with t-SPL nano-patterning, allowing for a true closed feedback loop.[12] Figure 2(g) shows an *in situ* image of the patterned metal electrodes in the PPA layer.

Next, we studied the electronic properties of the t-SPL fabricated GFETs at room temperature. Figure 3(a) shows the total resistance, R_{tot}, of three graphene devices as a function of the applied back-gate bias, indicating the increase in the device resistance with the channel length. The total resistance in Fig. 3(a) was calculated by taking the ratio of the drain–source voltage (V_{ds}) to the current (I_d). These devices [marked as 1–3 in the inset optical image in Fig. 3(a)] have different channel lengths. Note that the shorter length devices were not connected, possibly due to cracks in their channel regions. The Dirac point voltage (V_{Dirac}) for channels 1, 2, and 3 in Fig. 3(a) are 1.2 V, −1.4 V, and −5.6 V, respectively (Fig. S3). These Dirac voltage shifts correspond to residual carrier densities of 9.1 × 10^{10} cm^{-2}, 10.6 × 10^{10} cm^{-2}, and 4.2 × 10^{11} cm^{-2}, which indicate the preservation of the intrinsic state of graphene after the t-SPL GEFT fabrication process.

To analyze the electronic properties of these devices, we first extracted the contact resistance using the transmission-line method (TLM). In particular, the total resistance is the sum of the intrinsic channel resistance and the contact resistance, given by

$$R_{tot} = 2R_c + \frac{\rho_{ch} \cdot L}{W}, \tag{1}$$

where R_c is the contact resistance due to one electrode, ρ_{ch} is the channel resistivity of monolayer graphene, and L and W are the channel length and width, respectively. In this equation, R_{tot} scales linearly with L, whereas the y-intercept is $2R_c$. Moreover, the slope gives information about the intrinsic resistivity of graphene, which depends on the carrier concentration (n) in the graphene channel. In Fig. 3(b), we plot the total resistance of devices 1, 2, and 3 at three different electron carrier densities, giving an estimated total contact resistance ($2R_c$) of 504 Ω, 403 Ω, and 355 Ω at n = 1.1 × 10^{12} cm^{-2}, 1.9 × 10^{12} cm^{-2}, and 2.6 × 10^{12} cm^{-2}, respectively. Note that we calculated the carrier density n using the following[31] equation:

$$V_g - V_{Dirac} = \frac{e}{C_{ox}} n + \frac{\hbar v_F k_F}{e}, \tag{2}$$

where C_{ox} is the oxide capacitance (1.2 × 10^{-8} F/cm^2), $\hbar$ is the reduced Planck constant, v_F is Fermi velocity of graphene (1 × 10^6 m/s), and $k_F = \sqrt{n\pi}$ is the Fermi wave vector. Figure 3(c) shows the extracted specific contact resistance, ρ_c, plotted against the carrier density for the range of the applied gate bias. The gray shading in this plot marks the region where uncertainty in the intercept of the linear fits to R_{tot} data is considerably large (>26% of the extracted R_c). This region corresponds to low carrier densities near the charge neutrality point (CNP). At high carrier densities, however, the error in estimated R_c is small, and ρ_c is as low as 600 Ω·μm in the electron branch. These values indicate that the here fabricated contacts to monolayer graphene are of good quality, considering that no supplementary contact engineering strategies were used. Table I compares ρ_c of our graphene devices fabricated by t-SPL in ambient conditions with some of the best results reported in literature for graphene FET fabricated by EBL in UHV and by photolithography with and without different supplementary contact engineering methods. We remark that similar methods of contact engineering can also be implemented together with the t-SPL process to achieve similar reductions of ρ_c (Table I in the supplementary material).

Finally, we calculated the carrier mobility in the as-fabricated monolayer graphene FET. To do so, we extracted the channel resistivity of device 1 from the slope of the linear regressions in Fig. 3(b) at different carrier densities. Figure 3(d) shows the plot of ρ_{ch} against the carrier density in graphene. The carrier mobility can be estimated by fitting the channel resistivity using $\rho_{ch} = (ne\mu_L + \sigma_0)^{-1} + \rho_s$,

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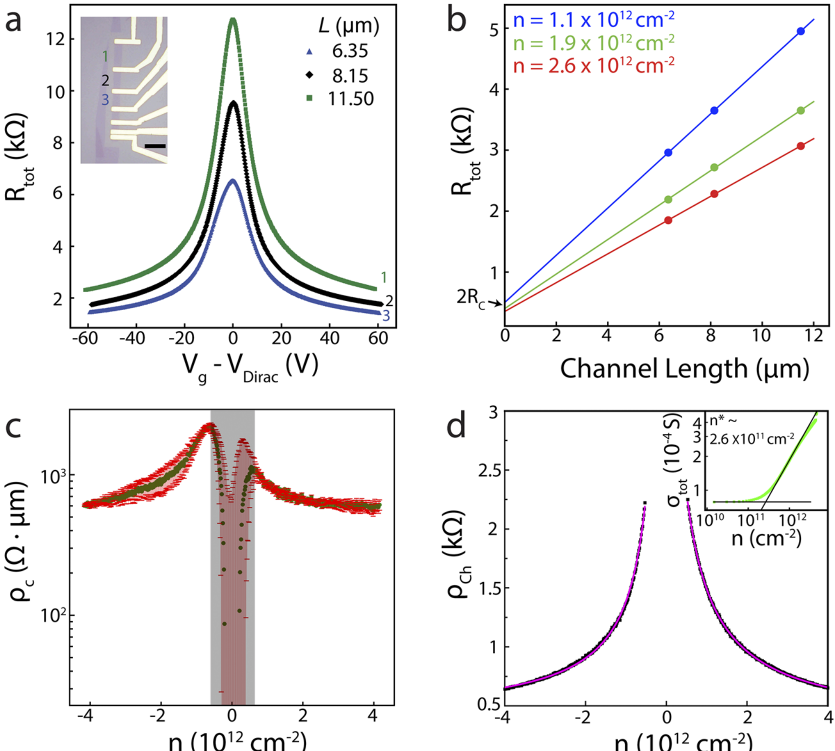

FIG. 3. Electrical characteristics of t-SPL fabricated devices. (a) Transfer characteristics of three GFETs in a TLM structure with the same channel width (3.5 μm) but different channel lengths. The contact width is 2.4 μm. The graphene ribbon has a full length of ~50 μm. The measurements were made at V_{ds} = 50 mV. (b) Plot of R_{tot} against the channel length for three different carrier densities for the GFETs in panel (a). The solid lines are linear fit to the data. The y-intercepts give $2R_c$. (c) Extracted specific contact resistance vs the carrier density. The green data points are the extracted ρ_c and the red bars represent the error. The extracted ρ_c values near CNP (the gray shading region) have considerable error. (d) Intrinsic channel resistivity plotted against the carrier density. The inset shows the double-logarithmic plot of conductivity vs carrier density, giving an estimated upper bound for the residual carrier density n^*. The black solid lines represent the extrapolated fits.

where μ_L represents the mobility due to long-range scattering, σ_0 is the minimum conductivity at CNP, and ρ_s indicates the contribution from short-range scattering.[32,33] Fitting the data in Fig. 3(d) (pink solid curve) yields $\mu_{L\text{-}Fit}$ of ~4500 cm^2/V s and ~6100 cm^2/V s for the electron branch and the hole branch, respectively. These carrier mobilities are within the range of previously reported values for graphene on SiO_2, which is between 2000 cm^2/V s and 20 000 cm^2/V s.[34–37]

We also employed the theoretical graphene transport study by Adam *et al.*[43] for evaluating the expected carrier mobility in the diffusive limit from the impurity concentration (n_{imp}) at the graphene–oxide interface. In particular, the transport mobility

TABLE I. Summary of state-of-art specific contact resistance ρ_c obtained by different fabrication methods.

Graphene	Lithography	Contact material	Contact engineering	Specific contact resistance (Ω·μm)	Carrier density (10^{12} cm^{-2})	Gate structure	References
CVD	PL	Ti/Au	UV ozone cleaning	200	...	Global back-gate	38
CVD	PL	Cr/Au	CO_2 cleaning	270	...	Global back-gate	39
			None	960	...		
CVD	EBL	Pd/Au	None	654	3	Global back-gate	40
			MoO_3 doping	200	70		
CVD	EBL	Pd/Au	High-purity Pd and high-vacuum deposition	100	3.75	Global back-gate	25
Exfoliated	EBL	Cr/Pd/Au	Edge contact	150	3	Global back-gate	41
CVD	EBL	Au	Holey contact	45	20	Global back-gate	27
			None	519	20		
Exfoliated	EBL	Ni	Ni-etched contact	100	...	Global back-gate	28
			None	630			
CVD	EBL	Ti/Pd/Au	Double contact	260	4.75	Global back-gate	42
Exfoliated	t-SPL	Cr/Au	None	600	3	Global back-gate	This work

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follows $\mu = 20e/(hn_{imp})$, where n_{imp} can be estimated from the residual carrier density (n^*) using $n^* \cong 0.3n_{imp}$. The plot in the inset of Fig. 3(d) shows the double-logarithmic plot of the conductivity vs carrier density, which gives an upper bound estimate of $n^* = 2.6 \times 10^{11}$ cm^{-2} from the σ plateau. Using this information, we calculate carrier mobility of ~5500 cm^2/V s. The obtained mobility from the analytical solution is comparable with the fitting results, providing further confidence in the extracted specific contact resistance in Fig. 3(c).

In summary, we demonstrated the application of t-SPL for fabricating GFETs. We showed that it is possible to combine t-SPL with plasma etching for producing graphene structures of desired shapes. More importantly, the t-SPL fabricated metal electrodes resulted in low-resistance contacts on monolayer graphene without contact engineering. Further improvements of the contact resistance require an in-depth study to identify the factors that limit the contact resistance in the t-SPL process. t-SPL is very attractive compared to EBL because it offers *in situ* simultaneous imaging and patterning capabilities and it operates in ambient conditions, which is a considerable advantage for achieving a cost-effective nano-patterning process. The results presented here establish the prospects of t-SPL for the fabrication of graphene devices.

See the supplementary material for the following analyses and/or descriptions: the high resolution t-SPL pattern in the PPA resist, nanoscale etch-pattern transfer and metal deposition using the t-SPL process, unshifted transfer characteristics of GFET in Fig. 3(a), and the literature review of contact engineering of metal-graphene contacts.

AUTHORS' CONTRIBUTIONS

X.L. and Z.H. contributed equally to this work.

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APPENDIX: EXPERIMENTAL

1. Graphene sample preparation

Graphene layers were identified under an optical microscope and confirmed by Raman spectroscopy. Graphene flakes were exfoliated on 285 nm SiO_2 on Si substrates from bulk graphite crystals (NGS Naturgraphit) using a Scotch tape. Monolayer graphene flakes were identified under an optical microscope and confirmed by Raman spectroscopy.

2. Defining graphene active region

Graphene samples were spin-coated with PMGI (polymethylglutarimide, Microchem) (2000 rpm for 35 s) followed by baking at 200 °C for 1 min. This step was repeated three times resulting in a film of 215 nm. Then, a PPA (polyphthalaldehyde, Sigma Aldrich) solution (0.9 wt. % in anisole) is spin-coated on PMGI (2000 rpm for 4 s and then 3000 rpm for 35 s) followed by baking at 90 °C for 3 min. This gives rise to a PPA/PMGI (15 nm/215 nm) polymer stack. The graphene active region was patterned on the PPA resist using a commercial t-SPL system, Nanofrazor (Heidelberg Instruments). After the t-SPL patterning, samples were immersed in a solution of TMAH in deionized water (tetramethylammonium hydroxide AZ726 MIF, MicroChemicals) (0.17 mol/L) for 400 s to chemically etch the exposed PMGI in the patterned region, then rinsed with deionized water (30 s) and IPrOH (30 s), and finally dried with N_2. Then, samples were etched with a mild O_2 reactive ion etching for 25 s (20 W, 100 mTorr; Oxford Instruments PlasmaPro NPG80 RIE) and transferred into the Remover PG (MicroChem) for a few hours to strip off the polymer resist, followed by rinsing (IPrOH) and drying (N_2).

3. Fabrication of GFETs by t-SPL

PMGI and PPA were spin-coated with the same conditions as described for defining the graphene active region. The patterns of electrical contacts were generated by t-SPL in the PPA resist over the previously defined graphene active region. The same chemical etching by TMAH was also performed to expose the graphene in the contact regions, which generates an undercut profile to facilitate the metal lift-off. Metal deposition is performed using an AJA Orion 8E e-beam evaporator (deposition rate: 1 Å s^{-1} and pressure ~10^{-8} Torr). Finally, samples were dipped in the Remover PG (MicroChem) for a few hours to lift off the metal and resist, followed by rinsing (IPrOH) and drying (N_2). The metal electrodes of back-gated t-SPL GFETs presented in this paper have been fabricated using Cr/Au (10 nm/20 nm).

4. Electrical measurements

The electrical measurements of the TLM-structured GFETs were made inside a Lakeshore probe station at a pressure of 10^{-5} Torr and using a Keithley 4200-SCS parameter analyzer.

5. AFM measurements

All the thicknesses of polymer resists and metals were measured by AFM (Bruker Multimode 8) operating in the tapping mode.

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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