



How to report and benchmark emerging field-effect transistors

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The use of organic, oxide and low-dimensional materials in field-effect transistors has now been studied for decades. However, properly reporting and comparing device performance remains challenging due to the interdependency of multiple device parameters. The interdisciplinarity of this research community has also led to a lack of consistent reporting and benchmarking guidelines. Here we propose guidelines for reporting and benchmarking key field-effect transistor parameters and performance metrics. We provide an example of this reporting and benchmarking process using a two-dimensional semiconductor field-effect transistor. Our guidelines should help promote an improved approach for assessing device performance in emerging field-effect transistors, helping the field to progress in a more consistent and meaningful way.

Research into field-effect transistors (FETs) based on emerging nanomaterials—including carbon nanotubes^{1,2}, graphene³, phosphorene⁴, silicene⁵, tellurene⁶, transition metal dichalcogenides^{7–9}, organic semiconductors^{10,11} and ultrathin metal oxides¹²—is thriving. Such studies allow the fundamental properties of the materials to be explored, and may lead to the development of various commercial applications. However, effectively and uniformly assessing the performance of emergent FETs is difficult due to the dependence of performance metrics on unique aspects of the device structure (Fig. 1a)¹³.

The structural parameters that influence device performance include channel length (L_{ch}) and contact length (L_{c}), gate insulator thickness (t_{ins}) and permittivity (ϵ_{ins}), contact metal types, the thickness of the channel material (t_{ch}) and the gating scheme (for example, top, bottom, gate-all-around, multi-channel). Performance metrics include on current (I_{on}), off current (I_{off}), the $I_{\text{on}}/I_{\text{off}}$ ratio, contact resistance (R_{c}), transconductance (g_{m}), subthreshold swing (SS), channel mobilities and drain-induced barrier lowering (DIBL). Although the different studies reported in the literature often include some of these benchmarking figures, they struggle to capture the myriad variables, making comparisons inaccurate or even biased at times. In addition, the emerging device community consists of researchers from disparate disciplines—including electrical engineering, chemistry, materials science and physics—which also makes consistent reporting and benchmarking challenging. In this Perspective we examine the challenges involved in assessing the operation and performance of FETs based on emerging materials, and provide guidelines on how to report and benchmark the devices.

Field-effect transistor structure and key parameters

In a FET, the structural parameters determine the electric fields and the eventual device performance (Fig. 1a). The subthreshold, transfer and output characteristics presented in Fig. 1b–d are the most common I – V (current–voltage) curves to capture device performance. Plotting the log of the drain current (I_{D}) as a function of gate–source voltage (V_{GS}) highlights the subthreshold (that is, off state) device behaviour. In contrast, transfer characteristics plot I_{D} versus V_{GS} on a linear scale and emphasize the device behaviour after V_{GS} exceeds the threshold voltage (V_{T}), where the device is in the on state. Ideally, the gate leakage current (I_{G}) versus V_{GS} should be plotted on the subthreshold plot as well.

The $I_{\text{D}}-V_{\text{GS}}$ sweeps in Fig. 1b,c should be conducted at both ‘small’ and ‘high’ drain–source voltage (V_{DS}) values to characterize device operation in both the linear and saturation regimes. We note that the small V_{DS} value should be sufficiently small to ensure linear-regime operation, but greater than $\sim 2k_{\text{B}}T$ (where k_{B} is the Boltzmann constant and T is the absolute temperature, that is, ~ 50 mV at room temperature) to ensure that the subthreshold behaviour (here, in particular, DIBL, $\partial V_{\text{T}}/\partial V_{\text{DS}}$) is not misinterpreted due to thermal injection of carriers from the drain. These curves enable easy extraction of DIBL to demonstrate how V_{DS} impacts V_{T} . The transfer characteristics should be acquired with forwards and backwards sweeps, checking for the presence of any hysteresis due to charge trapping¹⁴. When comparing the hysteresis from different devices, precise measurement conditions such as sweep rates, hold times and maximum bias voltages should be listed, as these parameters influence hysteresis. If hysteresis exists, it

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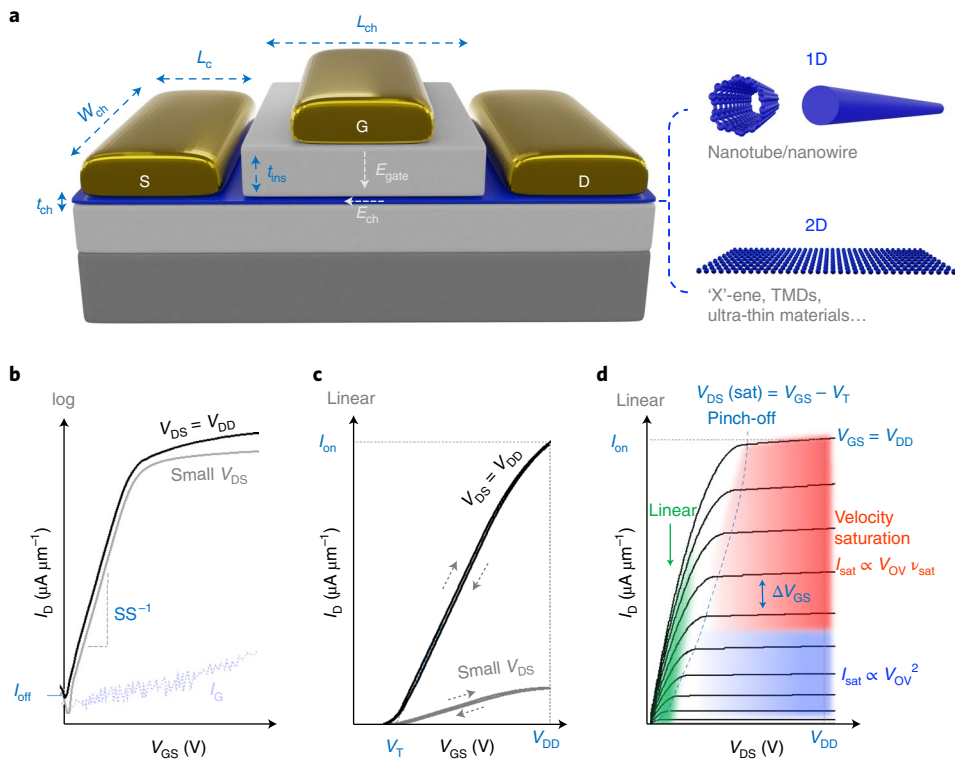


Fig. 1 | Basic device structure and electrical characteristics. **a**, Diagram of a typical nanomaterial-based n-type FET, highlighting the structure parameters and electric fields. TMD, transition metal dichalcogenide; W_{ch} , channel width; L_{ch} , channel length; L_c , contact length; t_{ch} , channel material thickness; t_{ins} , gate insulator thickness; E_{gate} , vertical electric field at the source end; E_{ch} , the channel electric field between source and drain. **b, c**, Subthreshold (**b**) and transfer (**c**) (I_D - V_{GS}) curves of an n-type FET under different V_{DS} voltages. Representative curves are shown for a single sweep in **b**, but forwards and backwards sweeps of V_{GS} should be collected to determine hysteresis, as shown in **c**. The gate leakage current is also shown in **b**. **d**, Output (I_D - V_{DS}) curves of the device, with the three main operation regimes labelled¹⁶. V_{GS} is swept from low to high in steps of ΔV_{GS} . v_{sat} is the saturation velocity of carriers in the channel material. I_{sat} scales as V_{OV}^2 in the classical pinch-off regime, but only linearly with V_{OV} when the velocity saturates. Self-heating could render this increase even sublinear^{16,54}. Note that V_{DD} is the supply voltage for the transistor (that is, the target maximum voltage of operation for both V_{DS} and V_{GS}).

should be accounted for in the analysis of V_{T} uncertainty and other device parameters that depend on V_{T} .

In the output characteristics (Fig. 1d), three main operation regimes are highlighted. The linear regime is characterized by the linear increase of I_{D} with both V_{DS} and V_{GS} . After V_{DS} surpasses the overdrive voltage ($V_{\text{OV}} = V_{\text{GS}} - V_{\text{T}}$ for n-channel FETs), I_{D} starts to saturate to I_{sat} , which could (based on the classical FET model¹⁵) increase quadratically with V_{OV} in the pinch-off regime and linearly with V_{OV} in the velocity saturation regime¹⁶. Note that the linear regime may present as nonlinear (often exponential) in the event of poor carrier injection at the contacts, such as from large Schottky barriers.

Multiple performance parameters can be extracted from the I - V curves in Fig. 1b-d. The most important performance metrics are the currents, which must be reported normalized by the channel width, W_{ch} (for example, in units of $\mu\text{A } \mu\text{m}^{-1}$). For one-dimensional (1D) or quasi-1D devices, it is common to first report the current per carbon nanotube (CNT)/nanowire/nanosheet stack. The current can then be normalized to units of $\mu\text{A } \mu\text{m}^{-1}$ by considering the expected channel density and pitch of the channel material (for example, 10 μA per CNT with 50 CNTs μm^{-1} , giving 500 $\mu\text{A } \mu\text{m}^{-1}$), because the aerial footprint of the device is a critical aspect of performance. When extracting I_{on} and I_{off} from these I - V curves, in a simplified scenario, I_{off} is the I_{D} measured at $V_{\text{GS}} = 0$ and $V_{\text{DS}} = V_{\text{DD}}$, whereas I_{on} is the I_{D} measured at $V_{\text{GS}} = V_{\text{DS}} = V_{\text{DD}}$. Here, V_{DD} is the voltage that would be supplied to operate the transistors. (For mainstream silicon technology, V_{DD} dropped to 1 V near 2010 and to 0.7 V in recent years¹⁷.) For modern technologies, the exact value of V_{DD}

depends on the application. For example, if the emergent transistor is used as an access transistor in a dynamic random-access memory (DRAM), then its V_{DD} will be a small value to ensure linear-regime operation in the on state. Reported emergent devices often do not have threshold voltages tuned such that $V_{\text{GS}} = 0$ is a sensible off state; additionally, there is often not a well-defined V_{DD} value due to the wide variety of device structural parameters. We hence suggest extracting the maximum and minimum I_{D} (I_{max} and I_{min}) from a typical subthreshold curve and reporting the $I_{\text{max}}/I_{\text{min}}$ ratios when V_{DS} is biased in both the linear and saturation regimes. A more detailed description on reporting and benchmarking $I_{\text{max}}/I_{\text{min}}$ is provided in Supplementary Note 1.

When reporting the I_{sat} of a device, it is necessary to note the carrier density n at which the I_{sat} is extracted. Ideally, the Hall effect is used to measure the carrier density for the channel material, but for most researchers in the FET community, more accessible approaches are needed that do not require specially designed test structures. In the linear regime, the average carrier density can be estimated as $n \approx C_{\text{ins}} (V_{\text{OV}} - V_{\text{DS}}/2)/q$, where C_{ins} is the gate insulator capacitance and q is the elementary charge; however, in the saturation regime, the depletion region in the channel complicates the estimation. The carrier density near the source side is the same for both the linear and saturation regimes. For convenience and simplicity, we recommend clearly labelling the carrier density near the source as $n_{\text{s}} (= C_{\text{ins}} V_{\text{OV}}/q)$ and using this value for both operation regimes. To determine V_{OV} , V_{T} is usually estimated using extrapolation in the linear portion of the transfer curve, as listed in Table 1. Other methods, such as constant-current¹⁸, Y-function

Table 1 | Checklist of suggested device parameters to report

Name	Characteristics	Additional details
Structural parameters	Contact length, L_c Channel length, L_{ch} Channel width, W_{ch} Insulator thickness, t_{ins} Channel thickness, t_{ch}	Specify contact and gating geometry/materials; include high-resolution electron microscopy evidence when reporting sub-20-nm dimensions (especially for L_c and L_{ch})
Insulator capacitance, C_{ins}	Capacitance–voltage or capacitance–frequency	Measured C_{ins} is more accurate than estimating ϵ_{ins} especially when a high- k insulator is used
Threshold voltage, V_T , and hysteresis, ΔV_T	Extrapolation in the linear portion of the transfer curve ¹⁸	<ul style="list-style-type: none"> I_D-V_{GS} should have forwards and backwards sweeps Consider V_T uncertainty due to hysteresis (charge trapping), the dependence of V_{DS} and I-V sweeps (Supplementary Note 2)
Drain current in saturation regime, I_{sat}	I_D - V_{DS} (saturation regime)	<ul style="list-style-type: none"> Sweep I_D-V_{DS} to the saturation regime Specify carrier density where I_{sat} is extracted Normalized by channel width
Contact resistance, R_c	Transfer length method (TLM) ²² (Supplementary Note 3)	<ul style="list-style-type: none"> Linear regime (small V_{DS}) Specify carrier density n_s or plot R_c versus n_s TLM should have at least four channels and include at least one each of contact and channel resistance-dominated devices
Conductivity mobility, μ_{con}	$\frac{1}{qn_s R_{sh}}$	<ul style="list-style-type: none"> R_{sh} is extracted from the slope of TLM plots or from four-probe measurements²¹ (units: $\Omega \square^{-1}$) Carrier density near the source: $n_s \approx C_{ins} V_{OV} / q$ Mobility from $R_{sh} = (qn_s \mu)^{-1}$ Plot mobility versus n_s to show field dependence
Transconductance, g_m	Transfer or output curves $g_m = \frac{\partial I_D}{\partial V_{GS}}$ at certain V_{DS}	Specify g_m (linear) or g_m (saturation)
Subthreshold swing (SS)	Subthreshold curves (inverse slope in mV dec ⁻¹ below V_T)	<ul style="list-style-type: none"> SS depends on C_{ins} and interface trap capacitance C_{it} Plot SS versus $\log_{10}(I_D)$
I_{on}/I_{off}	Subthreshold curves at saturation regime, $V_{DS} = V_{DS}(sat)$	<ul style="list-style-type: none"> Report I_{max}/I_{min} as an alternative along with the n_s range Plot I_G versus V_{GS} to show leakage current
DIBL	$\Delta V_T / \Delta V_{DS}$ from transfer curves	Key for short-channel devices

methods^{19,20} and four-probe measurements²¹, can be used to cross-check the linear extraction of V_T and reduce the variation when estimating n_s . More discussion regarding V_T extraction is given in Supplementary Note 2.

In addition to I_D , R_c is also essential to represent device performance. The transfer length method (TLM) is the most commonly used approach for extracting R_c , along with the sheet resistance, R_{sh} , of the channel (in units of $\Omega \square^{-1}$)²². The TLM approach requires a series of FETs with different channel lengths and consistent contact and gating configurations. It entails plotting the total resistance of each device versus L_{ch} at a given n_s , allowing R_c to be extracted as the extrapolated y -axis intercept from a linear fit to the data points. Typically, the V_{DS} for calculating the total resistance is the small V_{DS} used in Fig. 1b to ensure linear-regime operation. The channel lengths in the TLM should range from short (where the total resistance is dominated by R_c) to long (dominated by channel resistance $R_{ch} = R_{tot} - 2R_c$ or $R_{sh}L_{ch}$) where the actual short and long channel lengths will depend on the relationship between the channel resistance and the contact resistance. A more detailed discussion on extracting R_c and other considerations using TLM data is provided in Supplementary Note 3.

Another frequently reported parameter is the carrier mobility of the channel material. Among various forms of mobility, the field-effect mobility $\mu_{FE} = L_{ch} g_m / (W_{ch} C_{ins} V_{DS})$ is often used. However, μ_{FE} can be underestimated^{20,23} or overestimated^{21,24,25} relative to the drift mobility of the channel material depending on the details of V_{DS} , V_{GS} , R_c , L_{ch} , and gate capacitance. In particular, gated contact effects can significantly affect mobility extraction. Although different approaches^{20,22} have been proposed to make μ_{FE} less dependent on various factors, such as R_c and L_{ch} , none of them is sufficiently

general enough to be widely adopted. Conductivity mobility (μ_{con}) has the advantage of strictly reflecting the channel material properties and the quality of the channel–dielectric interface^{22,26}. In a FET, μ_{con} (ref. 22) can be estimated from the sheet resistance of the semiconductor channel and the carrier density, n_s (Table 1); thus, it does not involve the contact resistance or the device structure. High mobility is often a goal for research FETs; when such reports are made, it is critical to clearly state how the values are determined, and ideally multiple approaches (such as μ_{FE} and four-probe measurements²¹) are taken to cross-validate the claims. It is worth noting that the usefulness of channel mobility as an indicator of performance in aggressively scaled FETs is debatable, as devices with channel lengths <30 nm are going to be strongly limited by contact resistance (including carrier injection efficiency), with minimal dependence on transport in the channel^{27,28}.

The most representative FET parameters are listed in Table 1 as a suggested reporting checklist. Additional parameters are briefly discussed in Supplementary Note 4.

Beyond the parameters in Table 1, showing statistics and variation is strongly encouraged to obtain comprehensive coverage of the device performance. The variation can be shown as error bars, box plots, coefficient of variation or cumulative distribution function (see Supplementary Note 5 for a demonstration). Due to the many non-idealities associated with emerging materials or unconventional device geometries, it is almost unavoidable that there could be considerable uncertainties in many extracted parameters, including R_c , n_s and mobilities. These parameters are often interdependent. Reducing device variation is a major research theme for the eventual application of emergent FETs. Whatever measurements and specific analysis approaches are taken to determine these

Table 2 | Suggested benchmarking plots for evaluating device performance compared with other FETs

Parameter	Benchmarking plot	Notes
I_{\min} and I_{\max}	I_{\min} versus I_{\max}	<ul style="list-style-type: none"> Specify L_{ch} or L_{ch}/EOT Ideally specify the carrier density at which I_{\max} is extracted (Supplementary Note 1)
I_{sat}	I_{sat} versus n_s	Label L_{ch} and t_{ch} to imply channel resistance
I_D	I_D versus L_{ch}	At certain V_{DS} and n_s (for example, $V_{\text{DS}} = 1\text{ V}$ and $n_s = 10^{13}\text{ cm}^{-2}$)
R_c	R_c versus n_s	<ul style="list-style-type: none"> Or benchmark R_c versus t_{ch} at certain n_s Specify if semiconductor in contact regions is gated or not
μ_{con}	μ_{con} versus t_{ch}	For the same material, a thicker channel could have higher mobility due to less surface scattering
g_m	g_m versus n_s/L_{ch}	<ul style="list-style-type: none"> Because $g_m = \frac{W}{L} \mu C_{\text{ins}} V_{\text{OV}}$, $g_m \propto C_{\text{ins}} V_{\text{OV}}/L_{\text{ch}}$ $n_s \approx C_{\text{ins}} V_{\text{OV}}/q$ near the source end, so $g_m \propto n_s/L_{\text{ch}}$
SS	SS versus C_{ins}	<ul style="list-style-type: none"> Larger C_{ins} can yield smaller SS Identify Schottky barrier branch and thermal branch Or plot SS versus L_{ch} to show short-channel robustness Or plot SS versus $\log_{10}(I_D)$

parameters, the details should be clearly and explicitly reported, and our recommended approaches are demonstrated herein.

Once an emerging FET has been systematically parameterized, benchmarking tables and plots are extremely useful for comparing devices from different reports. Because the electric fields are the driving forces within FETs, benchmarking performance metrics based on electric fields is natural. However, special care is needed in considering electric fields in devices, because they are spatially non-uniform and depend on many other factors, such as fringing fields and quantum capacitance C_q . Thus, the electric fields in nanoscale FETs are more complicated than the simple definition of an applied voltage divided by a physically defined length. For example, it is a reasonable assumption that the channel electric field (E_{ch}) increases linearly from source to drain in the linear region of operation, but E_{ch} peaks sharply at the drain end of the channel in classical pinch-off (saturation)²⁹. To account for this, the average E_{ch} can be approximated as $(V_{\text{DS}} - 2I_{\text{lin}}R_c)/L_{\text{ch}}$ in the linear regime, accounting for voltage dropped at the contacts.

The vertical electric field at the source end, E_{gate} , can be estimated as $V_{\text{OV}}/t_{\text{ins}}$ if a planar gate is used. In turn, E_{gate} and the gate insulator permittivity determine the carrier density in the channel. However, both E_{gate} and the gate insulator permittivity are rather challenging to measure accurately. One more word of caution is justified: because many low-dimensional materials exhibit a low density of states, C_{ins} needs to be replaced by $C_{\text{ins}}C_q/(C_{\text{ins}} + C_q)$, where quantum capacitance (C_q) can be approximated as $q^2\text{DOS}$ (density of states)^{30,31}. Only for $C_{\text{ins}} \ll C_q$ does this expression become equivalent to C_{ins} . Because multiple parameters in Table 1 depend on n_s , benchmarking these versus n_s is recommended to evaluate devices from different studies. A suggested list of benchmarking plots to evaluate device parameters and performance metrics is provided in Table 2.

Drain current is the key output of a FET and is also frequently benchmarked and compared. However, many comparisons are oversimplified and not fairly conducted as the drain current depends on many parameters. As mentioned in Table 2, we recommend benchmarking I_D versus L_{ch} at certain V_{DS} and n_s values, enabling fair comparison between devices having different channel lengths. On the other hand, if a record I_{sat} is claimed, we recommend benchmarking the maximum I_{sat} versus n_s , because it is a much closer indicator for the eventual drive current and ultimately sets the operating delay of a circuit stage (delay $\tau \propto CV_{\text{DD}}/I_{\text{sat}}$). As mentioned previously, assuming limited short-channel effects, I_{sat} mainly depends on n_s and not on E_{ch} . Usually, one performance metric depends on multiple parameters; hence, key parameters should be annotated on the benchmarking plot (Table 2).

Reporting and benchmarking example

To demonstrate reporting and benchmarking based on the principles proposed above, MoS₂ is chosen as the example emerging channel material because it is among the most studied semiconducting nanomaterials in recent years and represents a family of 2D materials that holds promise for future transistor applications. Figure 2a shows an example transistor based on monolayer (1 L) MoS₂ grown by chemical vapour deposition. The device is top-contacted and back-gated, which is the most common and convenient FET structure used to explore emergent channel materials. The approach is as follows:

Step 1. The structural parameters of the device are determined and labelled (Fig. 2a). In this example, the gate insulator is AlO_x, which is grown by atomic layer deposition with the oxide capacitance ($C_{\text{ins}} \approx 280\text{ nF cm}^{-2}$) evaluated from a capacitance–voltage measurement of a large-area test capacitor. The thickness of the oxide ($t_{\text{ins}} \approx 20\text{ nm}$) is further confirmed by cross-sectional transmission electron microscope (TEM) imaging. From the thickness and capacitance, the dielectric constant of the oxide is estimated to be $\epsilon_{\text{ins}} \approx 6$. Other dimensions, such as L_{ch} , W_{ch} and L_c , are confirmed by scanning electron microscopy (SEM) after electrical characterization.

Step 2. I_D – V_{GS} and I_D – V_{DS} characterizations are performed, making sure that V_{DS} and V_{GS} are swept high enough for the device to reach saturation, and the V_{GS} sweep range is sufficient to observe I_{\min} in both the linear (low V_{DS}) and saturation (high V_{DS}) operation regions. An I_{\max}/I_{\min} value of $\sim 4 \times 10^7$ at $V_{\text{DS}} = 4\text{ V}$ can be extracted from the subthreshold curve in Fig. 2b. I_{\max} is extracted at $n_s \approx 1.4 \times 10^{13}\text{ cm}^{-2}$. I_{\min} is extracted under subthreshold conditions, where $V_{\text{GS}} < V_{\text{T}}$ yielding a negative V_{OV} and $n_s \approx 0$. The larger hysteresis for $V_{\text{DS}} = 4\text{ V}$ in Fig. 2b,c highlights the impact of the larger source–drain field on the interface charges in the channel. Due to hot-carrier stress from the high V_{DS} (explained later), V_{T} increases for high V_{DS} , resulting in an extracted DIBL of -274 to -436 mV V^{-1} , considering the effect of hysteresis. Also, from the transfer curves in Fig. 2c, the maximum $g_m(\text{sat})$ and $g_m(\text{lin})$ are estimated to be $\sim 59\text{ }\mu\text{S }\mu\text{m}^{-1}$ and $\sim 1.7\text{ }\mu\text{S }\mu\text{m}^{-1}$, respectively. In Fig. 2d, approximate current saturation is observed, with I_{sat} around $325\text{ }\mu\text{A }\mu\text{m}^{-1}$ obtained at $n_s \approx 1.3 \times 10^{13}\text{ cm}^{-2}$ at $V_{\text{DS}} = 4\text{ V}$. The blue and red points show the linear and saturation regions, approximately. The I_D – V_{DS} spacing is sublinear at the highest V_{GS} , which is a sign of possible self-heating.

Figure 2a–d is used for primary characterization of one device, and more derived plots are shown in Fig. 2e–h, providing a more complete picture of the device characteristics. The device spread and parameter variations based on ten similar TLM structures are shown in Supplementary Fig. 5. The full range of SS versus I_D is plotted in Fig. 2d, with a minimum SS of 280 mV dec^{-1} extracted in the subthreshold regime. Additionally, because V_{T} depends on V_{DS} , it is key to extract V_{T} at the associated V_{DS} (as noted in Table 1). R_c , R_{sh} and subsequently μ_{con} are extracted by using a TLM

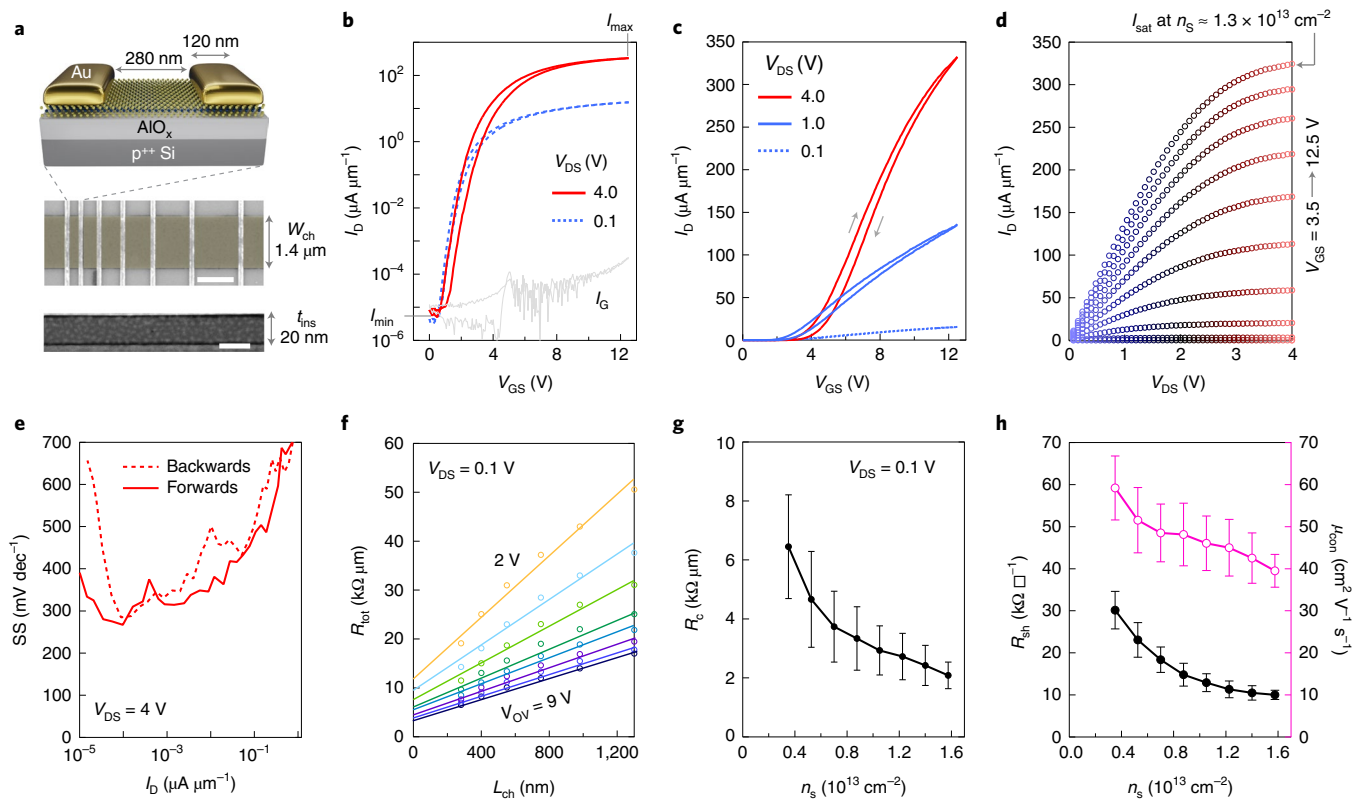


Fig. 2 | Example of reporting device performance for monolayer Au-contacted MoS₂ FETs. **a**, Device schematic and the basic structural parameters of the MoS₂ FET, a SEM image of a TLM structure with false-coloured MoS₂ area (scale bar, 1 μm) and a cross-sectional TEM image of the AlO_x (scale bar, 20 nm). **b**, Subthreshold (I_D - V_{GS}) curve of the device, with I_{max} and I_{min} labelled. I_G is the gate leakage current at $V_{DS} = 4$ V. The curve for $V_{DS} = 1$ V is intentionally not shown so the plot is less crowded. **c**, Transfer (I_D - V_{GS}) curves of the device, showing larger hysteresis with larger V_{DS} . **d**, Output (I_D - V_{DS}) curves of the device. V_{GS} changes in steps of 1 V. **e**, SS versus I_D for both forwards and backwards V_{GS} sweeps in **b**. **f**, Extraction of R_c from the TLM structure in **a**. R_{tot} is extracted at $V_{DS} = 100$ mV. **g**, Contact resistance versus n_s , showing the contact gating effect that is a result of the device operating as a Schottky barrier transistor with the gate modulating the semiconductor in the source-drain contact regions³². **h**, Extracted sheet resistance (left axis) and conductivity mobility (right axis) versus n_s . In **g** and **h**, error bars reflect the 90% confidence interval from a least-squares fit of the TLM.

structure as shown in Fig. 2f–h. The R_c is estimated to be ~ 2.1 kΩ μm, which is comparable to the R_{ch} of 2.8 kΩ μm for the device with channel length of 280 nm. The relation between n_s and extracted R_c is plotted in Fig. 2g to show the effect of the overall back-gate on the contact resistance (that is, contact gating^{32–34}). Figure 2h shows that μ_{con} decreases from 59 to 40 cm² V⁻¹ s⁻¹ with increasing n_s , probably due to the increased electron scattering with the oxide surface roughness.

Step 3. As a simplified example, we benchmark key device performance parameters in Fig. 3 (a limited number of reports are included). Currently, most papers do not report I_D - V_{GS} at V_{DS} (sat) or close to V_{DD} , as recommended above. Hence, plotting I_{min} versus I_{max} at certain V_{DS} (for example, $V_{DS} = 1$ V) while annotating L_{ch} is an acceptable approach (Fig. 3a). The upper limit of the carrier density is set at $n_s = 10^{13}$ cm⁻², ensuring a fair comparison of I_{max} . The I_{max}/I_{min} ratio annotated on the right axis is also shown in the dashed lines in Fig. 3a. Owing to better electrostatic control from the gate, devices with a larger L_{ch}/EOT ratio tend to yield higher I_{max}/I_{min} (where EOT is the equivalent oxide thickness). Other parameters also play a role, such as the leakage currents through the gate insulator or from source to drain. Large channel width can also produce a more accurate width-normalized I_{min} , especially when I_{min} is below the instrument noise floor. For example, a relatively high I_{max}/I_{min} ratio has been demonstrated in ref. 35 in devices with 20-μm channel width. Further study is still needed to investigate how to achieve high I_{max} and small I_{min} in aggressively scaled devices (small L_{ch} , L_c and EOT).

As mentioned previously, a high drain current in the saturation regime is a key performance metric. In Fig. 3b, I_{sat} is plotted versus n_s from representative studies of FETs based on MoS₂ as the channel material. We note that I_{sat} is extracted at different V_{DS} values, because different devices have different channel lengths, as annotated in Fig. 3b. We caution against plotting I_{sat}/L_{ch} versus n_s , because it implies that L_{ch} is the main limiting factor for I_{sat} , which is not necessarily true, especially for scaled devices where contact resistance typically dominates I_{sat} performance. Importantly, it is clear that I_{sat} needs to be further improved to meet the high-performance target of the most recent technology guidelines (at $V_{DD} \approx 0.65$ V near 2030)³⁶. Many reports have already used high n_s but fell short regarding I_{sat} , even with channel lengths down to ~ 10 nm (ref. 37), being strongly limited by their contacts.

Recently, semimetal contacts such as bismuth have been shown to produce high-quality contacts³⁸. It is nevertheless noteworthy that the two Bi-1L MoS₂ devices have a wide range of I_{sat} performance, encompassing all the other devices in Fig. 3b, yet the channel length difference between the two devices is only 115 nm. Interestingly, one of the Bi-contacted devices ($L_{ch} = 150$ nm) actually underperforms other Au-contacted devices with longer channel lengths. Hence, although some approaches show potential to achieve the International Roadmap for Devices and Systems (IRDS) high-performance goal of I_{sat} for the post-2030 era³⁶, further investigation is still needed to reliably and reproducibly realize high I_{sat} from a monolayer channel. In next-generation FETs, I_{sat} could also be increased by shifting to nanosheet device designs, which stack

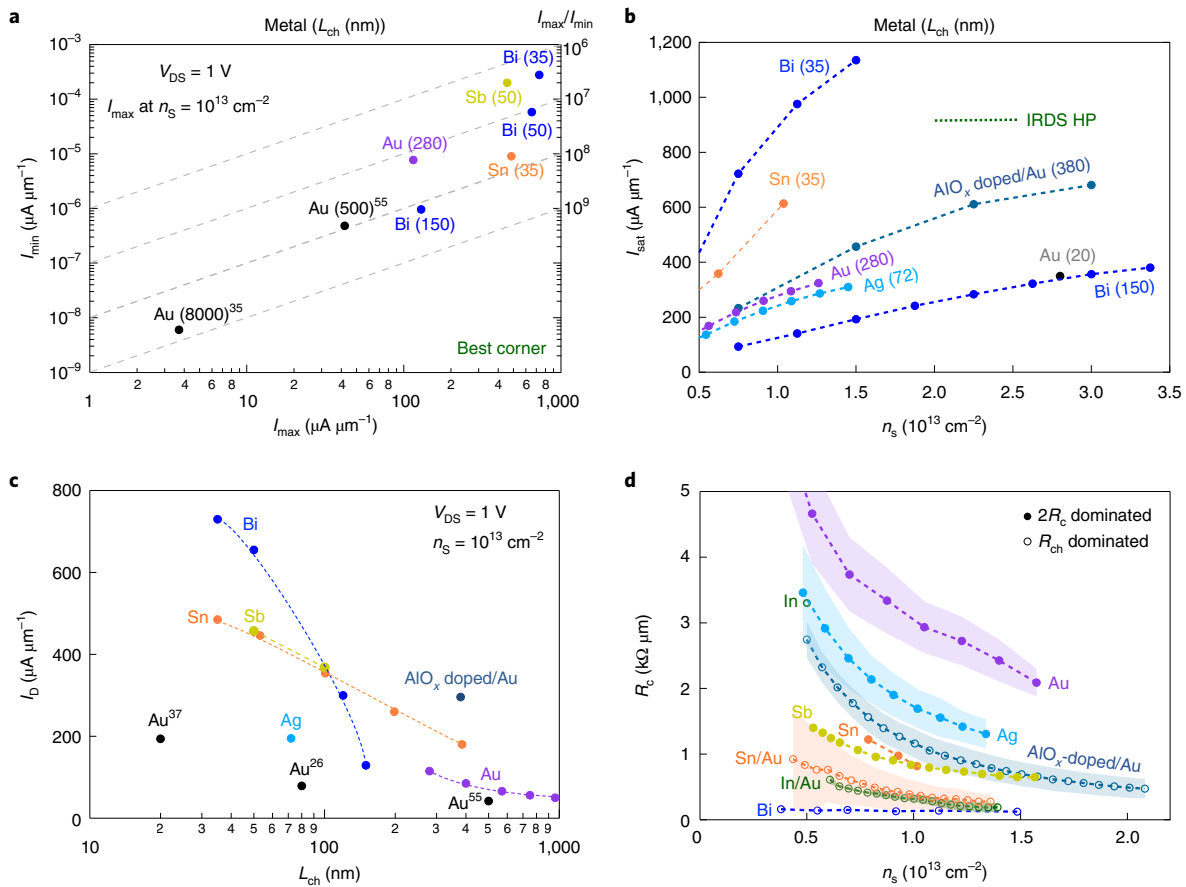


Fig. 3 | Example benchmarking device performance of monolayer MoS₂ FETs. a, Benchmarking I_{min} versus I_{max} . The I_{max} is extracted at $n_s = 10^{13}\text{ cm}^{-2}$. For simplicity, I_{min} values of the data points are extracted at their respective smallest current. More rigorous benchmarking of I_{min} versus I_{max} is described in Supplementary Note 1. **b**, Benchmarking I_{sat} versus n_s , where the channel length (in nm) is labelled next to the contact metals used in the devices. I_{sat} values are extracted at different V_{DS} (listed in Supplementary Table 1). These devices do not have the same $V_{DS}(\text{sat})$ as devices with different channel lengths and saturate at different V_{DS} . The IRDS high performance (HP) is shown in a range of n_s to represent uncertainties of the carrier density in future generation technologies. **c**, Benchmarking I_D versus L_{ch} at $V_{DS} = 1\text{ V}$ and $n_s = 10^{13}\text{ cm}^{-2}$. Reference⁵⁵ uses a top-gate, whereas other reports use a back-gate. **d**, Benchmarking R_c versus n_s in a few representative reports. The shaded regions represent uncertainties reported in the respective studies (Ag¹⁶ uses the 95% confidence interval, and In/Au⁵⁶, Sn/Au⁵⁶ and Au use standard error from the linear regression of TLM). The R_c versus n_s of Sb⁵⁷ is obtained using the Y-function method. The filled and open symbols show that the shortest channel device in the TLM structure is $2R_c$ and R_{ch} dominated, respectively. If R_{ch} dominates or the R_c is over an order of magnitude smaller than R_{tot} for the smallest device in TLM, the extracted R_c is of questionable validity; that is, the filled symbol data are more reliable (according to Supplementary Note 3). Different colours are assigned to different reported devices. The purple Au data denote devices described in Fig. 2. Most of the data are extracted from published reports: Ag¹⁶, AlO_x doped/Au⁵⁴, In/Au⁵⁶, Sn/Au⁵⁶, Sb⁵⁷, In⁵⁸ and Sn⁴⁰. In **a** and **c**, reference numbers are added for Au-contacted devices to better differentiate their performance. A few studies are plotted as dotted lines to highlight the trends and to improve the clarity of the plots.

multiple channels vertically to improve current density in the same device footprint³⁹.

In some reports, a proper saturation current is not given. Also, because different devices use different channel lengths, I_{sat} is often extracted at different V_{DS} . To highlight the impact of channel length, we recommend benchmarking I_D versus L_{ch} at $V_{DS} = 1\text{ V}$ and $n_s = 10^{13}\text{ cm}^{-2}$. This plot enables a direct comparison of devices with similar L_{ch} . In Fig. 3c, with channel length decreasing from 200 nm to 38 nm, devices contacted by both Bi³⁸ and Sn⁴⁰ yield relatively large increases in drain current. We note that the Bi-contacted devices are based on different MoS₂ films. The different quality of the MoS₂ may partially contribute to the large increase of I_D with a relatively small change in L_{ch} . Nevertheless, Fig. 3c,d presents the potential of atomically thin materials for producing high drain current, especially for scaled devices.

In Fig. 3d, R_c is plotted against n_s considering most devices have gated contacts (that is, the back-gate modulates the channel and

contacts^{32–34}). Although some reported R_c values reach below $500\ \Omega\mu\text{m}$, their TLM extractions are all based on channel resistance-dominated devices, which can lead to questionable validity in their claimed R_c (an artificially small or even a negative R_c can be extracted, see Supplementary Note 3 for details). We advocate that, if a record R_c is claimed from TLM, R_{sh} should be cross-examined by using other methods such as four-probe measurements, which can provide a relatively accurate estimation of R_{sh} versus n_s (Supplementary Note 3). With R_{sh} versus n_s from four-probe measurements, R_c versus n_s can be derived by deducting the $R_{ch} = R_{sh}L_{ch}$ from R_{tot} to confirm the TLM extracted value. Showing extraction of R_c from many TLM structures can also increase confidence in the data by providing an average value of the R_c rather than just the minimal value from a single TLM^{41,42}. Furthermore, R_c is heavily impacted by contact gating, as is evident from the similar trends of R_c versus n_s observed in different studies. Accordingly, further research is needed to obtain a small R_c without gating the contacts.

Looking forward, many opportunities remain to develop transistors that simultaneously have small contact resistance, high I_{sat} , large $I_{\text{max}}/I_{\text{min}}$ ratio and minimal short-channel effects by using emergent nanomaterials. To achieve this technological goal, interface engineering at the contacts and gate dielectric needs to be further investigated^{43–45}, along with progress in material synthesis⁴⁶ and integration⁴⁷. Moreover, it is important to focus on channel thicknesses below ~ 3 nm, where low-dimensional nanomaterials can excel compared to Si, which suffers from poor carrier transport properties and a widened bandgap in this thickness regime⁴⁸.

In addition to the example benchmarking plots in Fig. 3, other benchmarks can also be used to compare different devices, for example, as included in Table 2, plotting $I_{\text{max}}/I_{\text{min}}$ versus t_{ch} or $I_{\text{max}}/I_{\text{min}}$ versus L_{ch}/EOT to compare the off-state device performance. Plotting SS versus C_{ins} or SS versus $\log_{10}(I_{\text{D}})$ (ref. 49) can be used to evaluate subthreshold behaviour and trends across different devices. Finally, to show the quality of the channel materials, the channel sheet resistance or conductivity mobility can be plotted versus carrier densities, as in Fig. 2h. Representative reports with relatively large I_{sat} are listed in Supplementary Table 1, including results for FETs with both monolayer and multilayer MoS₂ channels (example benchmarking plots are provided in Supplementary Note 6). In the literature, notable benchmarking examples can be found in refs. 38,50, which highlight different channel materials, and in ref. 51, which focuses on device performance in integrated circuits (speed, gain, density, power consumption, fan-out capabilities, and so on).

Conclusions

Our guidelines should help put key performance metrics in a proper context and enable researchers to effectively report and benchmark emergent transistors based on various emergent nanomaterials. Although each of the listed metrics is important, it is not necessary—nor always possible—to extract and present all of them. As such, it is essential to completely describe the device geometry, to collect and report appropriate current–voltage characteristics, and to describe in detail the procedures followed in the experiments. The approaches used to analyse data and extract benchmarking metrics should also be described in detail. Depending on the context and need, we recommend three sets of parameters to report and benchmark. The first includes maximum saturation current, on/off current ratio, transconductance and subthreshold swing. These values can be directly obtained from the measured I – V characteristics that cover both linear and saturation regimes. These values are mainly determined by the intrinsic material properties, gate stack configuration and contact quality. The second includes the derived parameters such as mobilities and contact resistance, where uncertainty and statistical spread on these derived parameters should be shown. The third set of parameters are those specific to certain transistor demonstrations based on the target application^{52,53}. For example, DIBL is essential when reporting and evaluating ultra-scaled FETs. It is important—whenever possible—to benchmark against other novel materials and also the state of the art in mature technology^{38,50}. By using these guidelines, it should be possible to comprehensively and consistently reveal, highlight, discuss, compare and evaluate device performance, thus helping to identify advances and opportunities in the search for improved transistors.

Data availability

The data used in this paper are available from the corresponding authors upon reasonable request.

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References

- Chen, Z. et al. An integrated logic circuit assembled on a single carbon nanotube. *Science* **311**, 1735 (2006).
- Franklin, A. D. et al. Sub-10-nm carbon nanotube transistor. *Nano Lett.* **12**, 758–762 (2012).
- Geim, A. K. Graphene: status and prospects. *Science* **324**, 1530–1534 (2009).
- Ye, P. D. et al. Phosphorene an unexplored 2D semiconductor with a high hole mobility. *ACS Nano* **8**, 4033–4041 (2014).
- Tao, L. et al. Silicene field-effect transistors operating at room temperature. *Nat. Nanotechnol.* **10**, 227–231 (2015).
- Wang, Y. et al. Field-effect transistors made from solution-grown two-dimensional tellurene. *Nat. Electron.* **1**, 228–236 (2018).
- Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS₂ transistors. *Nat. Nanotechnol.* **6**, 147–150 (2011).
- Das, S., Chen, H. Y., Penumatcha, A. V. & Appenzeller, J. High performance multilayer MoS₂ transistors with scandium contacts. *Nano Lett.* **13**, 100–105 (2013).
- English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved contacts to MoS₂ transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).
- Sirringhaus, H. 25th anniversary article: organic field-effect transistors: the path beyond amorphous silicon. *Adv. Mater.* **26**, 1319–1335 (2014).
- Waldrip, M., Jurchescu, O. D., Gundlach, D. J. & Bittle, E. G. Contact resistance in organic field-effect transistors: conquering the barrier. *Adv. Funct. Mater.* **30**, 1904576 (2020).
- Li, S. et al. Nanometre-thin indium tin oxide for advanced high-performance electronics. *Nat. Mater.* **18**, 1091–1097 (2019).
- Li, M. Y., Su, S. K., Wong, H. S. P. & Li, L. J. How 2D semiconductors could extend Moore's law. *Nature* **567**, 169–170 (2019).
- Datye, I. M. et al. Reduction of hysteresis in MoS₂ transistors using pulsed voltage measurements. *2D Mater.* **6**, 011004 (2019).
- Streetman, B. G. & Banerjee, S. K. *Solid State Electronic Devices* 6th edn (Pearson, 2006).
- Smithe, K. K. H., English, C. D., Suryavanshi, S. V. & Pop, E. High-field transport and velocity saturation in synthetic monolayer MoS₂. *Nano Lett.* **18**, 4516–4522 (2018).
- Pinckney, N. et al. Impact of FinFET on near-threshold voltage scalability. *IEEE Des. Test* **34**, 31–38 (2017).
- Ortiz-Conde, A. et al. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **42**, 583–596 (2002).
- Ghibaudo, G. New method for the extraction of MOSFET parameters. *Electron. Lett.* **24**, 543–545 (1988).
- Chang, H. Y., Zhu, W. & Akinwande, D. On the mobility and contact resistance evaluation for transistors based on MoS₂ or two-dimensional semiconducting atomic crystals. *Appl. Phys. Lett.* **104**, 113504 (2014).
- Pang, C. et al. Mobility extraction in 2D transition metal dichalcogenide devices—avoiding contact resistance implicated overestimation. *Small* **17**, 2100940 (2021).
- Schroder, D. K. *Semiconductor Material and Device Characterization* 3rd edn (Wiley, 2015).
- Mleczo, M. J. et al. HfSe₂ and ZrSe₂: two-dimensional semiconductors with native high- k oxides. *Sci. Adv.* **3**, e1700481 (2017).
- Nasr, J. R., Schulman, D. S., Sebastian, A., Horn, M. W. & Das, S. Mobility deception in nanoscale transistors: an untold contact story. *Adv. Mater.* **31**, 1806020 (2019).
- Bittle, E. G., Basham, J. I., Jackson, T. N., Jurchescu, O. D. & Gundlach, D. J. Mobility overestimation due to gated contacts in organic field-effect transistors. *Nat. Commun.* **7**, 10908 (2016).
- Smithe, K. K. H., English, C. D., Suryavanshi, S. V. & Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS₂ devices. *2D Mater.* **4**, 011009 (2017).
- Franklin, A. D. Nanomaterials in transistors: from high-performance to thin-film applications. *Science* **349**, aab2750 (2015).
- Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **4**, 786–799 (2021).
- Pao, H. C. & Sah, C. T. Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors. *Solid State Electron.* **9**, 927–937 (1966).
- John, D. L., Castro, L. C. & Pulfrey, D. L. Quantum capacitance in nanoscale device modeling. *J. Appl. Phys.* **96**, 5180 (2004).
- Xu, H., Zhang, Z. & Peng, L.-M. Measurements and microscopic model of quantum capacitance in graphene. *Appl. Phys. Lett.* **98**, 133122 (2011).
- Appenzeller, J., Zhang, F., Das, S. & Knoch, J. in *2D Materials for Nanoelectronics* (eds Houssa, M. et al.) 207–240 (CRC Press, 2016).
- Arutchelvan, G. et al. From the metal to the channel: a study of carrier injection through the metal/2D MoS₂ interface. *Nanoscale* **9**, 10869–10879 (2017).

34. Prakash, A., Ilatikhameneh, H., Wu, P. & Appenzeller, J. Understanding contact gating in Schottky barrier transistors from 2D channels. *Sci. Rep.* **7**, 12596 (2017).
35. Illarionov, Y. Y. et al. Improved hysteresis and reliability of MoS₂ transistors with high-quality CVD growth and Al₂O₃ encapsulation. *IEEE Electron Device Lett.* **38**, 1763–1766 (2017).
36. *IEEE International Roadmap for Devices and Systems* (IEEE, 2020); <https://irds.ieee.org/>
37. Patel, K. A., Grady, R. W., Smithe, K. K. H., Pop, E. & Sordan, R. Ultra-scaled MoS₂ transistors and circuits fabricated without nanolithography. *2D Mater.* **7**, 015018 (2020).
38. Shen, P.-C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
39. Ahmed, Z. et al. Introducing 2D-FETs in device scaling roadmap using DTCO. In *Proc. 2020 International Electron Devices Meeting, IEDM 22.5.1–22.5.4* (IEEE, 2020); <https://doi.org/10.1109/IEDM13553.2020.9371906>
40. Chou, A. S. et al. High on-state current in chemical vapor deposited monolayer MoS₂ nFETs with Sn ohmic contacts. *IEEE Electron Device Lett.* **42**, 272–275 (2021).
41. Sebastian, A., Pendurthi, R., Choudhury, T. H., Redwing, J. M. & Das, S. Benchmarking monolayer MoS₂ and WS₂ field-effect transistors. *Nat. Commun.* **12**, 693 (2021).
42. Kumar, A., Tang, A., Philip Wong, H. S. & Saraswat, K. Improved contacts to synthetic monolayer MoS₂—a statistical study. In *Proc. IEEE International Interconnect Technology Conference 1–3* (IEEE, 2021); <https://doi.org/10.1109/IITC51362.2021.9537515>
43. Cheng, Z., Price, K. & Franklin, A. D. Contacting and gating 2-D nanomaterials. *IEEE Trans. Electron Devices* **65**, 4073–4083 (2018).
44. Illarionov, Y. Y. et al. Insulators for 2D nanoelectronics: the gap to bridge. *Nat. Commun.* **11**, 3385 (2020).
45. Cheng, Z. et al. Are 2D interfaces really flat? *ACS Nano* **16**, 5316–5324 (2022).
46. Zhou, J. et al. A library of atomically thin metal chalcogenides. *Nature* **556**, 355–359 (2018).
47. Liu, Y. et al. Van der Waals heterostructures and devices. *Nat. Rev. Mater.* **1**, 16042 (2016).
48. Uchida, K., Koga, J. & Takagi, S. Experimental study on electron mobility in ultrathin-body silicon-on-insulator metal-oxide-semiconductor field-effect transistors. *J. Appl. Phys.* **102**, 074510 (2007).
49. Haratipour, N., Namgung, S., Oh, S. H. & Koester, S. J. Fundamental limits on the subthreshold slope in Schottky source/drain black phosphorus field-effect transistors. *ACS Nano* **10**, 3791–3800 (2016).
50. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
51. Nikonov, D. E. & Young, I. A. Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits. *IEEE J. Explor. Solid State Comput. Devices Circuits* **1**, 3–11 (2015).
52. Abuzaid, H., Williams, N. X. & Franklin, A. D. How good are 2D transistors? An application-specific benchmarking study. *Appl. Phys. Lett.* **118**, 030501 (2021).
53. Lemme, M. C., Akinwande, D., Huyghebaert, C. & Stampfer, C. 2D materials for future heterogeneous electronics. *Nat. Commun.* **13**, 1392 (2022).
54. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS₂ doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
55. Lembke, D. & Kis, A. Breakdown of high-performance monolayer MoS₂ transistors. *ACS Nano* **6**, 10070–10075 (2012).
56. Kumar, A. et al. Sub-200 Ωμm alloyed contacts to synthetic monolayer MoS₂. In *Proc. IEEE International Electron Devices Meeting (IEDM)* 154–157 (IEEE, 2021).
57. Chou, A. et al. Antimony semimetal contact with enhanced thermal stability for high performance 2D electronics. In *Proc. IEEE International Electron Devices Meeting (IEDM)* 150–153 (IEEE, 2021).
58. Wang, Y. et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **568**, 70–74 (2019).

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Author contributions

All authors contributed to the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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