Spin-based Reconfigurable Logic for Power- and Area-Efficient Applications

Nikhil Rangarajan[†*], Satwik Patnaik[†*], Johann Knechtel[‡], Ozgur Sinanoglu[‡], and Shaloo Rakheja[†]

***Abstract*—The accelerated proliferation of portable and low-power computing devices in recent years has incentivized new paradigms in low-cost reconfigurable computing. Emergent devices, especially from the spin-domain, are promising in this design-space owing to their area efficiency, lower power dissipation, and reconfigurability. In this paper, we design a polymorphic spin-based logic for power- and area-efficient applications by exploiting the giant spin-Hall effect (GSHE) in heavy metals. The GSHE device offers $\sim 600\times$ reduction in area and $\sim 13.8\%$ reduction in power dissipation over 45-nm CMOS devices, while improving circuit modularity over CMOS FPGAs and reconfigurable computing platforms based on emergent devices. reconfigurable computing platforms based on emergent devices.**

***Index Terms*—Reconfigurable computing, spin-domain, giant spin-Hall effect, polymorphic gates, FPGA**

I. Introduction

The rapidly growing demand for low-power and area-efficient devices has been fueled by an unprecedented surge in portable and energy-aware applications like wearable electronics, wireless sensor-actuator systems, smart healthcare, transport and communication. Wireless sensor networks (WSN) and radio frequency identification (RFID) have become indispensable for remote sensing and identification in hazardous environments. Wearable electronics like smart watches, fitness trackers, biochips, and health monitors have diffused into our day-to-day lives. While virtually all these applications require (i) ultra-low power operation, (ii) low area footprint, and (iii) modularity or reconfigurability, the latency requirements for such systems are not very stringent. The thriving low-power electronics design-space is anticipated to become one of the largest sectors of the electronics industry in the coming decade. Recently, there has been a thrust towards reconfigurable and polymorphic systems based on novel devices for such low-power and area-constrained applications. Unique characteristics of emergent devices that make them an attractive option in this application-space include non-volatile data retention, near-zero leakage, ultimate scalability, and ease of integration with existing CMOS technologies.

A functionally enhanced all spin logic (ASL)-based architecture was proposed in [1], which achieves runtime reconfiguration between INV/BUF by changing the orientation of the polarizing magnets. In [2], a hybrid spin-CMOS threshold logic gate leveraging a four-terminal spin Hall effect-based domain wall motion (DWM) device is presented. This design implements AND/NAND, OR/NOR, XOR/XNOR logic at femto-Joule operating energies and nanosecond delays. Ambipolar silicon nanowire field effect transistors (SiNW FETs) that can realize NAND/NOR or XOR/XNOR logic with improved logical efficiency as compared to CMOS were proposed in [3]. A hybrid logic circuit that uses memristive crossbar arrays functioning as the reconfigurable data routing network, fabricated on top of a CMOS layer, was demonstrated in [4]. This hybrid memristor-CMOS architecture is able to implement AND/OR/NAND/NOR/INV and D flip-flop functionalities, and offers significant benefits in terms of power consumption and non-volatility of the memristor, but requires additional circuitry to integrate the crossbar array with CMOS circuitry. The authors in [5] implement a spin-based logic design by integrating a magnetic tunnel junction (MTJ) on top of a giant spin-Hall metal layer, to realize AND/OR/NAND/NOR operations. However, the different logic functions are achieved by changing the switching threshold of the MTJ during manufacturing, and hence this logic is not reconfigurable or runtime polymorphic. The DWM-based five-terminal device proposed in [6] is able to implement basic Boolean logic functions (except buffer) within one device. However, this design requires 13 additional CMOS transistors per gate, which exacerbates the power and area cost.

In this paper, we propose a spin-based reconfigurable logic family by exploiting the runtime polymorphism of the giant spin-Hall effect (GSHE) device [7]. The GSHE device is capable of implementing all 16 Boolean functions of two variables, including the eight basic Boolean gates (INV/BUF/AND/OR/NAND/NOR/XOR/XNOR), using a single device. It requires minimal additional CMOS circuitry to achieve this, and is able to switch between the different logic functionalities dynamically on-the-fly. This exceptional feature coupled with its reduced power and area footprints make it an ideal candidate for portable low-power and area-efficient applications. The runtime reconfigurability imparts GSHE logic with the ability to implement various applications on a single chip, and switch between the functionalities as and when required. Such a design would result in tremendous gains in area, power, and lifetime of systems such as those deployed for remote sensing. We note here that in GSHE logic, the gates themselves morph to perform multiple functions, which is in contrast to conventional CMOS FPGA architectures that have a reconfigurable routing fabric in addition to configurable logic blocks. The GSHE logic could also have a huge potential for future 5G mobile communication systems to implement load or protocol-dependent dynamically morphing systems.

The main contributions of this paper are:

[†] N. Rangarajan, S. Patnaik and S. Rakheja are with the Department of Electrical and Computer Engineering, New York University, 2 MetroTech Center, Brooklyn, NY, USA 11201. E-mail: (nikhil.rangarajan, sp4012, shaloo.rakheja)@nyu.edu

[‡] J. Knechtel and O. Sinanoglu are with the Division of Engineering, New York University Abu Dhabi, Saadiyat Island, Abu Dhabi, UAE 129188. E-mail: (johann, ozgursin)@nyu.edu

[*] N. Rangarajan and S. Patnaik contributed equally.

(1) To highlight the implementation of the various Boolean logic functions using the GSHE device,
(2) To analyze the dynamic reconfigurability of the GSHE logic, and to evaluate the area, power, and delay metrics of the implemented GSHE logic,
(3) To compare the performance metrics of benchmark circuits implemented using GSHE logic against those of CMOS-based implementations and other polymorphic gates proposed in prior works.

The proposed GSHE logic is shown to outperform CMOS in terms of aggregate area and power metrics. Although other emerging technologies like the SiNWFET-based scheme in [3] offer more competitive delay and power metrics, GSHE logic offers a higher integration density and greater modularity in terms of reconfigurable functions implemented.

II. GSHE Device Model

The GSHE device, illustrated in Fig. 1(a), relies on the phenomena of spin-Hall effect and magnetic dipolar coupling to implement Boolean logic functions. Upon the injection of a charge current (orange arrow in Fig. 1(a)) into the giant spin-Hall layer (blue in Fig. 1(a), typically composed of a heavy metal (HM) like W, Pt or Pd), a spin accumulation of opposite polarities arises on the lateral surfaces of the layer [7]. The direction of spin accumulation is orthogonal to the direction of the injected charge current, with the polarization of the spin current being orthogonal to both of them. In Fig. 1(a), the charge current is assumed to be along $\hat{x}$, while the spin accumulation and polarization directions are along $\hat{y}$ and $\hat{z}$, respectively. The polarized spin current imparts a torque to the magnetization vector of the free write (W) nanomagnet (peach in Fig. 1(a)) through the spin-transfer torque (STT) mechanism. The W nanomagnet is magnetically coupled to the read (R) nanomagnet (also in peach) via their mutual dipolar coupling. We consider a negative coupling, which means that in equilibrium, the magnetizations of W and R nanomagnets are anti-parallel to each other. Hence, when the STT acts on the W nanomagnet to switch it from one stable state to the other, the R nanomagnet will also switch, but in the opposite direction. Once the information is transferred from the W nanomagnet to the R nanomagnet, an output electrical current is generated via an MTJ stack using two fixed nanomagnets (dark green in Fig. 1(a)) sitting atop the R nanomagnet. Since the two fixed nanomagnets in the MTJ are configured in an anti-parallel fashion, the final magnetization state of the R nanomagnet will be parallel to one of the fixed nanomagnets and anti-parallel to the other. Voltage signals of opposite polarities are applied to contacts on top of each of the fixed nanomagnets. The MTJ in which the R nanomagnet is parallel to the fixed nanomagnet (V^- in Fig. 1(a)) will offer a lower resistance path for the output electrical current. By reversing the polarities of the MTJ supply voltages, the direction of the output electrical current can be flipped. The direction of the electrical current determines the logic state; therefore, interchanging the voltage polarities (V^+ and V^-) switches the operation of this basic device setup from an inverter to a buffer (or vice versa), as shown in Fig. 1(b).

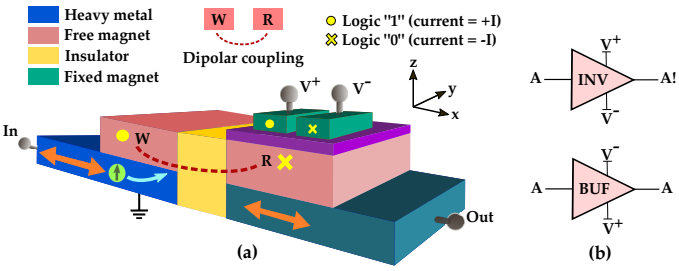
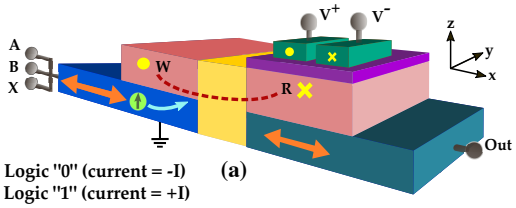


Fig. 1: (a) Construction and operation of the GSHE switch. A charge current (orange arrow) supplied to the heavy metal layer produces a spin current, which results in STT-induced switching of the W nanomagnet. Dipolar coupling with the W nanomagnet switches the R nanomagnet, and logic read-out is achieved via an MTJ arrangement on the R side. The GSHE switch in this figure is laid out horizontally for better clarity, but will be fabricated as a vertical stack. (b) Realizing inverter and buffer operations with the GSHE switch. Polarity of voltages on top of the fixed nanomagnets decides the direction of the output electrical current and, therefore, the output logic state.

III. Complex Logic using the GSHE Device

A. Implementation of NAND / NOR / AND / OR

NAND/NOR gates are implemented with the GSHE device using the setup shown in Fig. 2(a). Three current domain signals, A, B and X, are fed into the input terminal of the GSHE device. While A, B are the primary inputs, input X is a tie-breaking signal, which is required to implement an even-input gate, as seen from the truth tables in Fig. 2(b). By choosing $X = +I$, the gate exhibits the functionality of a two-input NAND gate, while $X = -I$ transforms the gate into a two-input NOR gate. That is, changing the direction of current X during operation will dynamically reconfigure the gate from NAND to NOR or vice versa.



X= -I

A	B	X	I (total)	Out
-I	-I	-I	-3I	+I
-I	+I	-I	-I	+I
+I	-I	-I	-I	+I
+I	+I	-I	+I	-I

X= +I

A	B	X	I (total)	Out
-I	-I	+I	-I	+I
-I	+I	+I	+I	-I
+I	-I	+I	+I	-I
+I	+I	+I	+3I	-I

(b)

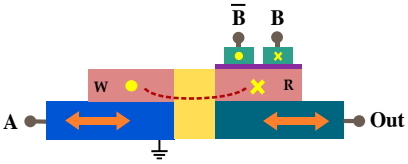
Fig. 2: (a) Configuration of GSHE device for NAND/NOR operation. (b) Realization of NAND/NOR and their respective truth tables.

In general, n-input logic gates can be constructed directly using the same setup shown in Fig. 2(a) if $X = \pm(n-1)I$. Alternately, two-input GSHE gates may be cascaded to implement complex gates with a higher fan-in. The effect of increasing the number of inputs is that the total spin current feeding into the W nanomagnet increases, thereby reducing the switching delay of the device, albeit at the cost of higher power consumption. For a detailed analysis on the power-delay optimization of the GSHE device, the reader is referred

to [7]. Here, I is formulated in terms of the critical current for the W nanomagnet, which will be used for calculating the performance metrics of the device in Section IV. Finally, to implement AND/OR gates, the polarities of the voltages on the fixed nanomagnets in the MTJ stack must be flipped ($V^{+/-} \rightarrow V^{-/+}$).

B. Implementation of XOR / XNOR

To realize XOR logic, the tie-breaking signal X is eliminated. One of the primary inputs (say A) is applied as a current domain signal, while the other primary input and its complement (B and $\overline{B}$) are applied as voltages to the $\times$ and $\bullet$ fixed nanomagnets in the MTJ stack. The gate configuration



(a)

A	W	R	B	B̄	Out
-I	✖	•	✖	•	-I
-I	✖	•	•	✖	+I
+I	•	✖	✖	•	+I
+I	•	✖	•	✖	-I

(b)

Fig. 3: (a) Implementation of XOR logic using the GSHE gate. (b) Truth table for XOR operation. $\times$ (into the plane) and -I correspond to logic 0 whereas $\bullet$ (out of the plane) and +I correspond to logic 1. In the truth table, W, R, B and B' refer to the orientation of the write and read nanomagnets, and the fixed magnets connected to the B and B' voltage terminals respectively.

and truth table for XOR operation is shown in Fig. 3. Here, for instance, applying a current of $-I$ as the input A (first row of the truth table) sets the W nanomagnet in $\times$ orientation, and the R nanomagnet in $\bullet$ orientation. Now, applying B and $\overline{B}$ on the $\times$ and $\bullet$ fixed nanomagnets, respectively, will result in an output current flowing into the device ($-I$). This is because $\overline{B}$ is applied on the fixed nanomagnet that is parallel to the R nanomagnet. The XOR gate can be converted to an XNOR gate by interchanging B and $\overline{B}$ on the voltage terminals.

C. Implementation of majority logic

A	B	C	I (total)	W	R	V⁺	V⁻	Out
-I	-I	-I	-3I	✖	•	✖	•	-I
-I	-I	+I	-I	✖	•	✖	•	-I
-I	+I	-I	-I	✖	•	✖	•	-I
-I	+I	+I	+I	•	✖	✖	•	+I
+I	-I	-I	-I	✖	•	✖	•	-I
+I	-I	+I	+I	•	✖	✖	•	+I
+I	+I	-I	+I	•	✖	✖	•	+I
+I	+I	+I	+3I	•	✖	✖	•	+I

Fig. 4: Truth table of majority gate implemented with the GSHE device.

The GSHE device can directly implement a three-input majority logic gate, for which the truth table is shown in Fig. 4. The three inputs are applied as current signals at the input terminal, while the control signal X is eliminated. Voltage V^+ is applied on the fixed nanomagnet oriented along $\times$, and V^- is applied on the fixed nanomagnet along $\bullet$. As before, the polarity of the voltage signals on the MTJ stack and the magnetization state of the R nanomagnet determines the direction of the output electrical current and, therefore, the Boolean logic function realized by the gate.

IV. Runtime Polymorphism of GSHE Logic

The dynamic reconfigurability of GSHE logic is extremely advantageous in terms of area savings, since multiple functions can be implemented on the same chip. Among others, this is particularly compelling for Internet of Things (IoT) systems. Consider, for instance, a remotely deployed sensor-actuator system that senses environmental signals periodically, stores them in a built-in memory, and actuates a response once a certain threshold has been crossed. This system can be very efficiently implemented using GSHE logic, on a single chip. The circuitry would initially be configured to function as a sensor that samples and stores the incoming stimulus, and then reconfigured to implement the actuator circuit, which responds according to the stored data.

Besides this general motivation, we next discuss the implementation of (i) all 16 possible Boolean functions for two inputs, and (ii) a polymorphic full adder/subtractor circuit, all using the GSHE device.

A. Full set of Boolean functions and peripheral circuitry

The GSHE device is uniquely able to implement not only majority logic, but all 16 possible Boolean functions of two variables (Fig. 5) and dynamically morph between them. This level of polymorphism and reconfigurability is afforded in the GSHE device due to the structural differences and extra degrees of tunability that it possesses as compared to other emerging device designs (e.g., [1, 2]), namely the voltage polarities applied to output MTJ stacks. The reconfiguration at the circuit-level is achieved using control circuitry as shown in Fig. 6, where the control bits (K_1 to K_{11}) in the MUX setup determine the functionality of the particular GSHE gate. A magneto-electric (ME) switching-based transducer [8] is added at the output of the GSHE gate to transduce the output current as required for the fan-out stages. Such transducers are capable of (i) charge current to charge current conversion ($+I/B$ to $-I/\overline{B}$), (ii) voltage to charge current conversion (high/low voltage levels to $+/-I$), and (iii) charge current to voltage conversion ($+/-I$ to high/low levels).

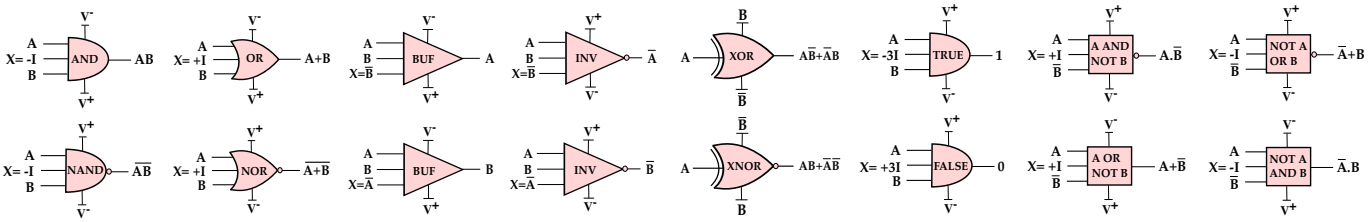


Fig. 5: All 16 possible Boolean functionalities for two inputs, A and B, implemented using the GSHE device. Note that the inverse of B ($\overline{B}$) is available through magneto-electric switching-based transducers [8] placed in the interconnects. Adapted from [9].

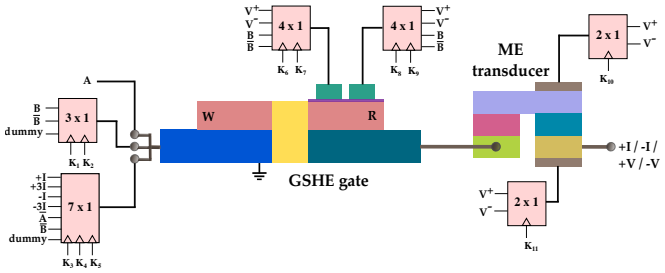


Fig. 6: Control circuit scheme for configuring the GSHE device to implement any of the 16 Boolean functionalities depicted in Fig. 5. The ME transducer is to transduce the output current as needed for the fan-out stages.

B. Polymorphic full adder/subtractor

Full adders and subtractors are essential logic modules and are pervasively used in any integrated circuit, including IoT devices. A 1-bit full adder/subtractor can be realized using two XOR gates and one Majority gate as follows [6]:

(a) Full adder

$$\text{Sum} = A \oplus B \oplus C, \quad \text{Carry} = MAJ3(A, B, C) \quad (1)$$

(b) Full subtractor

$$\text{Diff} = A \oplus B \oplus C, \quad \text{Borrow} = MAJ3(\overline{A}, B, C) \quad (2)$$

We use the configuration shown in Fig. 7 to implement these circuits. Here we leverage the reconfigurability of the GSHE device for the transformation of a full adder to a full subtractor without any modifications at the layout level. Gate $X3$ functions as a buffer for the full adder and as an inverter to achieve the full subtractor, and changing the voltage polarities on $X3$ allows one to dynamically change between the two circuits. This implementation is essentially different from CMOS-based adder-subtractor circuits, which are not reconfigurable and, hence, require $1.5\times$ the number of gates. Whereas, using low-power GSHE logic, one can achieve both functions at a fraction of that area and power. We note here that the ASL-based and DWM-based designs in [1] and [2] respectively are also able to implement majority logic using a tie-breaking signal, owing to the additive nature of the input spin currents.

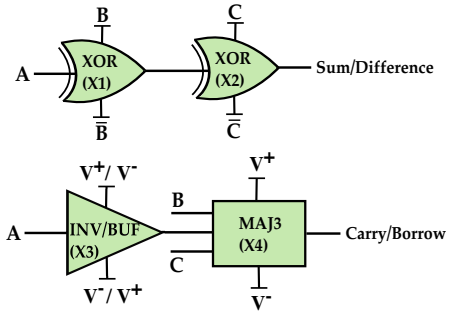
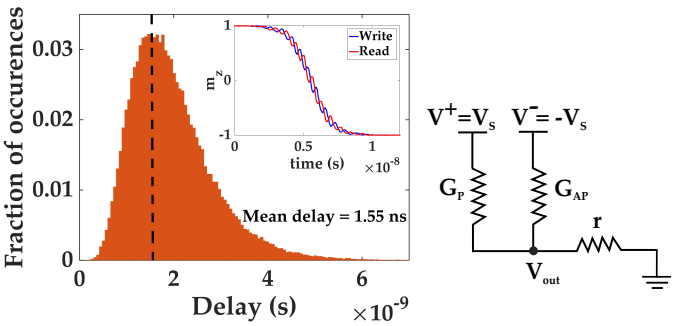


Fig. 7: Dynamic reconfiguration of full adder to full subtractor and vice versa using GSHE XOR, INV/BUF and MAJ3 gates.

Now, to showcase the system level performance of the proposed design, we present a comparison of a 32-bit ripple carry adder circuit to be implemented using GSHE versus CMOS. The CMOS adder is constructed using the 65 nm technology node and is optimized for IoT systems [10]. To obtain the metrics for the GSHE 32-bit ripple carry adder, we first evaluate the area, power, and delay (APD) metrics of an individual GSHE gate. The geometrical and material parameters of the GSHE device used for analysis paper are given in Table I. To deterministically switch the state of the GSHE device, a critical spin current of $I_S = 20\ \mu$A is required (details can be found in [7]). Even though the switching process is deterministic, the delay of magnetization reversal is stochastic and subject to a distribution as depicted in Fig. 8(a). The average delay in an ensemble of $100,000$ simulations is 1.55 ns. While constructing a large circuit using GSHE logic, some of the gates in the critical path would be faster than the average case, while some would have a delay greater than 1.55 ns. Hence, we assume 1.55 ns as the delay of each gate in the critical path for the purpose of evaluating circuit-level delay metrics. This translates to circuit-level speeds of typically a few 10's to 100's of MHz, which, even though slower than CMOS circuits, is acceptable for IoT systems. Process variations in the device ($\pm 10\%$ variation in nanomagnet thickness) would result in shifting of the delay distribution and mean delay. However, those effects are negligibly small as compared to the intrinsic thermal variability in the device, and are hence not considered.



(a) Probability density function of delays of GSHE device at input spin current of 20μA.

(b) Circuit representation of the GSHE device.

Fig. 8: Obtaining delay and power of the GSHE device. Inset of (a) shows typical magnetization trajectories of the dipolar-coupled read and write nanomagnets of the GSHE device.

Figure 8(b) illustrates the circuit representation of the GSHE device, for calculating its power dissipation. The total power of the GSHE device, including MTJ leakage, is given as

$$P_{\text{GSHE}} = \frac{V_{\text{out}}^2}{r} + (V_S - V_{\text{out}})^2 G_P + (V_S + V_{\text{out}})^2 G_{AP}, \quad (3a)$$

$$V_{\text{out}} = \frac{I_S\ r}{\beta}; \qquad V_S = \frac{I_S}{\beta}\left[\frac{1 + r(G_P + G_{AP})}{G_P - G_{AP}}\right], \quad (3b)$$

where V_S is the voltage applied to the MTJ stack, G_P and G_{AP} are the parallel and anti-parallel conductances of the MTJ stacks, r is the resistance of the giant spin-Hall HM, and $\beta = \frac{I_{\text{spin}}}{I_{\text{elec}}} = \theta_{SH}\left(\frac{w_{nm}}{t_{hm}}\right)$ is the internal gain of the HM. Here, w_{nm} is the width of the nanomagnets and t_{hm} is the thickness of the HM layer. G_P and G_{AP} are calculated from the TMR and RAP values given in Table I as $420\ \mu$S and $155.6\ \mu$S, respectively. Considering a HM layer 46 nm long, the thickness and resistivity of the HM in Table I yield $r \sim 1k\Omega$. These values result in a total power of $0.2125\ \mu$W for the GSHE device, from (3a). Note that this power is for a spin current equal to

the critical current of 20μA. Increasing the spin current further will result in an improved delay for the device, but at the cost of higher power consumption. The layout of the GSHE device, illustrated in Fig. 9, was created according to the design rules for beyond-CMOS devices, formulated in units of maximum misalignment length λ. The area of the GSHE device derived from this layout is $0.0016\ \mu\text{m}^2$.

TABLE I: Specifications of GSHE device, extended from [7].

Parameter	Value
Volume	$(28 \times 15 \times 2)$ nm^3
Saturation magnetization (M_s)	10^6 A/m (W) 5×10^5 A/m (R)
Uniaxial energy density (K_u)	2.5×10^4 J/m^3 (W) 5×10^3 J/m^3 (R)
Critical spin current (deterministic switching)	20 μA
Resistance area product (RAP)	$1\Omega\mu\text{m}^2$ [11]
Tunneling Magnetoresistance (TMR)	170% [11]
G_P	420×10^{-6} S
G_{AP}	155.6×10^{-6} S
Spin-Hall angle (θ_{SH})	0.4
Internal gain of HM (β)	6
Thickness of HM (t_{hm})	1nm
Resistivity of HM	$5.6 \times 10^{-7}\Omega$m

Utilizing the GSHE device metrics obtained above, we evaluate the overall performance of the GSHE 32-bit ripple carry adder, which is illustrated in Fig. 10. As seen from this figure, the GSHE-based circuit offers significant improvements in terms of area and power over the CMOS implementation. Hence, the GSHE design is particularly advantageous for implementing logic modules in IoT chips with stringent power and area constraints.

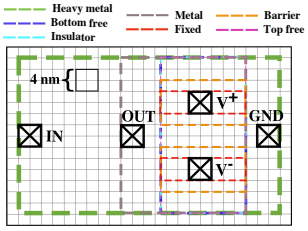


Fig. 9: Layout of GSHE gates for a vertically stacked structure – the read unit is built on top of the write unit for better coupling. Free and fixed refer to the nanomagnets in the device.

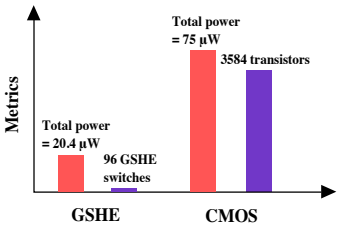


Fig. 10: Comparison of total power and device count for a 32-bit adder. For CMOS, the adder considered is the dual rail design from [10], optimized for IoT circuits.

V. Benchmarking

In this section, we compare the area, power, and delay (APD) metrics of benchmark circuits implemented using four techniques: (i) GSHE logic, (ii) CMOS, (iii) DWM switches in [6], and (iv) triple-insulated gate (TIG) SiNWFET in [3]. We utilize 10 benchmark circuits from the ISCAS'85 benchmark suite. All simulations are carried out using *Cadence Innovus* at the 45 nm technology node, utilizing the typical process corner. For a fair comparison, we first obtain the CMOS implementation of a given benchmark, and assume that the other, emerging device-based implemenations would be constructed using a one-to-one replacement of all CMOS gates. The APD metrics for CMOS, [6], [3], and our proposed approach are outlined in Table II. Compared to the CMOS implementation, our approach scales particularly well for area, with an average saving of $\sim 600\times$ across all benchmarks used in this work. Note here that this improvement is obtained only from the gate area, as we are considering similar interconnect dimensions for CMOS and GSHE logic. With respect to power consumption, GSHE logic achieves an average reduction of 13.8% when compared to CMOS-based implementations. However, the power savings are considerably higher when compared to [6], where, on an average, we achieve a reduction of $\sim 74\times$. As compared to the SiNWFET-based design in [3], GSHE circuits exhibit an order of magnitude more power dissipation. However, the average area saving afforded by GSHE logic is $\sim 435\times$ as compared to [3].

Note that the power and delay metrics reported for GSHE logic in Table II include the overheads incurred in the ME transduction peripheral unit shown in Fig. 6. For calculating the delay, we determine the critical path of every design under consideration and keep track of all the logic gates that make up the critical path. This allows us to estimate the delay when the same circuits are constructed with GSHE gates. For example, 10 CMOS logic gates in the critical path would result in a delay of ~ 18 ns in the GSHE logic version of the circuit—the delay of each GSHE gate is 1.55 ns (Section IV) and the delay of each magneto-electric transducer is ~ 0.25 ns. Accordingly, the benchmarks listed in Table II can be operated at frequencies of 14–50 MHz for the GSHE logic versions, which is lower than for classical CMOS implemenations (186–556 MHz), but it is important to note that the GSHE-based circuits are far more economical in terms of area and power. As the primary requirement of power- and area-efficient systems, like IoT devices, is not necessarily a fast operating mode, we believe this increased delay of GSHE logic would not become a prohibitive factor in the design of such circuits.

Considering an aggregate metric, i.e., the ADP product, both the TIG SiNWFET and the proposed GSHE logic outperform CMOS, with TIG SiNWFET exhibiting the best ADP product of all. However, GSHE logic enables the highest integration density owing to its smaller footprint. It also exhibits unique and promising properties such as non-volatility and the capability to operate with tunable stochasticity, which are not found in other emerging devices. These properties make the GSHE device suitable for novel computing paradigms like neural computing [12]. In terms of modularity and reconfigurability, GSHE logic is the "clear winner" as it can implement more logic functionalities (namely all 16 for two inputs) using the same device than any other emerging device-based scheme. With regards to improving the delay and power metrics of spin Hall devices as compared to emerging technologies like the TIG SiNWFET, new device setups based on the colossal spin Hall effect in topological insulators (TI) could also be used within the proposed framework, to achieve ultra-low power dissipation and latency. The spin Hall angle in TIs is manifolds greater ($\sim 10\times$) than that in heavy metals, and can considerably increase the efficiency of charge to spin conversion in the device. The implications of such setups will

TABLE II: Area (A), power (P), and delay (D) comparison for selected benchmarks. Note that the authors of [6] do not provide any area estimate. However, their device dimensions and the need for peripheral CMOS circuits imply that the area is considerably larger than for our proposed GSHE logic. The power and delay metrics for the GSHE implementation include the overheads incurred from the magneto-electric transduction in the interconnects.

Benchmark	CMOS			DWM logic [6]			TIG SiNWFET [3]			Proposed GSHE logic		
	A(μm^2)	P(mW)	D(ns)	A(μm^2)	P(mW)	D(ns)	A(μm^2)	P(mW)	D(ns)	A(μm^2)	P(mW)	D(ns)
c432	129.011	0.036	2.087	–	1.0	26	100.89	0.00187	0.30	0.261	0.040	43.2
c499	232.218	0.074	1.797	–	1.2	15	188.41	0.00366	0.28	0.299	0.046	23.4
c880	290.472	0.077	1.784	–	2.1	22	219.42	0.00404	0.24	0.531	0.084	28.8
c1355	234.346	0.083	2.072	–	2.0	14	166.87	0.00334	0.29	0.301	0.046	19.8
c1908	283.822	0.084	2.328	–	3.6	21	207.20	0.00375	0.33	0.451	0.070	34.2
c2670	459.116	0.128	1.821	–	5.6	20	269.68	0.00494	0.22	0.824	0.129	28.8
c3540	856.521	0.263	2.799	–	8	32	515.74	0.00932	0.42	1.626	0.256	39.6
c5315	1,073.842	0.245	2.538	–	11	28	662.60	0.01202	0.31	1.936	0.305	36
c6288	1,936.481	0.795	5.371	–	75	58.9	1814.34	0.03292	1.08	3.394	0.534	73.8
c7552	1,122.254	0.308	3.325	–	24	72.2	852.10	0.01594	0.27	1.869	0.294	37.8

be explored in a future work.

VI. Conclusion

This paper introduces a novel spin-based reconfigurable logic design suitable for low-power and low-area applications, by utilizing polymorphic GSHE gates. These gates, which leverage the giant spin-Hall effect in heavy metals, are capable of implementing various Boolean logic functions using a single device, and exhibit the ability to dynamically morph between different gates on-the-fly. Compared to existing CMOS-based and other emergent devices-based reconfigurable systems, GSHE devices exhibit significant area and power savings, while operating at 10's–100's of MHz speeds that are sufficient especially for power- and area-efficient circuits. Integrating these spin-based polymorphic gates with conventional reconfigurable interconnects opens up new avenues in the field of reconfigurable computing.

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N ikhil Rangarajan is a Ph.D. candidate at the department of Electrical and Computer engineering, New York University, New York, NY, USA. He has an M.S. in electrical engineering from New York University. His research interests include spintronics, nanoelectronics and device physics. He is a student member of IEEE.

S atwik Patnaik is a Ph.D. candidate at the department of Electrical and Computer engineering, New York University, New York, NY, USA. His research interests include security and trust issues for CMOS and emerging devices and low power VLSI design, and has an M.Tech. in Computer Science from Indian Institute of Information Technology, Gwalior, India. He is a student member of IEEE, ACM, SIGDA.

J ohann Knechtel is a Postdoctoral Associate at New York University Abu Dhabi. Previously, he was with Masdar Institute of Technology, UAE (2015–16), TU Dresden, Germany (2010–14, PhD in Computer Engineering), as well as a visiting researcher with CUHK, China (2012) and UMich, USA (2010). His research is on Electronic Design Automation, particularly in the context of emerging technologies and hardware security. Dr. Knechtel is a member of IEEE (knechtel@ieee.org).

O zgur Sinanoglu is a Professor of Electrical and Computer engineering at New York University Abu Dhabi. He obtained his PhD in Computer Science and Engineering from University of California San Diego. He has industry experience at TI, IBM and Qualcomm, and has been with NYU Abu Dhabi since 2010. Prof. Sinanoglu's research interests include reliability and security of VLSI circuits, where he has around 160 conference and journal papers, and 20 issued and pending US Patents.

S haloo Rakheja is an Assistant Professor of Electrical and Computer engineering with New York University, Brooklyn, NY, USA, where she works on nanoelectronic devices and circuits. Prior to joining NYU, she was a Postdoctoral Research Associate with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, USA. She obtained her M.S. and Ph.D. degrees in electrical and computer engineering from Georgia Institute of Technology, Atlanta, GA, USA.