Physical Design Automation for 3D Chip Stacks – Challenges and Solutions

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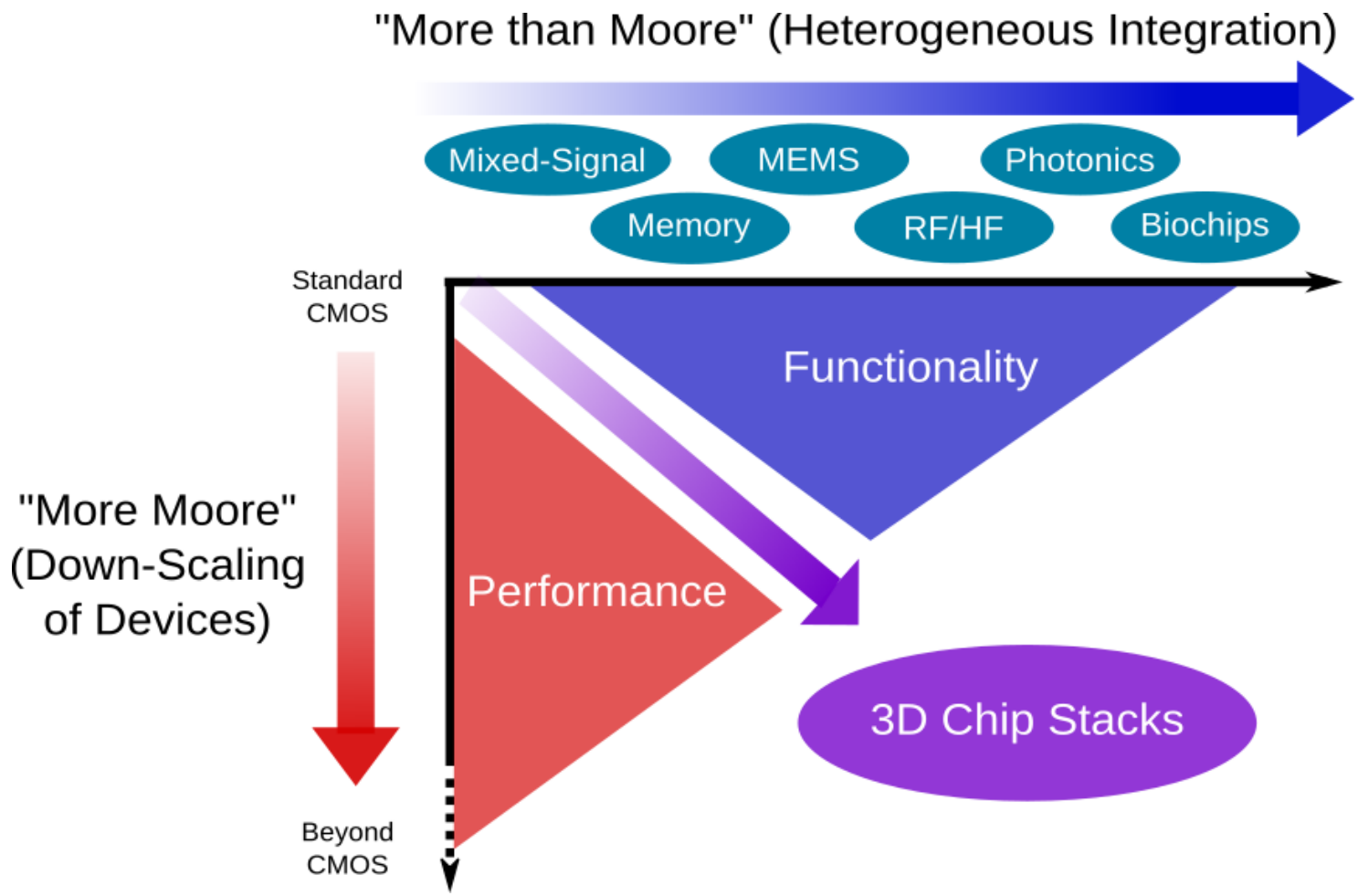
TwinLab "3D Stacked Chips"
Masdar Institute and TU Dresden

ISPD 2016, April 4

Outline

1. Introduction: Motivation and 3D Chip Stacking Options
2. Classical Challenges – Aggravated but Solvable
3. Novel Design Challenges and Emerging Solutions
4. Summary

3D Chip Stacks: Meeting Trends for Modern Chip Design



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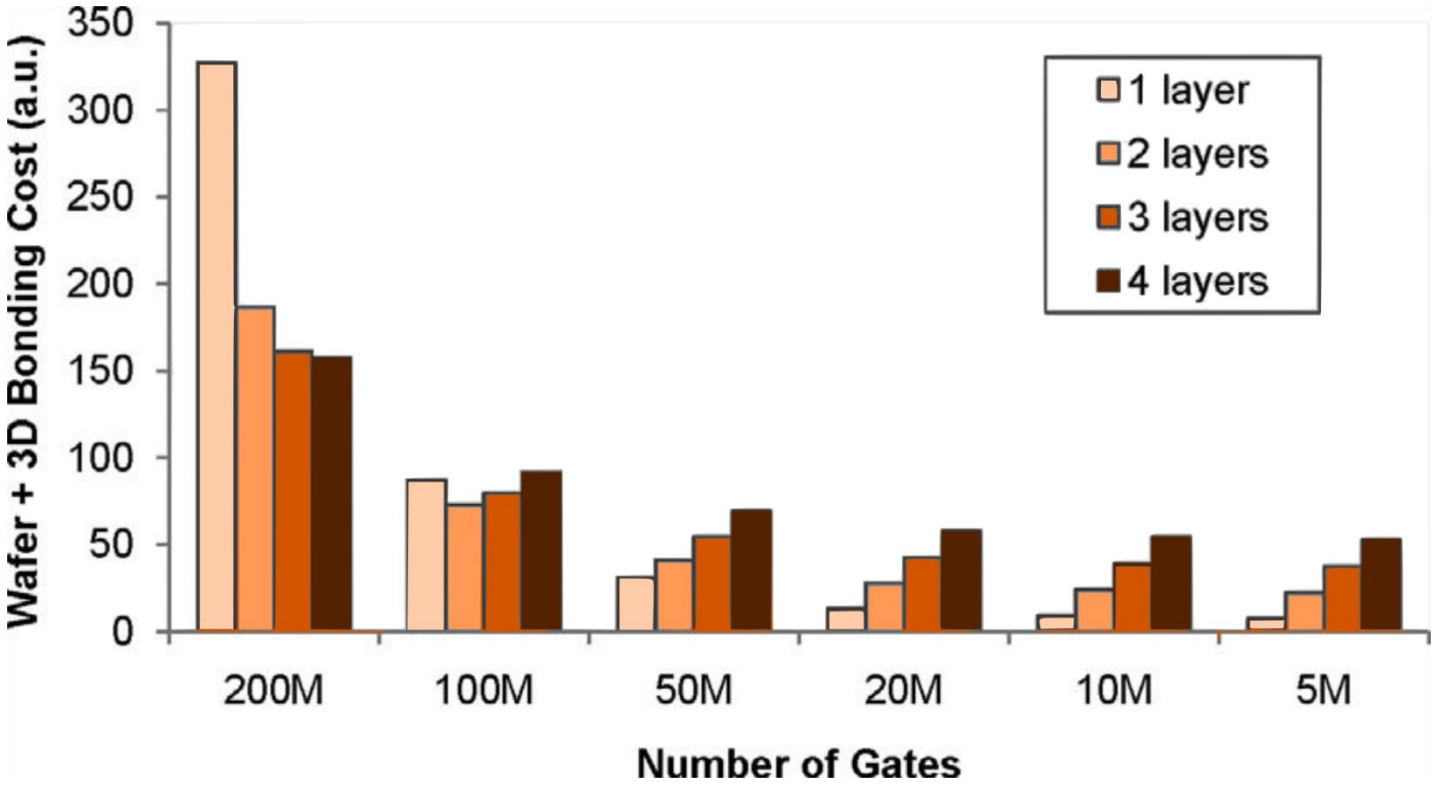
3D Chip Stacks: Cost Benefits



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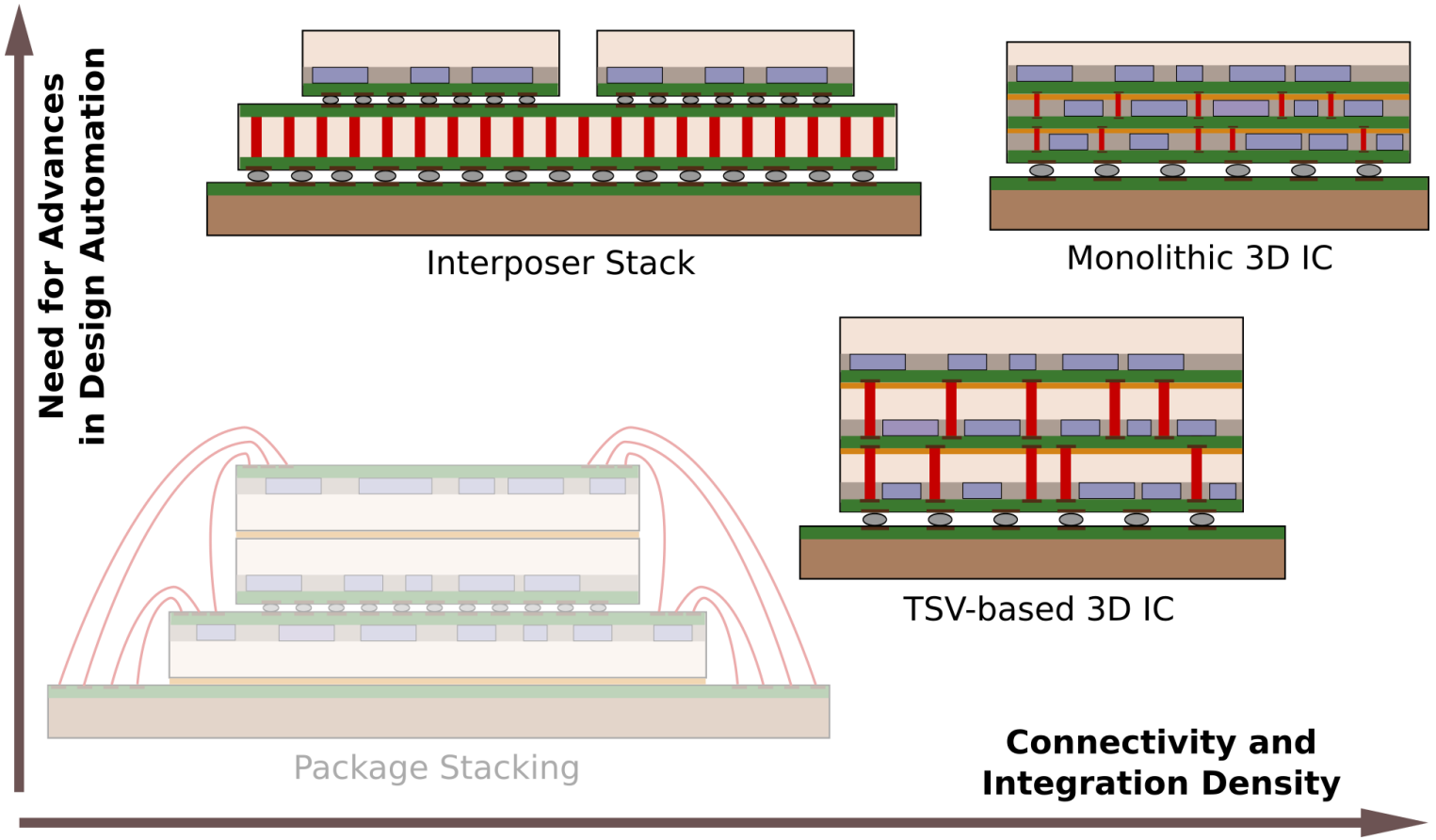
3D Chip Stacking Options



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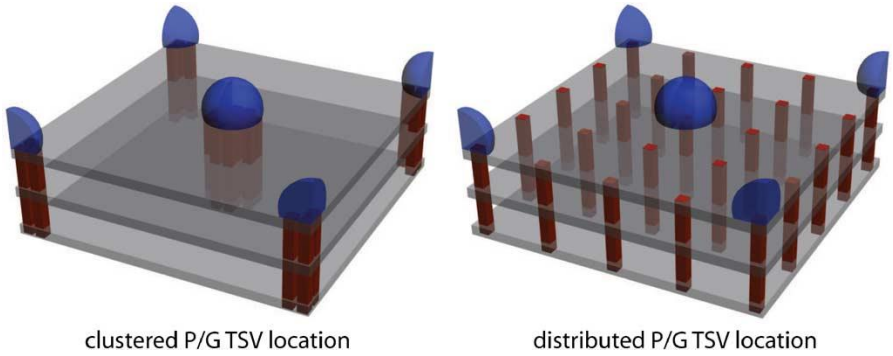
Power Delivery and Thermal Management

- For *d* dies, approx. *d*-fold power density than 2D chips
  - Large current to be delivered without excessive noise
  - Large heat to be dissipated

- Arrangement of TSVs
  - Distribute PG TSVs
  - Align TSVs for better heat dissipation



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- Dedicated 3D PDNs
  - Synchronize synthesis of PG grids among all dies

- Low-power, thermal-aware design

- Technological measures: decap dies, multiple power supplies, microfluidic channels, etc.

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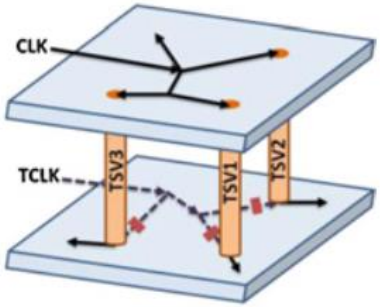
Clock Delivery

- Reliable, uniform and high-speed delivery across multiple dies

- Redundant and/or array arrangement of clock TSVs



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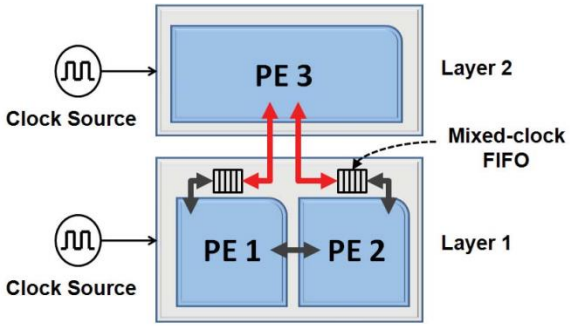
- Multiple clock domains
  - Mitigate inter-die variations
  - Enable testability



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- Dedicated 3D clock-network synthesis
  - Account for vertical interconnects' impact on timing (variations)
  - 3D extension of effective techniques such as MMM and DME

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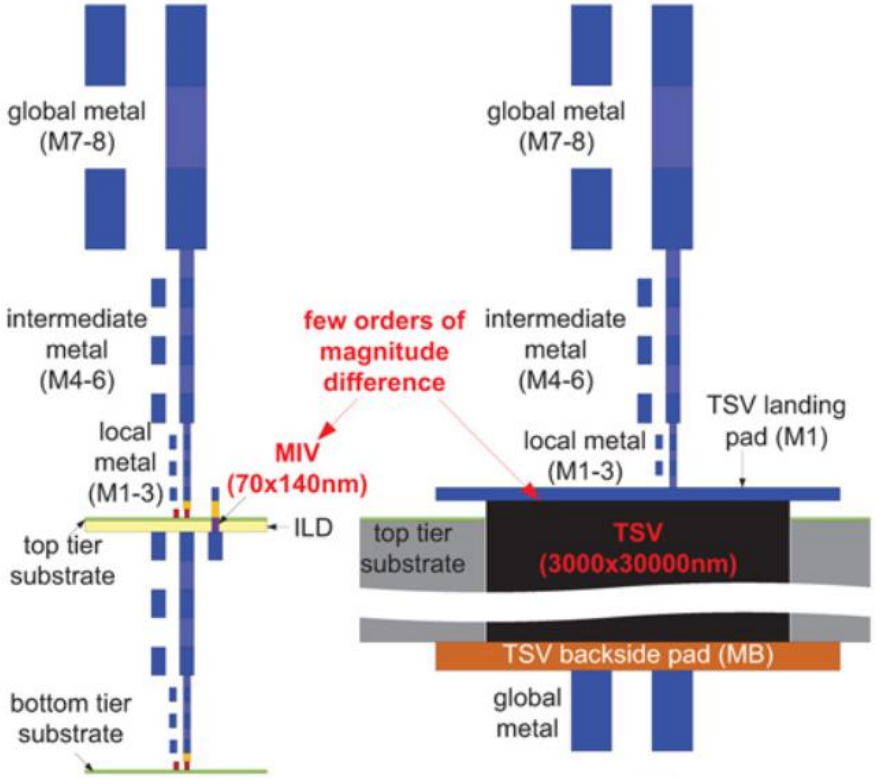
Partitioning and Floorplanning

- Traditional 2D metrics not sufficient

- Technology-aware partitioning; not min-cut



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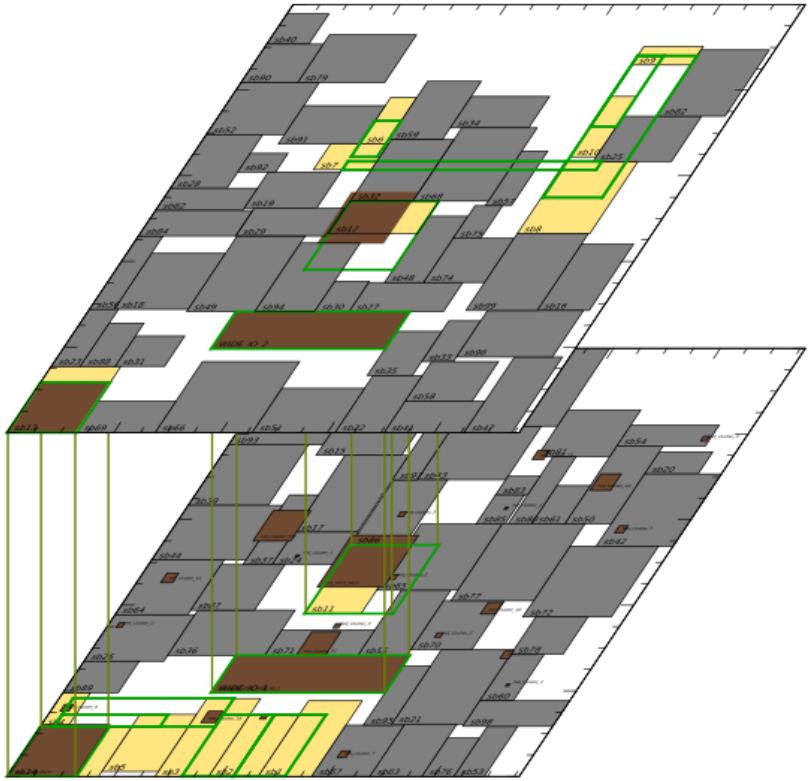
- Technology-aware partitioning; not min-cut
- Multi-objective floorplanning
  - Thermal management
  - Stress management
  - PDN-noise management
  - Interconnects-aware timing
  - Co-arrangement of modules and global interconnects
- Fast, holistic and accurate design evaluation



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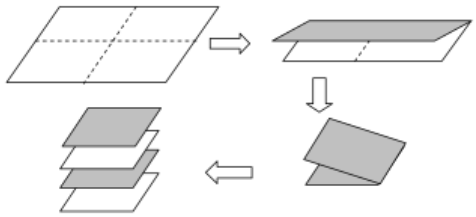
Placement

- Placement throughout the 3D domain is complex

- Folding-based placement
  - Practical for monolithic ICs



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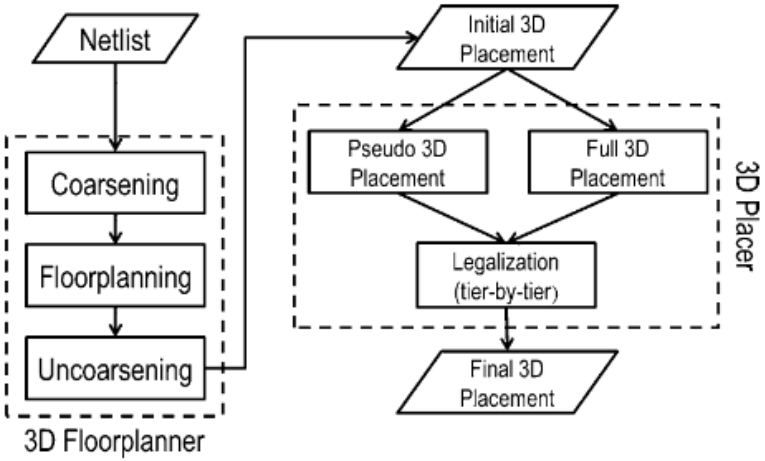
- Analytic placement
  - Solving systems of equations either for 2.5D or 3D domain
  - Complex; requires clustering and coarsening, global smoothing, etc.

- Hierarchical placement
  - A framework for GP, DP, legalization
  - Not restrictive; analytical placer etc.
  - Co-placement of TSVs



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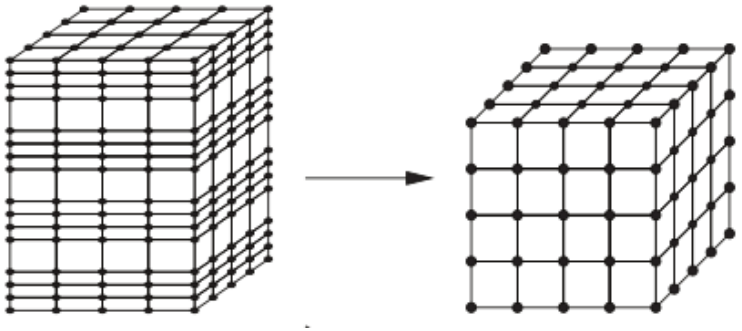
Routability Estimation and Routing

- Nets may span across multiple dies; heterogeneous topologies

- Analytic and heuristic estimation
  - Extended HPWL and routing graphs
  - Interconnects models, with TSV parameters, buffer emulation etc.
  - Probabilistic models, used for routability-driven paritioning or placement



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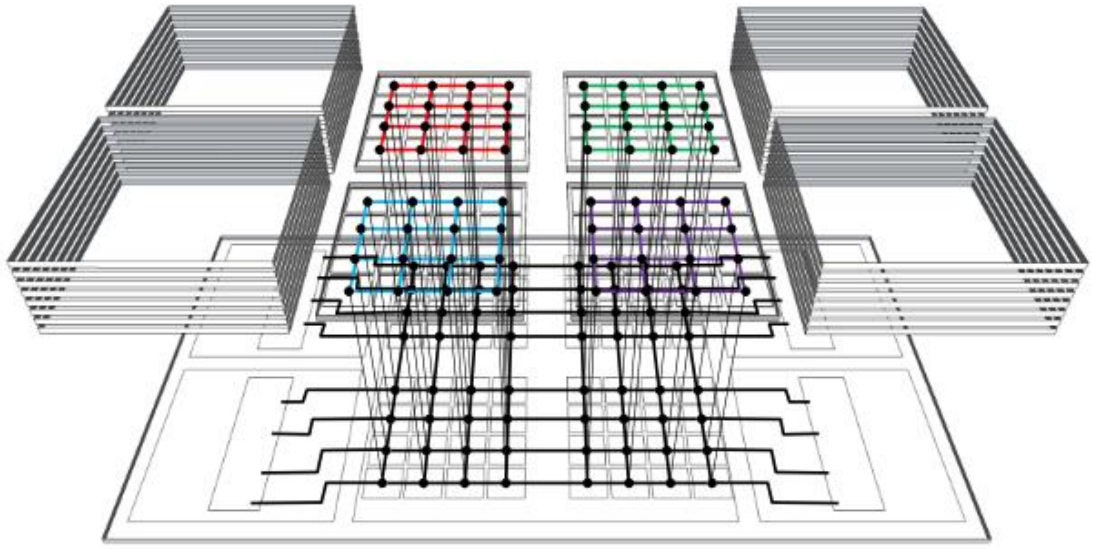
Routability Estimation and Routing

- Nets may span across multiple dies; heterogeneous topologies

- Global routing
  - TSV-based 3D ICs: 3D Steiner trees, thermal analysis, (re)arrange TSVs
  - Interposer stacks: 3D NoC design; challenging for heterogeneous stacks



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  - TSV-based 3D ICs: 3D Steiner trees, thermal analysis, (re)arrange TSVs
  - Interposer stacks: 3D NoC design; challenging for heterogeneous stacks

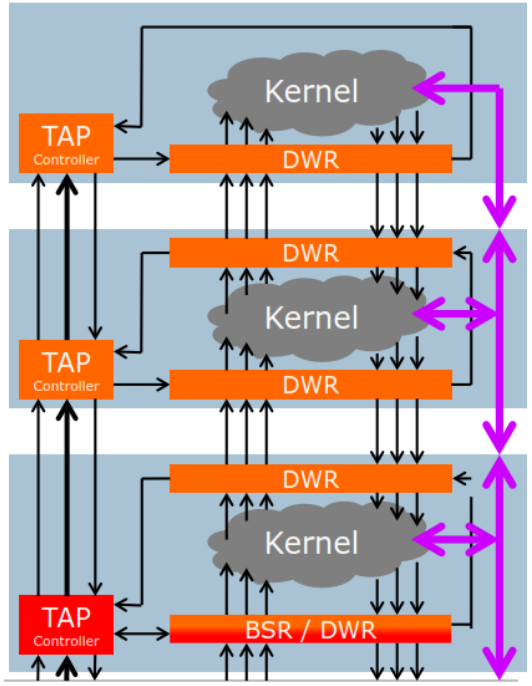
- Detailed routing: not fundamentally different once vertical and global interconnects are planned for

Testing

- Multiple testing requirements; pre-bond and post-bond testing

- Tailored fault models and at-speed testing, e.g., ATPG considering TSV-induced thermo-mechanical stress

- Standard for testing architecture: IEEE P1838
  - Test access based on IEEE 1149.1
  - Die wrapper register like IEEE 1500
  - Internal debugging via IEEE P1687



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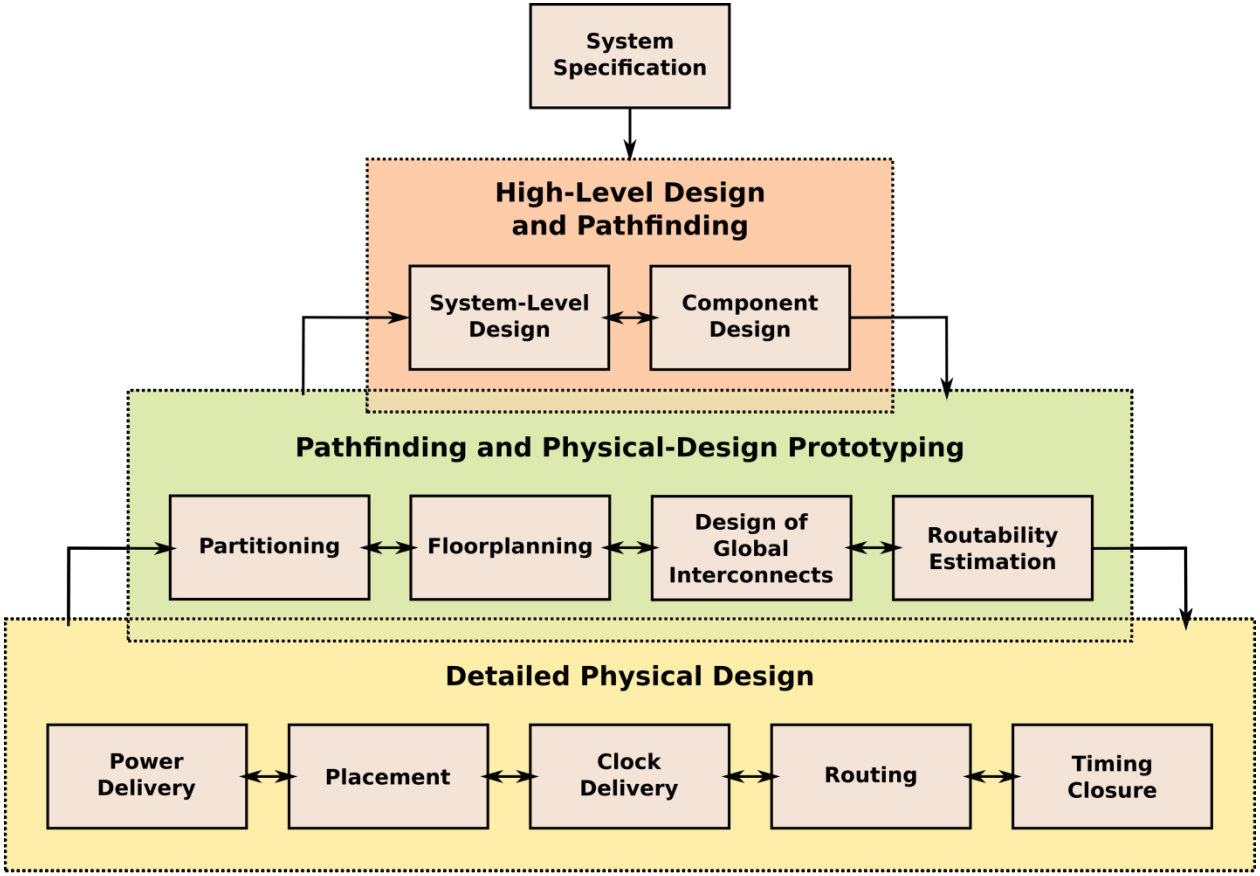
1. Derive components from high-level descriptions
2. Prototyping: generate and evaluate "coarse" layouts



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High-Level PD: Pathfinding and Chip-Package Co-Design

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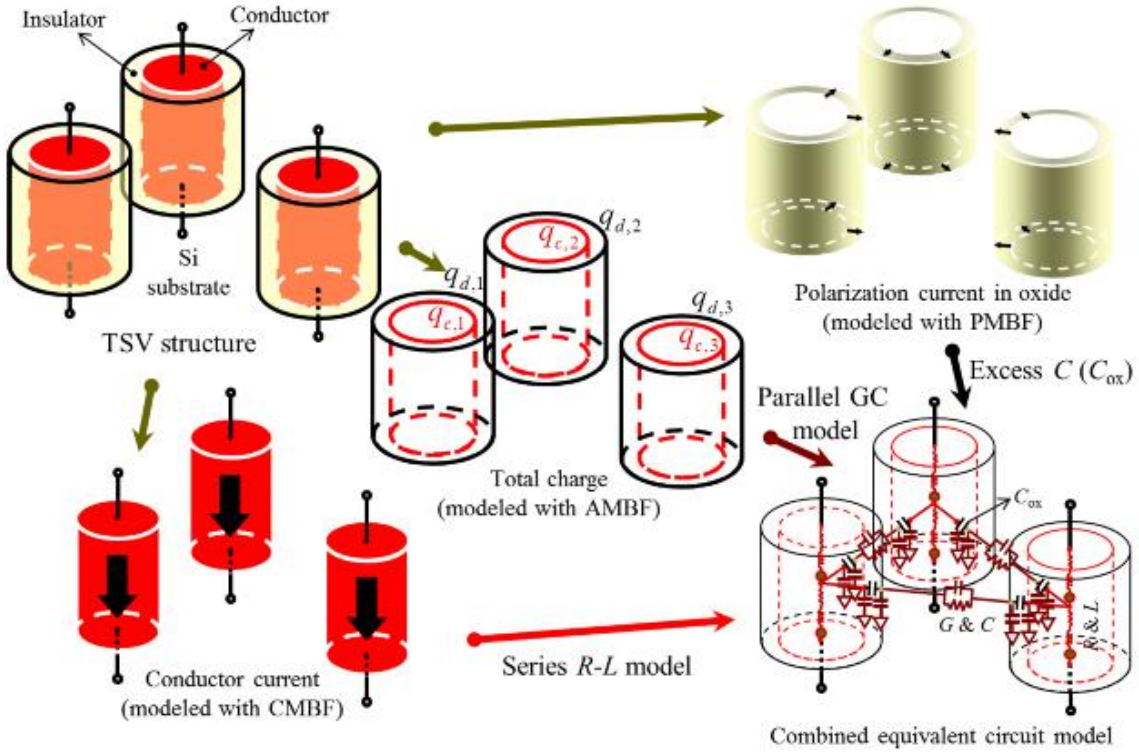
   - Abstracted, modular components, e.g., RTL modules
   - Parameterizable multi-port components for TSVs, bumps, etc.



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   - Abstracted, modular components, e.g., RTL modules
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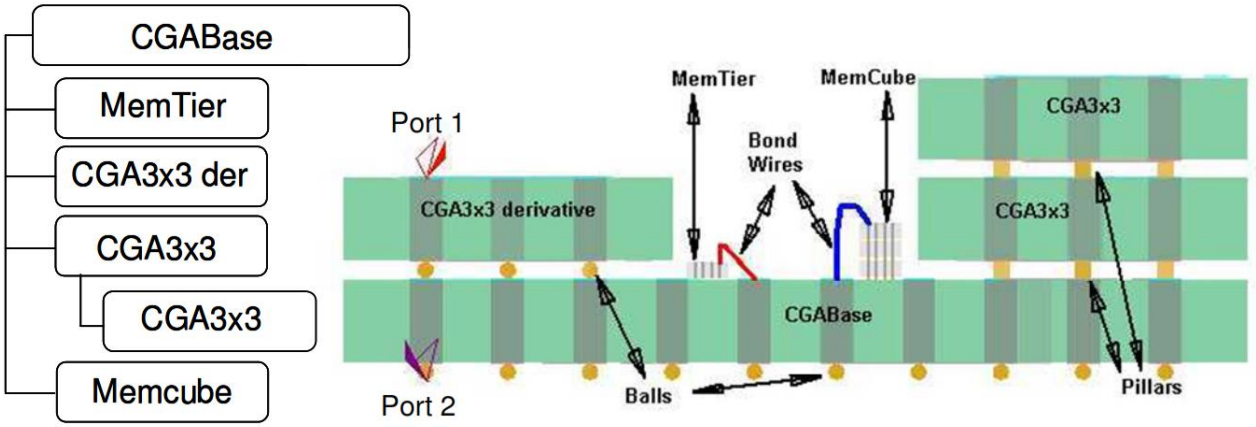
2. Prototyping: generate and evaluate "coarse" layouts
   - Explore different stacking and technology options
   - Annotate stack and modules with simulation feedback; management of multi-physical effects



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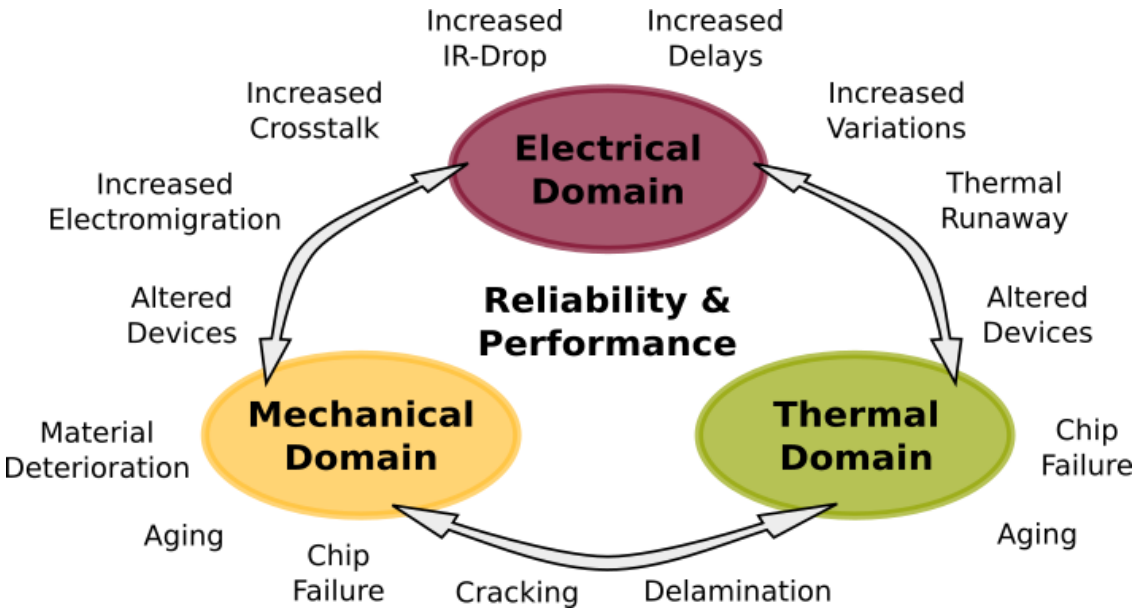
Multi-Physics Simulation

- Strong coupling of physical domains in 3D stacks



- Scalable simulation techniques, linking across different design levels

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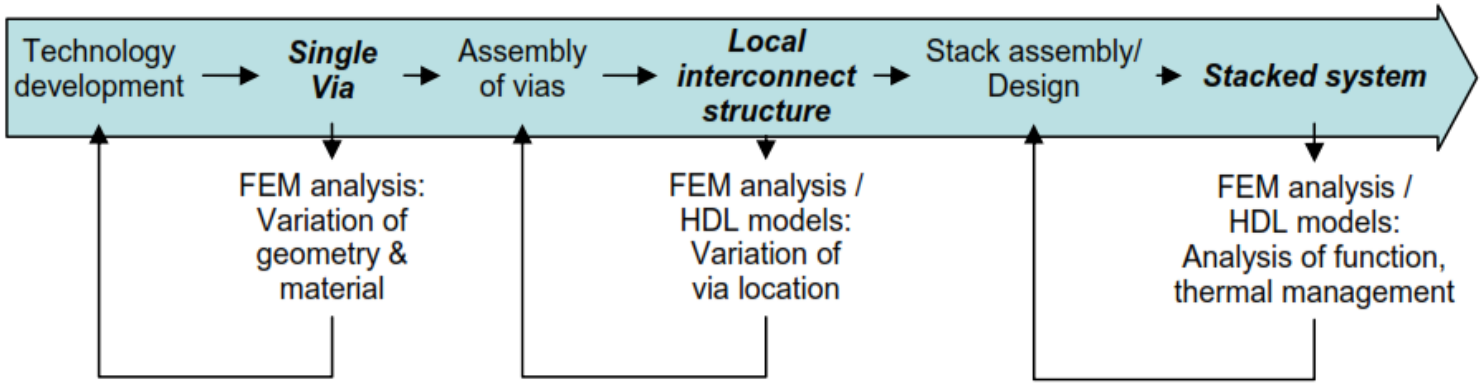

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- Scalable simulation techniques, linking across different design levels
  - From fine-grain to abstracted, high level simulation
  - Model generation, network simulation, superposition etc

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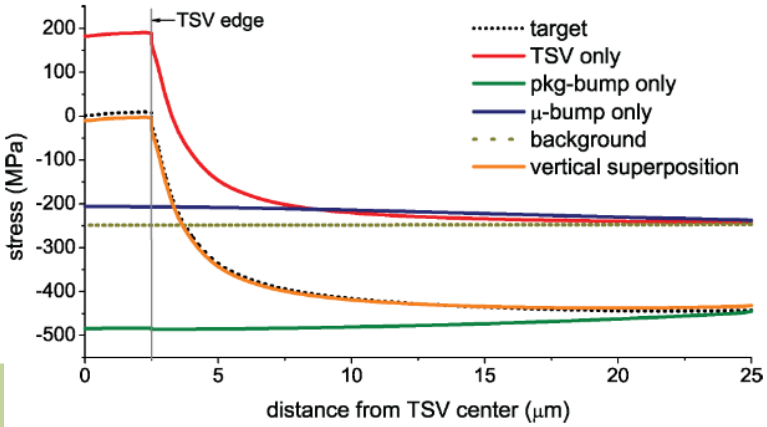

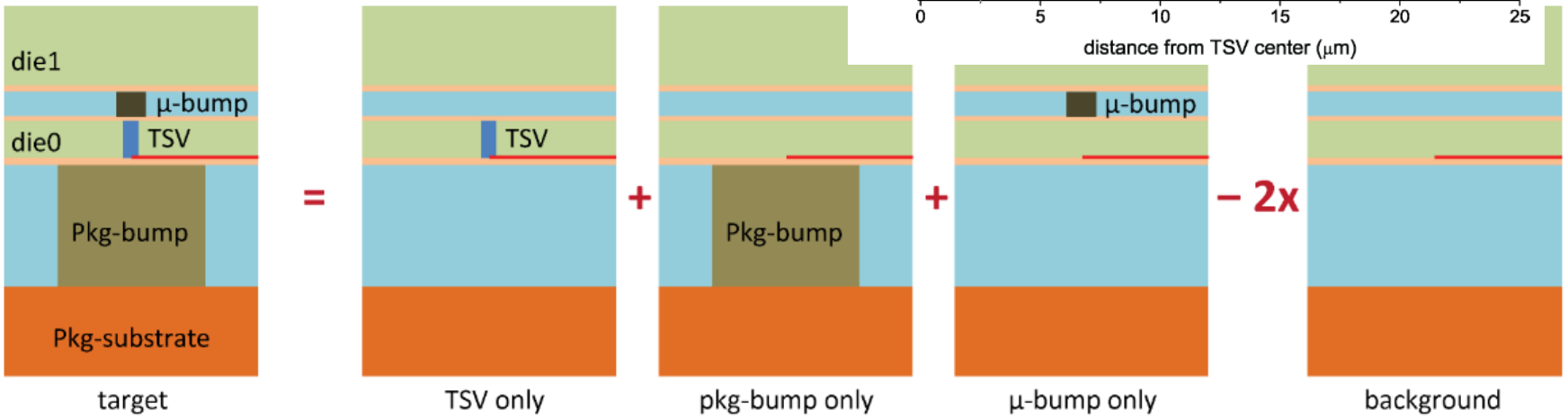

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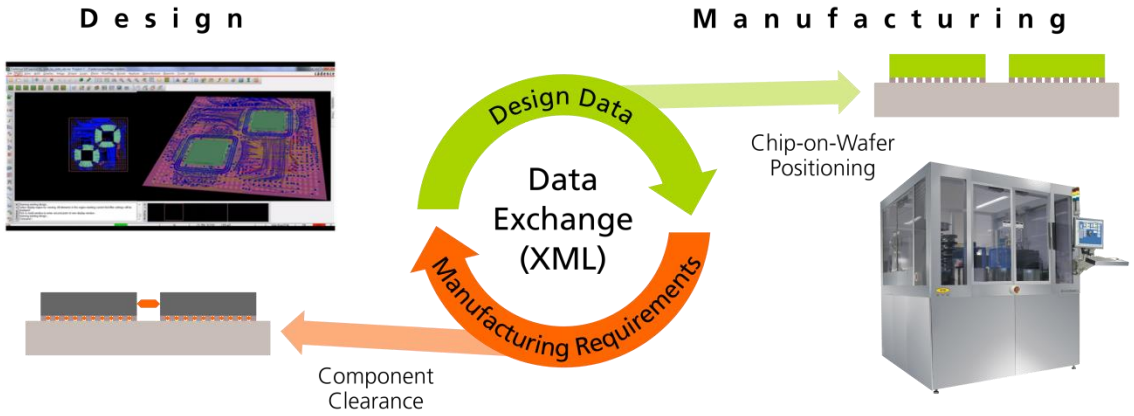
Design Standards and File Formats

- Lack of standards and file formats for data exchange hinder commercial adoption

- Multiple standards for memory integration; mass production of memory stacks
  - Wide I/O, High Bandwidth Memory (HBM), Hybrid Memory Cube (HMC)

- Assembly design kit (ADK)
  - Exchange of design data, manufacturing steps, material properties etc.
  - Streamlining interaction of tools and verification for whole stack



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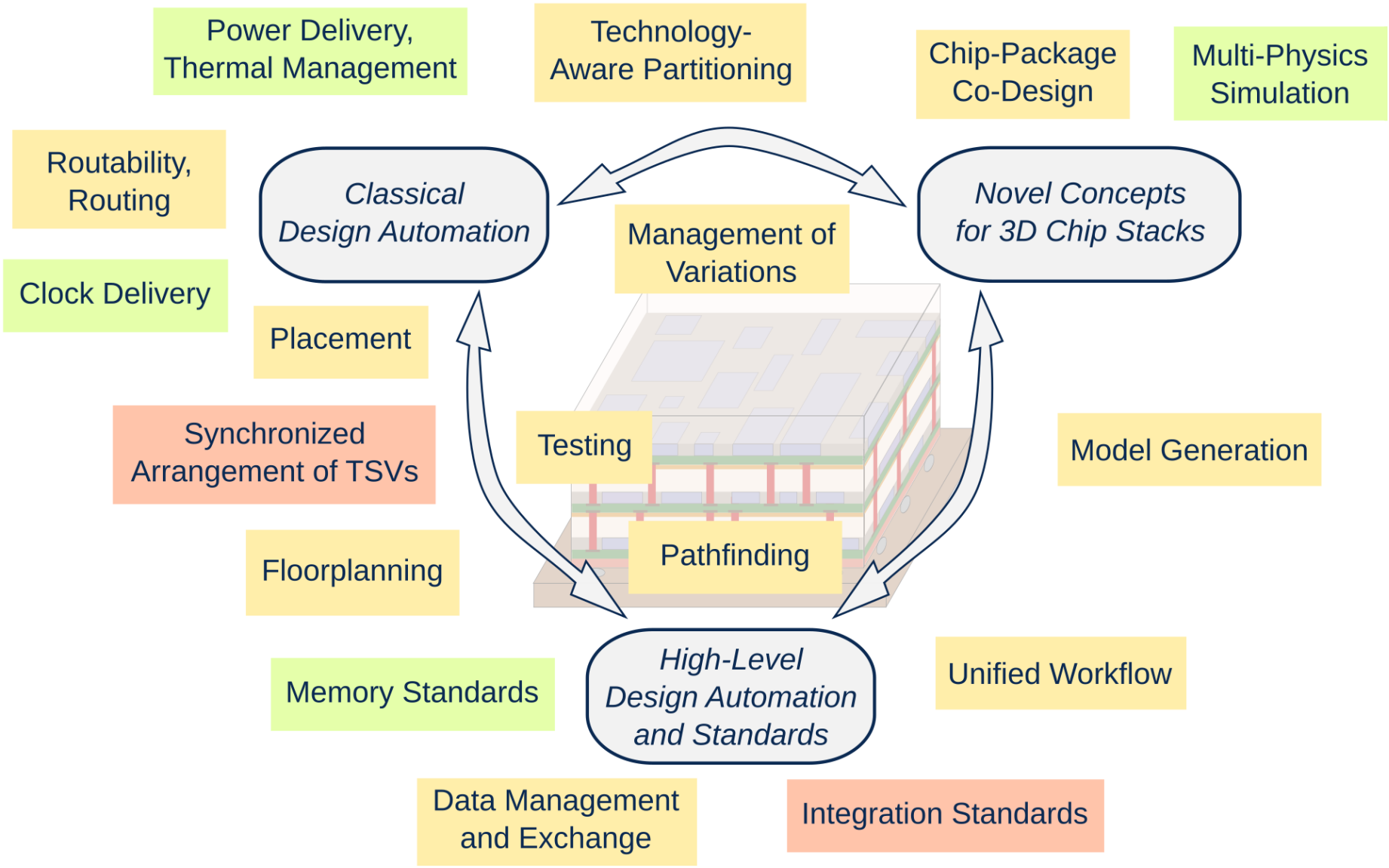

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- Comprehensive overview, more than 100 references
- http://dx.doi.org/10.1145/2872334.2872335