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Design Automation for 3D Chip Stacks: Challenges and Solutions

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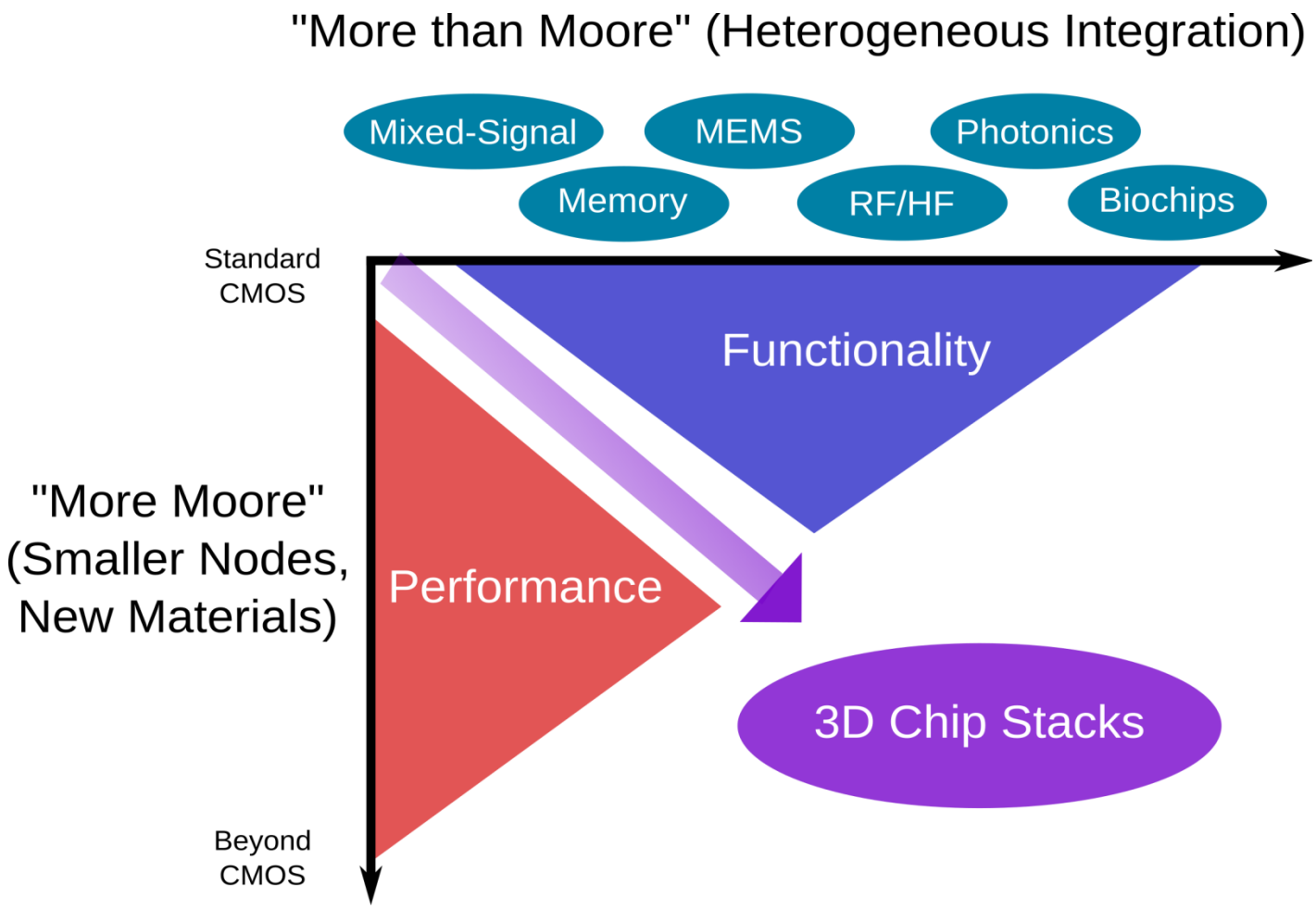
Tutorial (Part 1/2) at
ICCD 2016, October 2nd

Access Slides: tiny.cc/ICCD16-3D

Outline

1. Motivation, Flavors, and Examples of 3D Chip Stacks
2. Classical Challenges – Aggravated but Solvable
3. Novel Design Challenges and Emerging Solutions
4. Summary Part 1 and Introduction Part 2

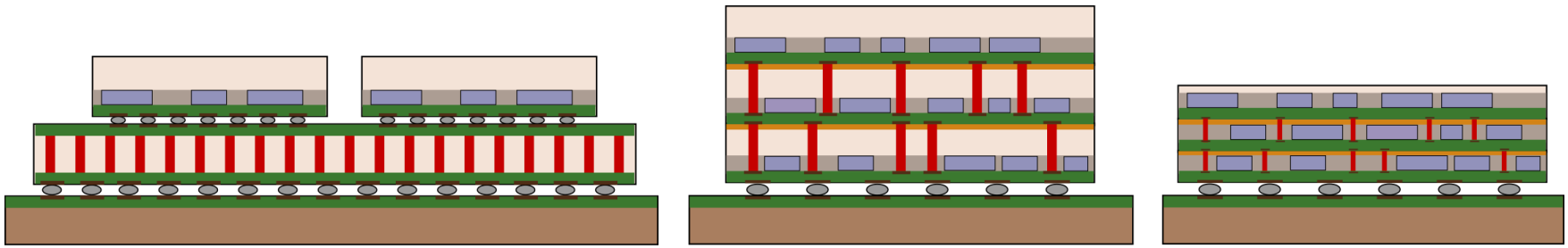
3D Chip Stacks: Meeting Trends for Modern Chip Design



Principles of 3D Chip Stacks

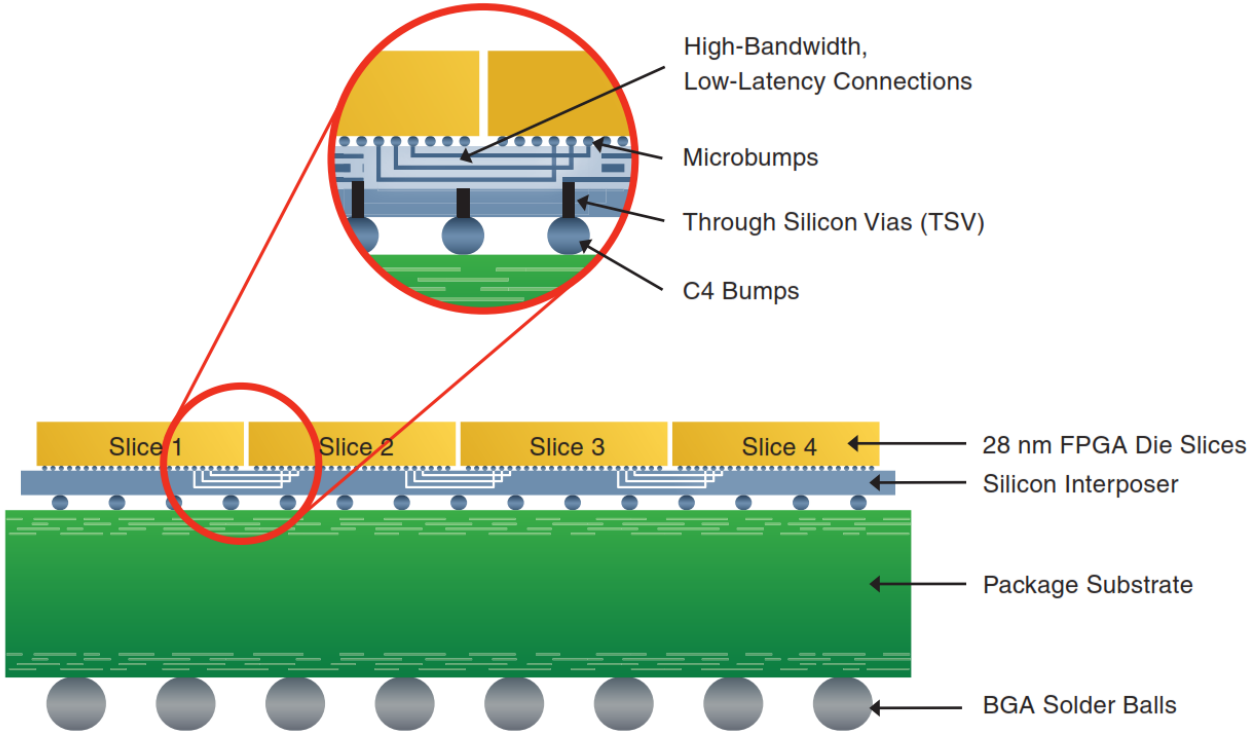
- Multiple vertically stacked active layers (dies)
  - ⊕ Shorter and vertical interconnects: power consumption, delay, bandwidth
  - ⊕ Separate and smaller dies: heterogeneous integration, yield, cost, size
  - ⚠ Complex design, design automation, and manufacturing processes

- Different options; focus on three most important options



Interposer Stacks

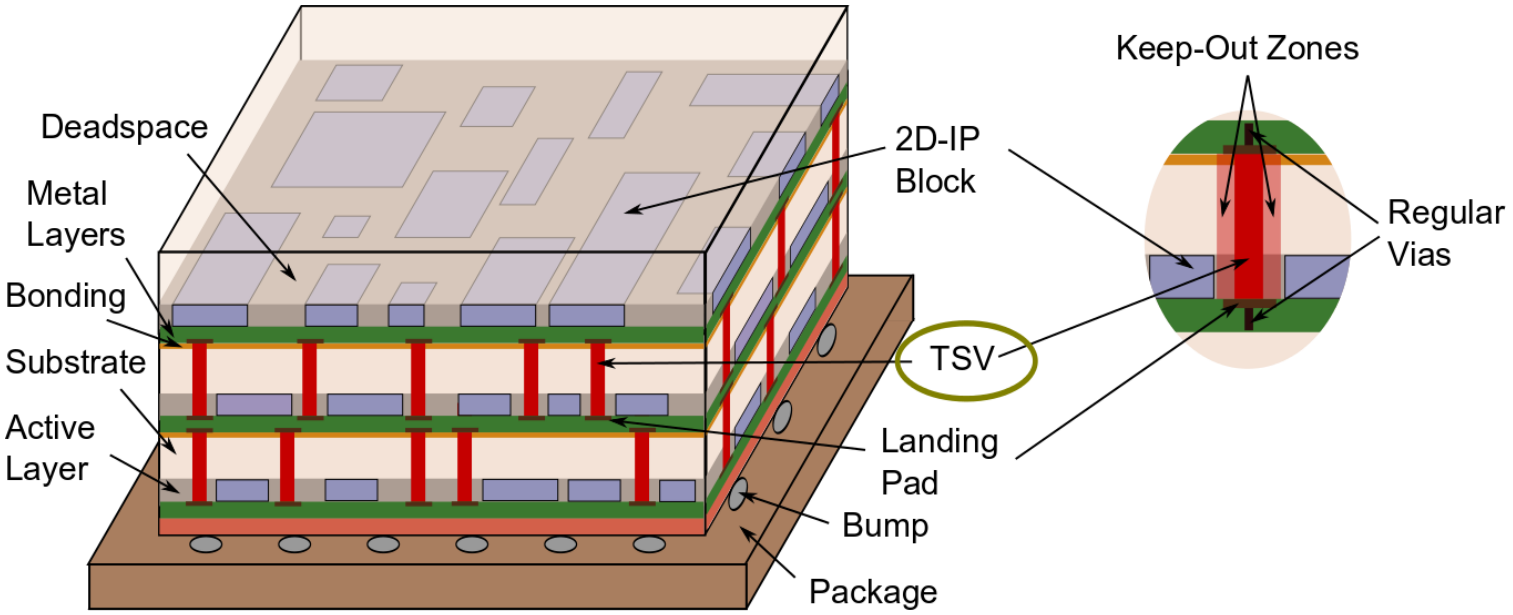
- Chip-level integration
- Interposer as (Si) carrier with regular metal layers
- Mainly lateral stacking; “2.5D integration”
- Packaging-centric manufacturing; good acceptance in industry



Dorsey, P. Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency Xilinc, Inc., 2010

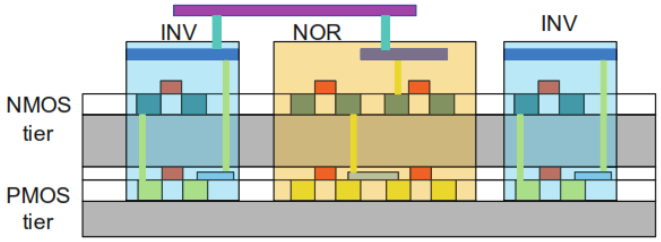
TSV-based 3D ICs

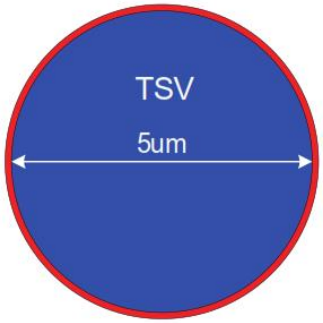
- Block-level integration
- Through-Silicon Vias (TSVs): vertical metal plugs for electrical inter-chip connections
- Die manufacturing and die stacking can be separated

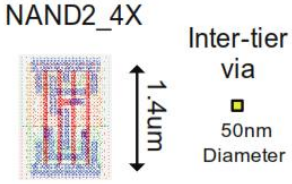


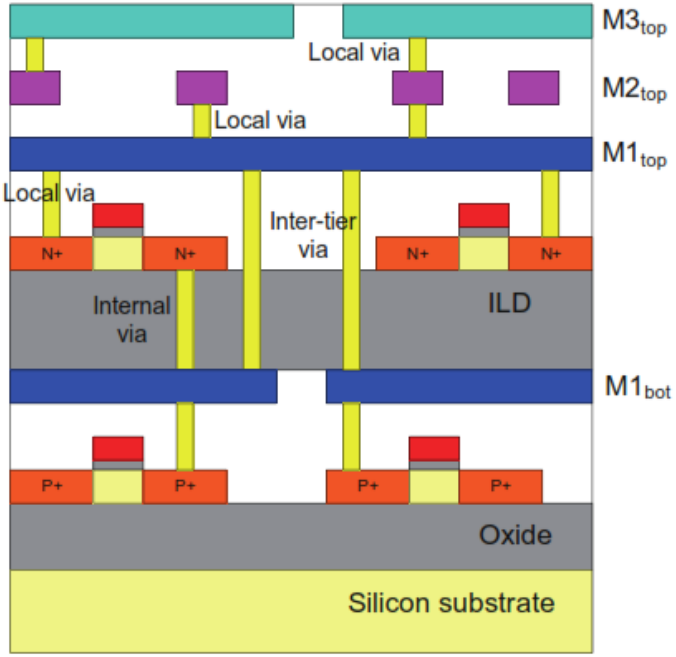
Monolithic 3D ICs

- Transistor-level, fine-grain integration
- Inter-layer vias like regular vias
- Dedicated sequential manufacturing process



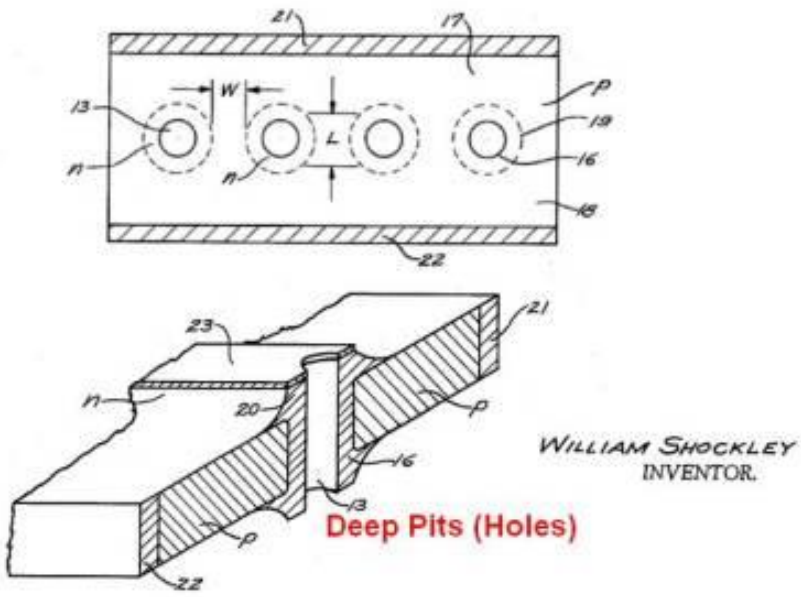




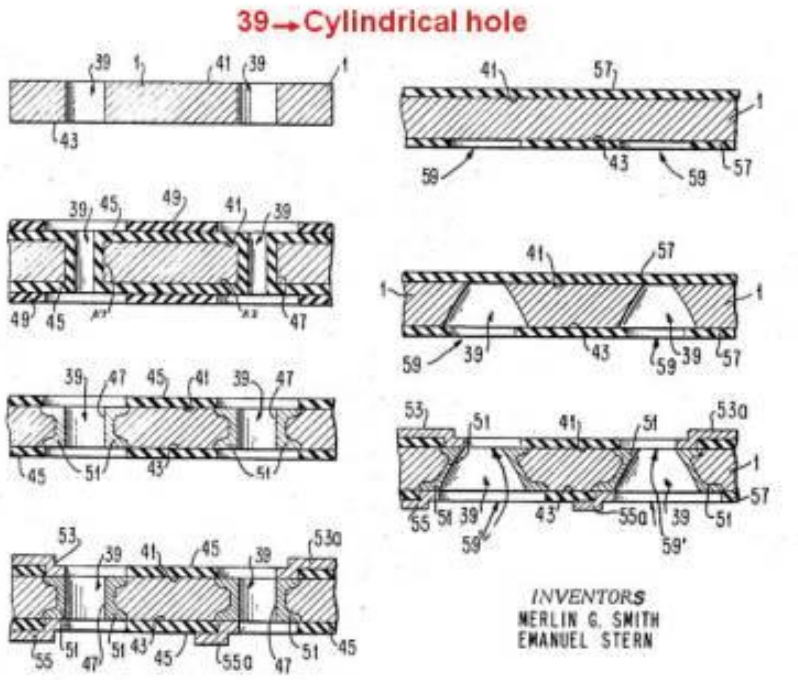


Liu, C. & Lim, S. K. A Design Tradeoff Study with Monolithic 3D Integration
Proc. Int. Symp. Quality Elec. Des., 2012

Very Early Foundations for TSVs (1950s,60s)



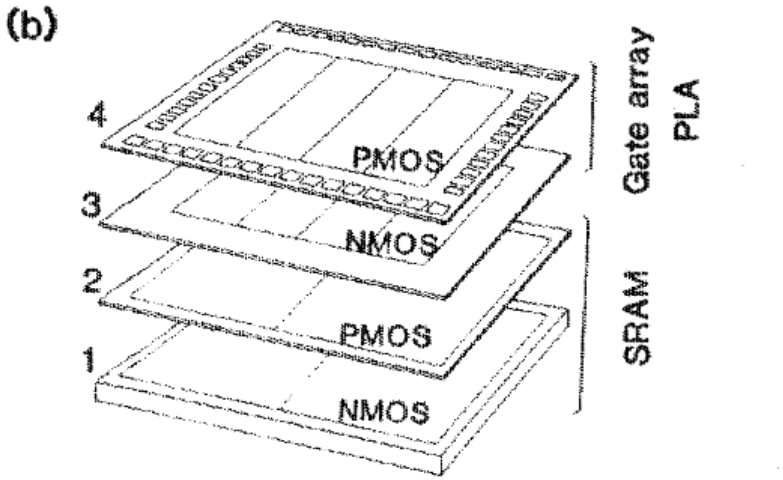
William Shockley, "Semiconductive Wafer and Method of Making the Same", US Patent # 3,044,909, filed on October 23, 1958 and granted on July 17, 1962.



Merlin Smith and Emanuel Stern, "Methods of Making Thru-Connections in Semiconductor Wafers", US Patent # 3,343,256, filed on December 28, 1964 and granted on September 26, 1967.

Early 3D ICs (1989)

- Very same motivation like today
  - Heterogeneous integration (for process optimization)
  - Shorter interconnects



Kunio, T., et al. "Three dimensional ICs, having four stacked active device layers." Electron Devices Meeting, 1989. IEDM'89. Technical Digest., International. IEEE, 1989. Authors with NEC Corp.

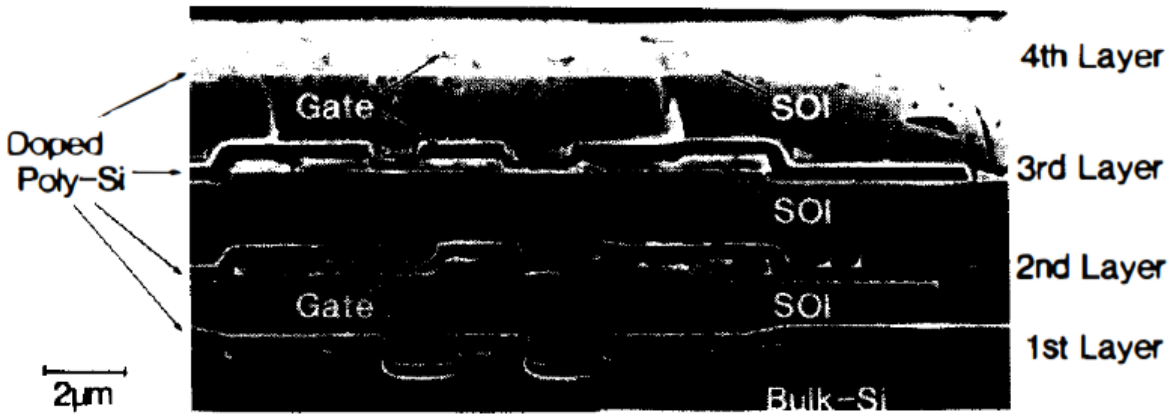
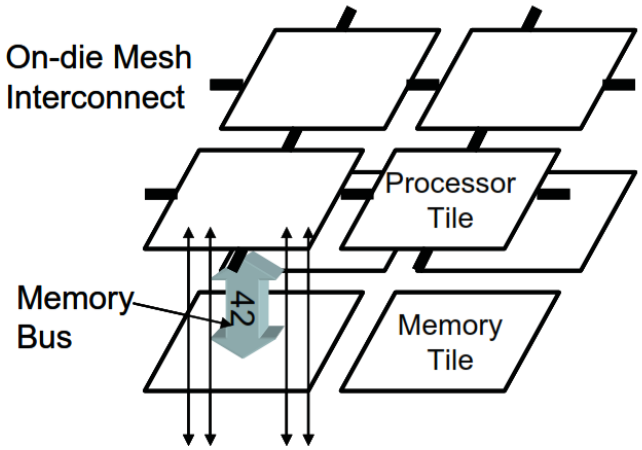


Fig.7 Cross-sectional SEM photograph of a four-layer-stacked 3D-IC, including doped poly-Si.

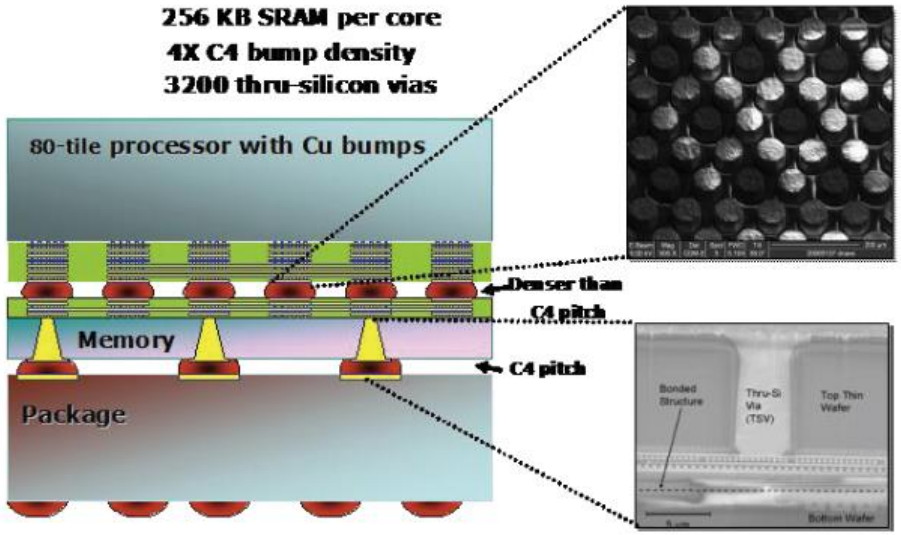
Prototypes of TSV-based 3D ICs: Memory on Logic

- Teraflops Research Chip, Intel, 2007
  - 80 cores, stacked SRAM on top
  - 1 TB/s memory bandwidth; approx. 100x better power-performance figure (here 2.2W; traditional bus: 20W for 100GB/s)

- Tile-based architecture; simplified (full-custom) design process



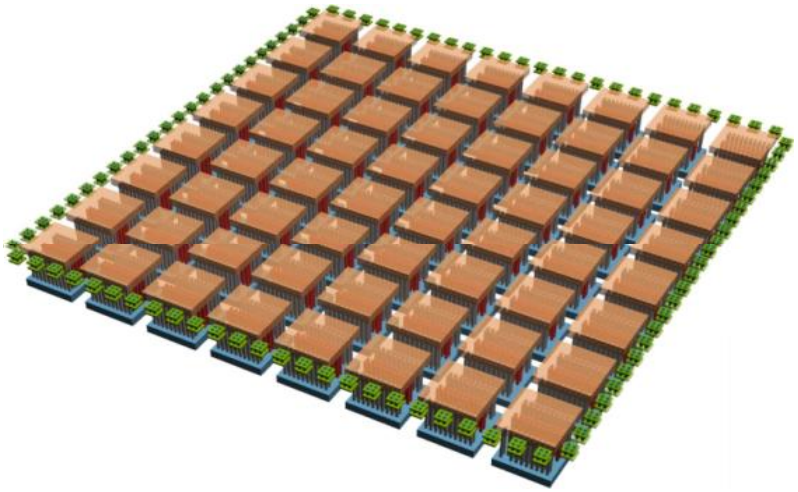
Borkar, S. 3D Integration for Energy Efficient System Design Proc. Des. Autom. Conf., 2011, 214-219

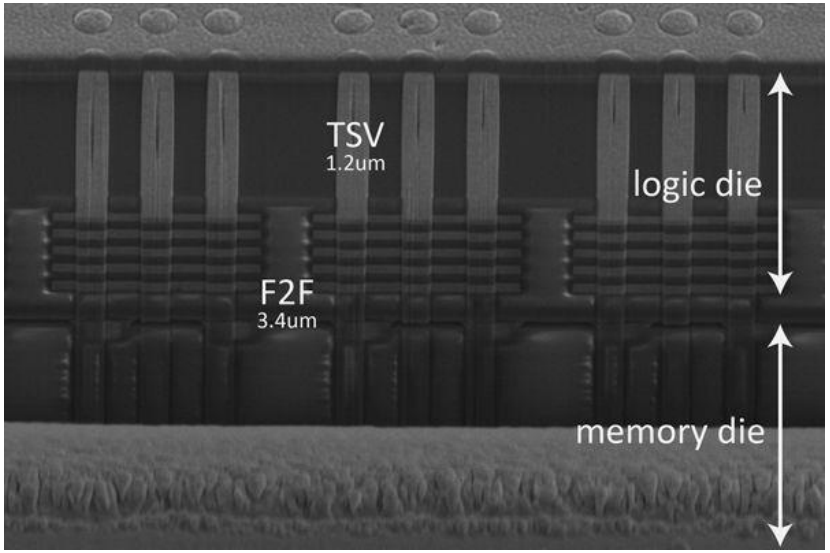


Prototypes of TSV-based 3D ICs: Memory on Logic

- 3D-MAPS, Georgia Tech, 2010 onwards
  - 64-128 cores, 1-2 logic dies, 1-3 memory dies
  - Up to 64 GB/s (2,5x Intel i7 & DDR3), at 4 W power consumption

- Tile-based architecture; 2D EDA flow with custom scripts and tools

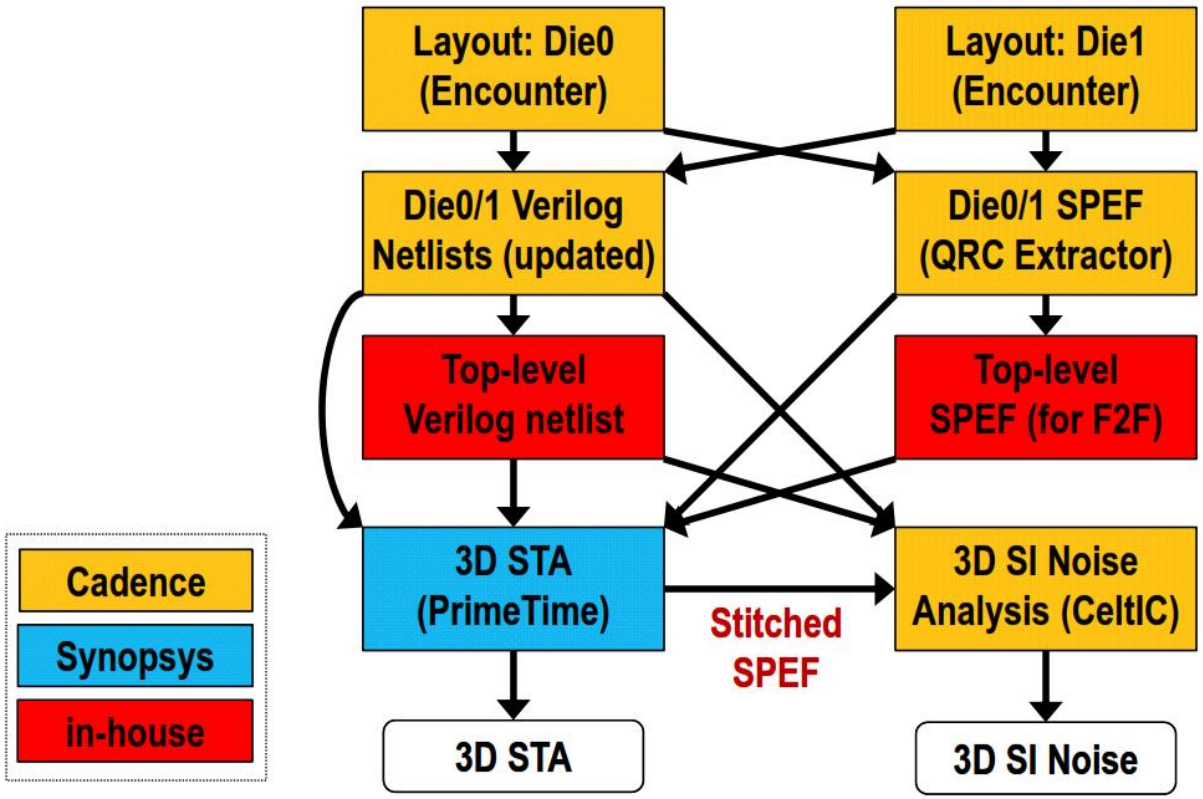




Kim et al. 3D-MAPS: 3D Massively Parallel Processor with Stacked Memory
Proc. Int. Solid-State Circ. Conf., 2012

Prototypes of TSV-based 3D ICs: Memory on Logic

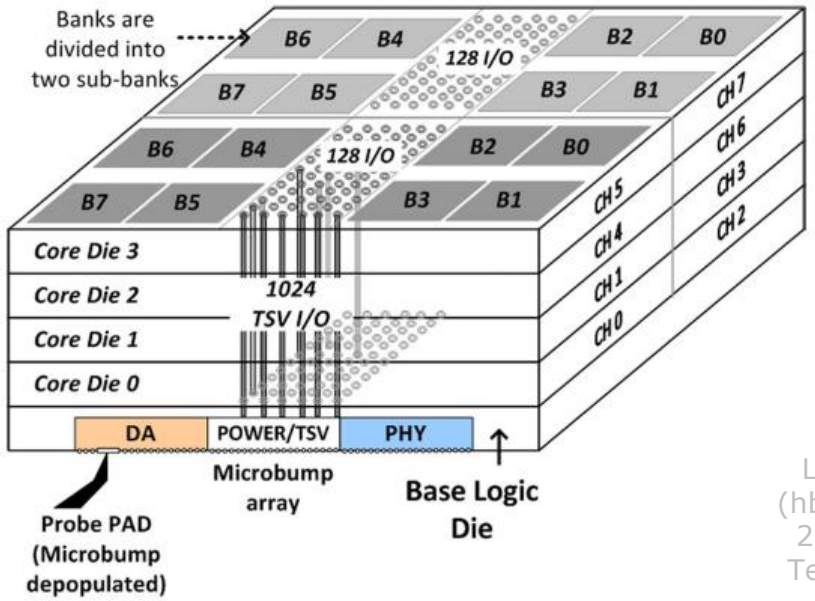
- 3D-MAPS, Georgia Tech, 2010 onwards
  - For example, flow for static timing analysis with signal integrity

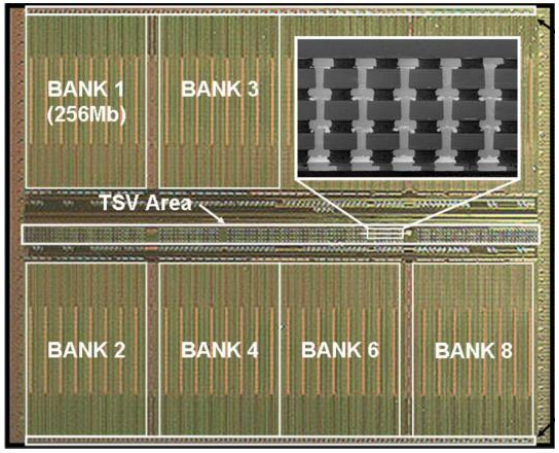


Kim et al. 3D-MAPS: 3D Massively Parallel Processor with Stacked Memory
Proc. Int. Solid-State Circ. Conf., 2012

First Commercial TSV-based 3D ICs: Memory Integration

- Hybrid Memory Cube (HMC), 2011 onwards
  - 128 GB/s; 15x DDR3 at 30% power of DDR3
- High Bandwidth Memory (HBM), 2011 onwards
  - JEDEC standard
  - HBM2: 256 GB/s
  - 2016: Samsung, mass production; SK Hynix, 4GB stacks in August

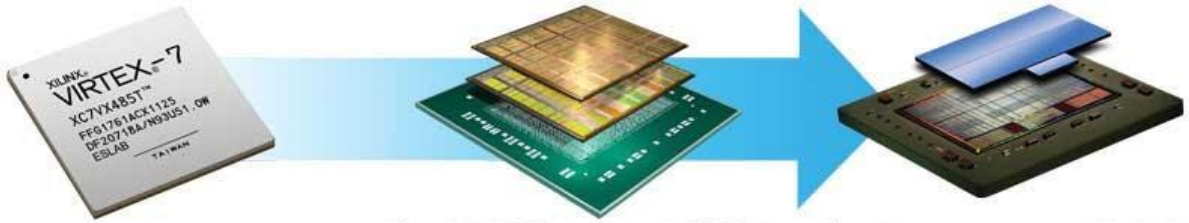




Lee et al. A 1.2 v 8gb 8-channel 128gb/s high-bandwidth memory (hbm) stacked dram with effective microbump i/o test methods using 29nm process and tsv. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, pages 432–433. IEEE, 2014.

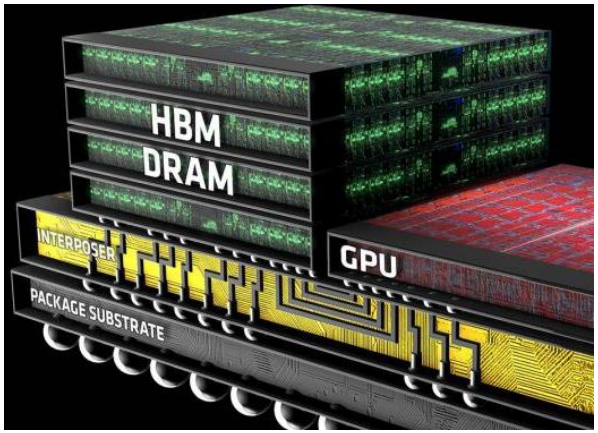
First Commercial Interposer Stacks

- Xilinx Virtex 7, 2011 onwards

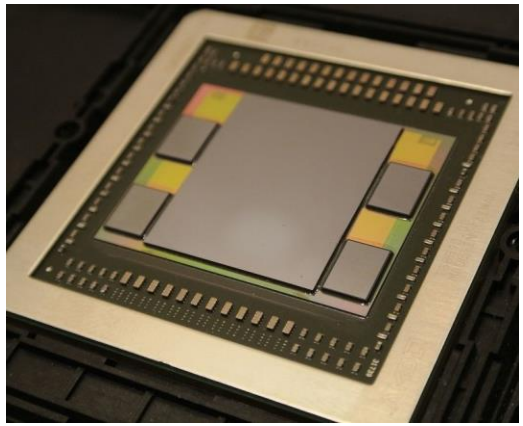


xilinx.com

- AMD Fiji, 2015: GPU, GPU, HBM on interposer
  - 8 years R&D; 20 partners; 15-16 prototypes
  - 8.9 billion transistors; 3x smaller PCB footprint



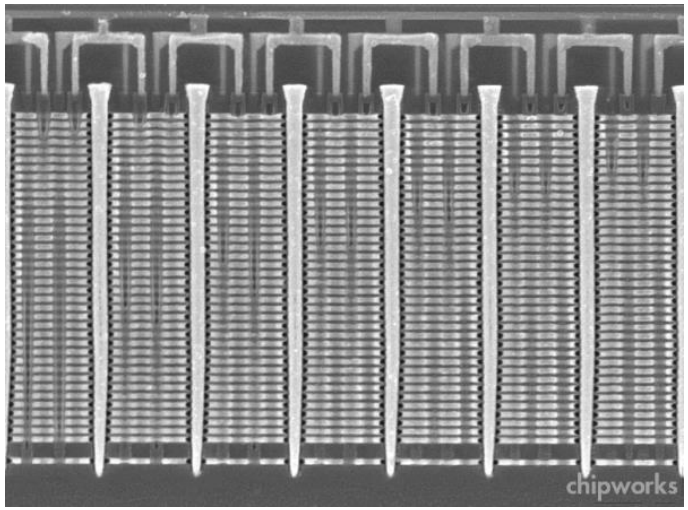
anandtech.com



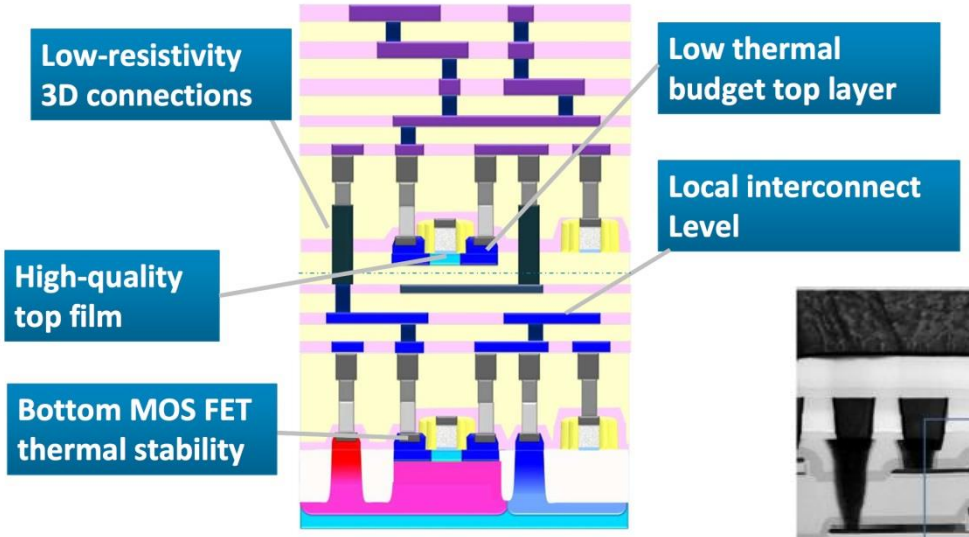
wikipedia.org

Monolithic 3D ICs: Progress for Technology

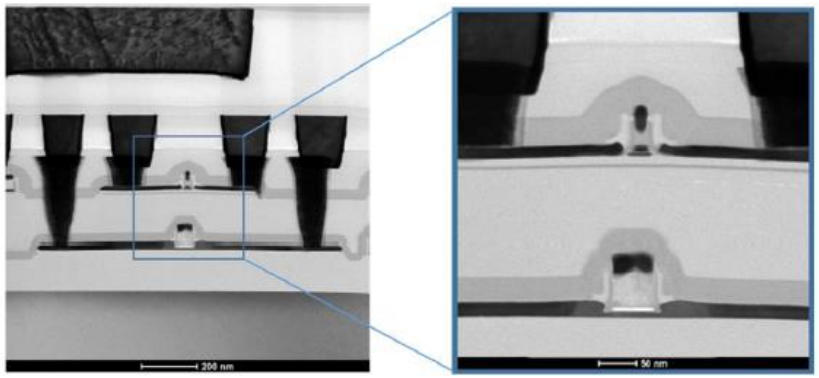
- V-NAND, Samsung and others, since 2012
  - Probably in 256GB iPhone 7
- CEA-Leti "CoolCube", since 2014
  - First demonstration of CMOS-over-CMOS 3D VLSI CoolCube integration on 300mm, 2016 VLSI Symposium



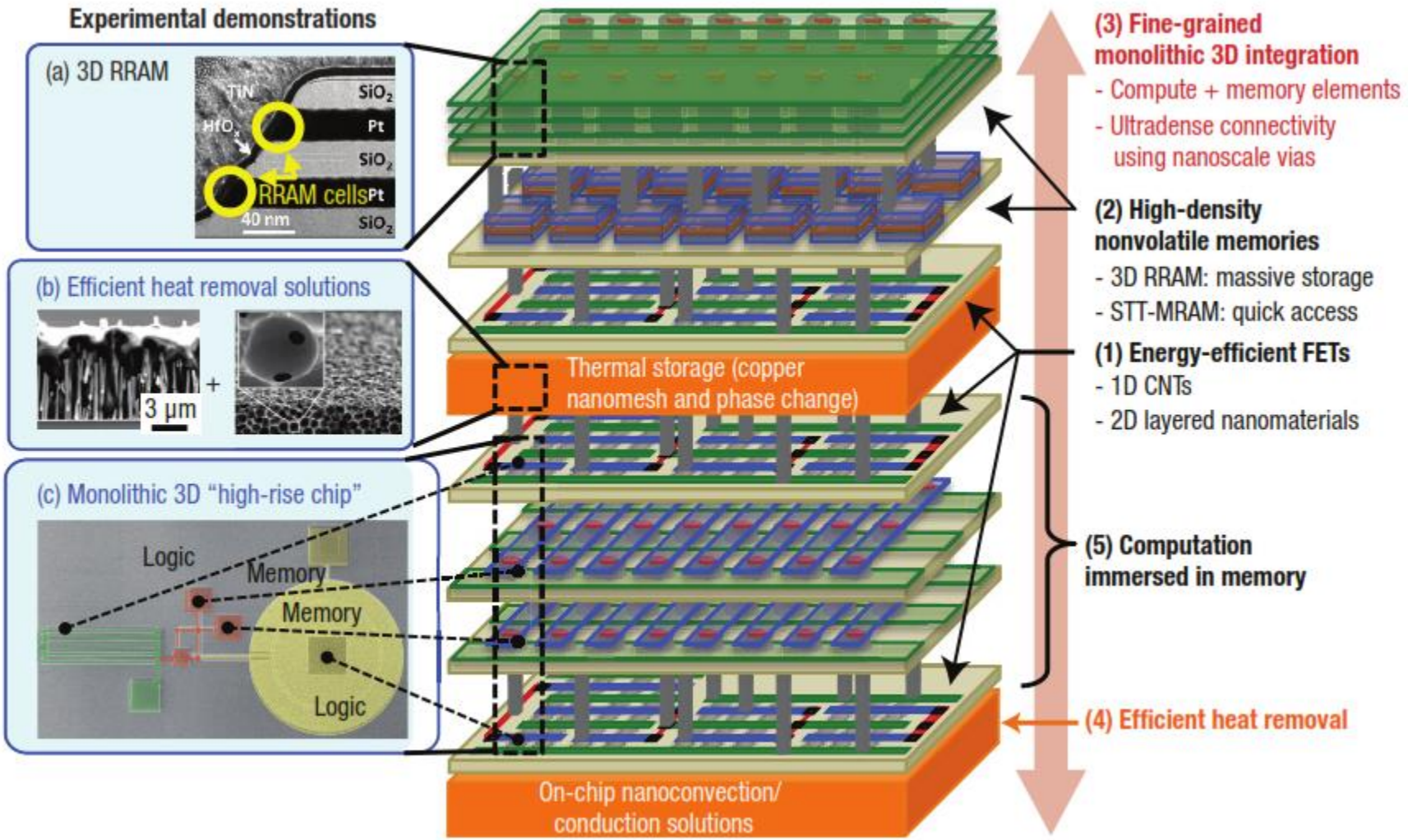
hardware.info



vlsisymposium.org

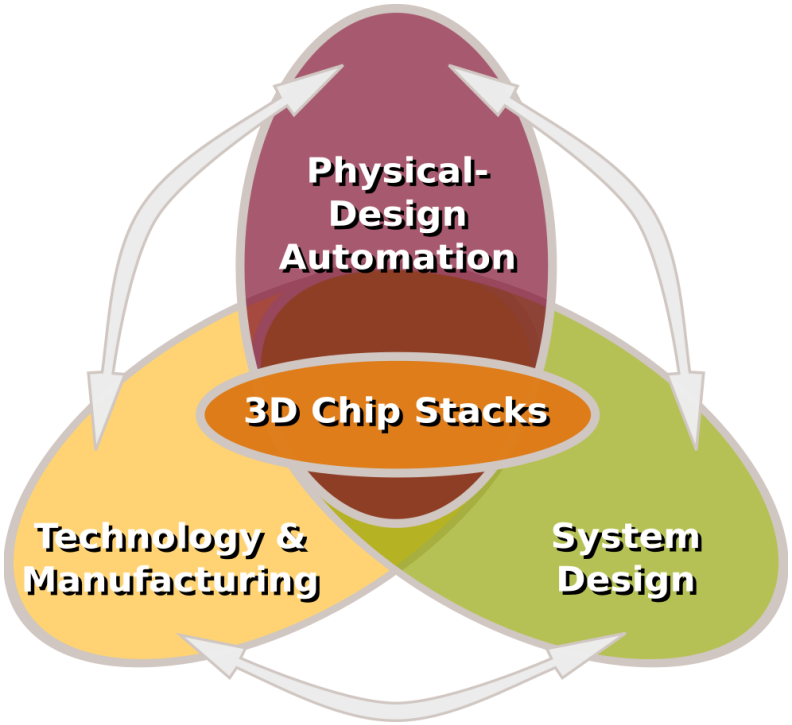


Monolithic 3D ICs: Towards Novel Computing Designs



Aly et al. Energy-Efficient Abundant-Data Computing: The N3XT 1,000x Trans. Comp., 2015, 48, 24-33

Design Automation as Key Enabler for 3D Chip Stacks



- Tutorial Part 1 (Johann Knechtel): classical and novel EDA challenges and solutions for 3D, logic integration
- Tutorial Part 2 (Ibrahim Elfadel): 3D in IoT sensors with focus on MEMS, imaging, memory and photonics

Outline

1. Motivation, Flavors, and Examples of 3D Chip Stacks
2. Classical Challenges – Aggravated but Solvable
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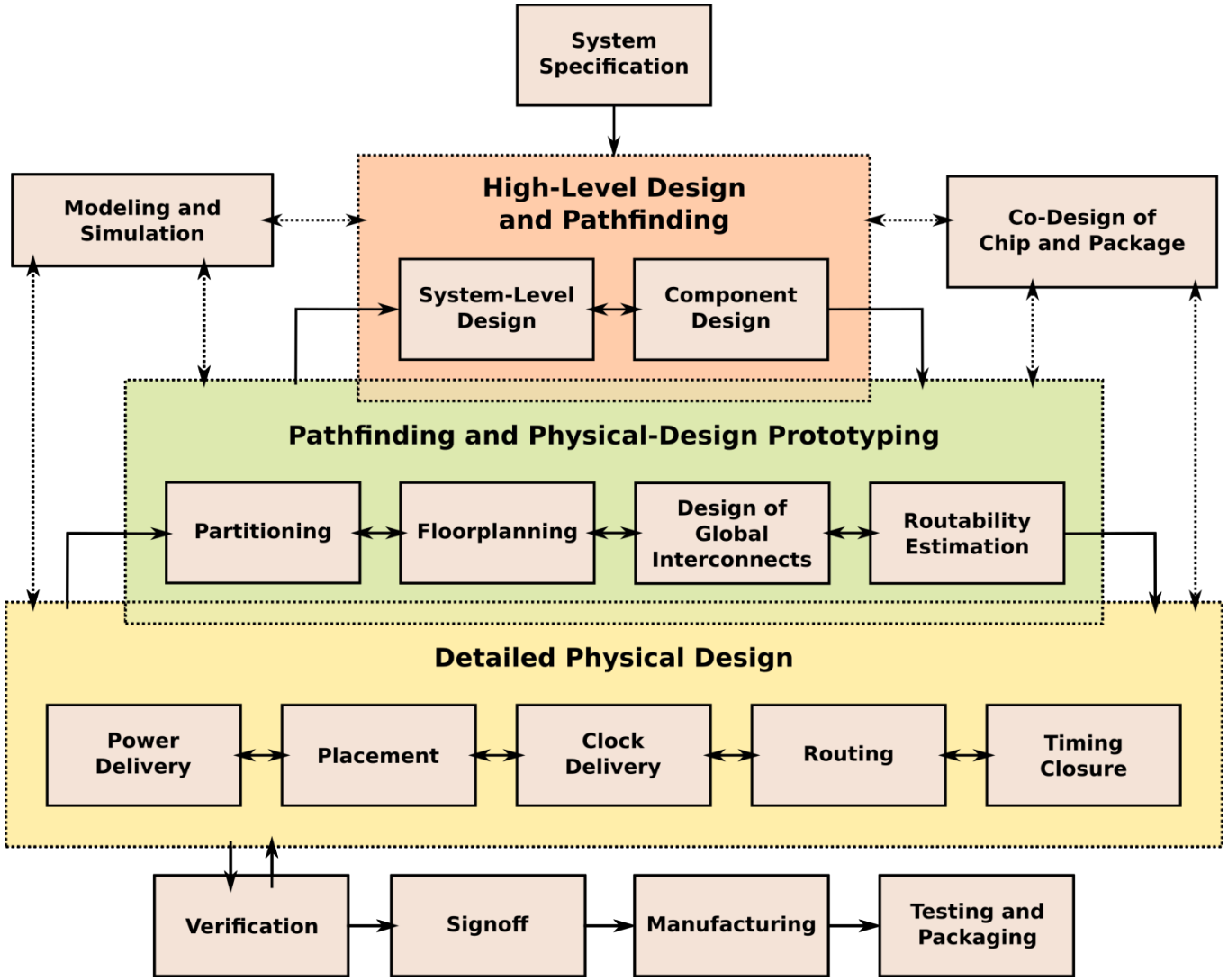
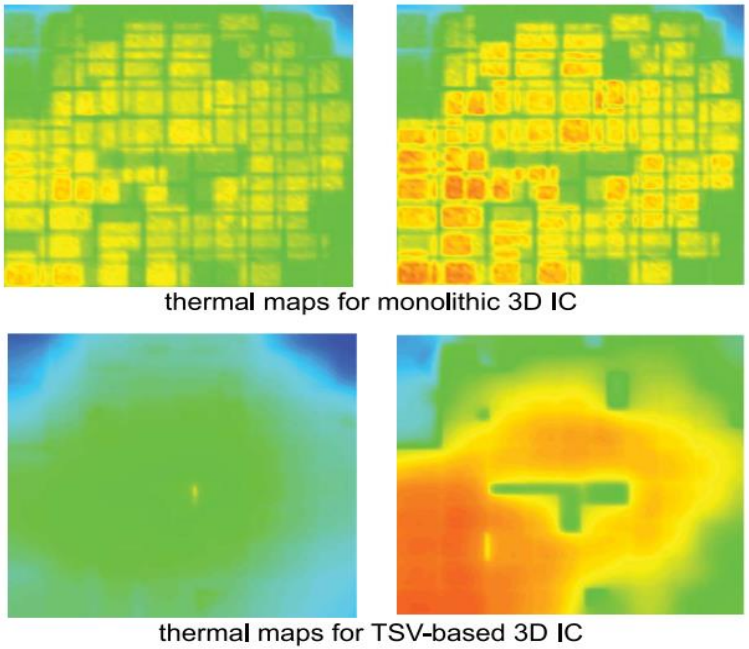
Design Automation Flow for 3D Chip Stacks

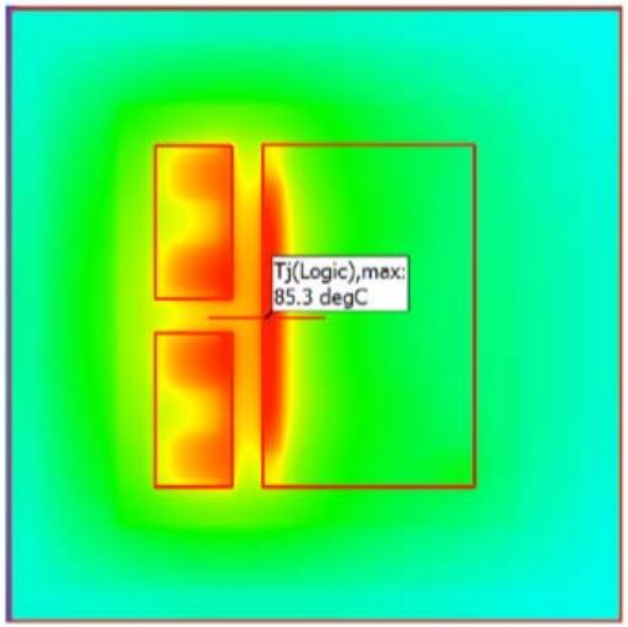


Thermal Modeling and Simulation

- For *d* dies, approx. *d*-fold power density than 2D chips
  - Large heat to be dissipated
  - Thermal profiles very different for various stacking scenarios
- Need for flexible and scalable modeling and simulation



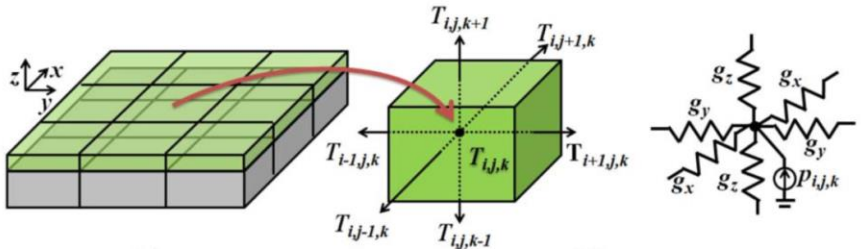
Samal et al. Adaptive Regression-Based Thermal Modeling and Optimization for Monolithic 3-D ICs Trans. Comp.-Aided Des. Integr. Circ. Sys., 2016, 35, 1707-1720



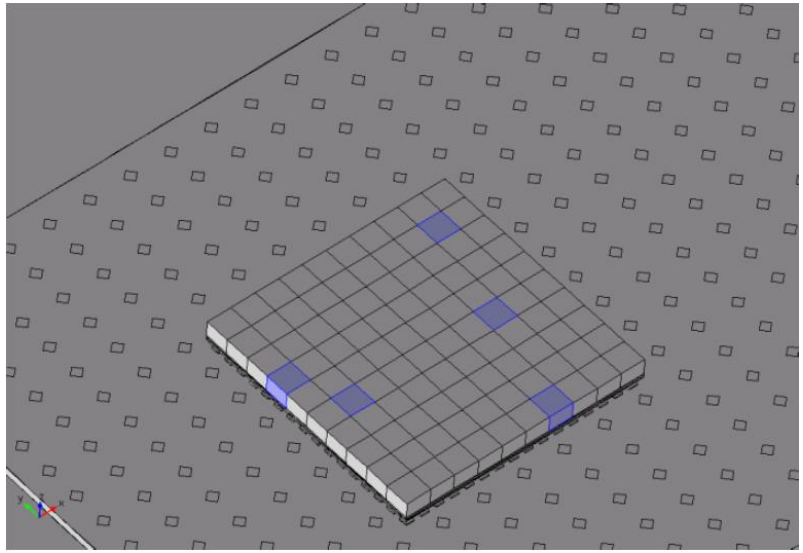
Iyer, S. S. Heterogeneous Integration for Performance and Scaling Trans. Compon., Packag., Manuf. Technol., 2016, 6, 973-982

Thermal Modeling and Simulation

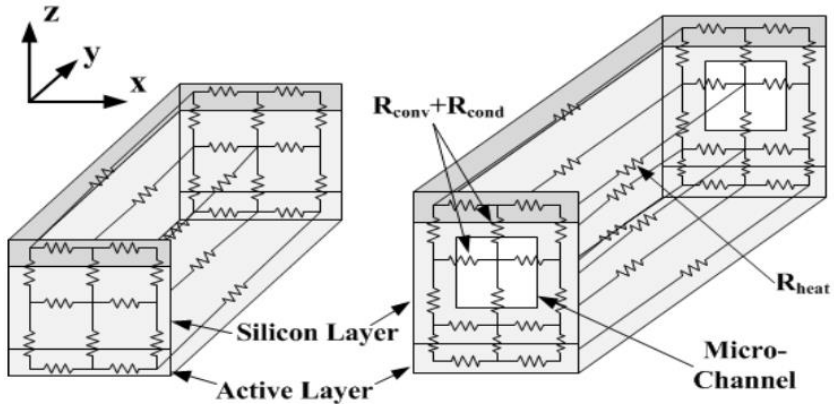
- Thermal modeling
  - FEM, FDM
  - Equivalent RC networks
  - Tailored analytical models (Green's function etc.)



Lee, Y.; Pan, C.; Huang, P. & Yang, C. LUTSim: A Look-Up Table-Based Thermal Simulator for 3-D ICs Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 1250-1263



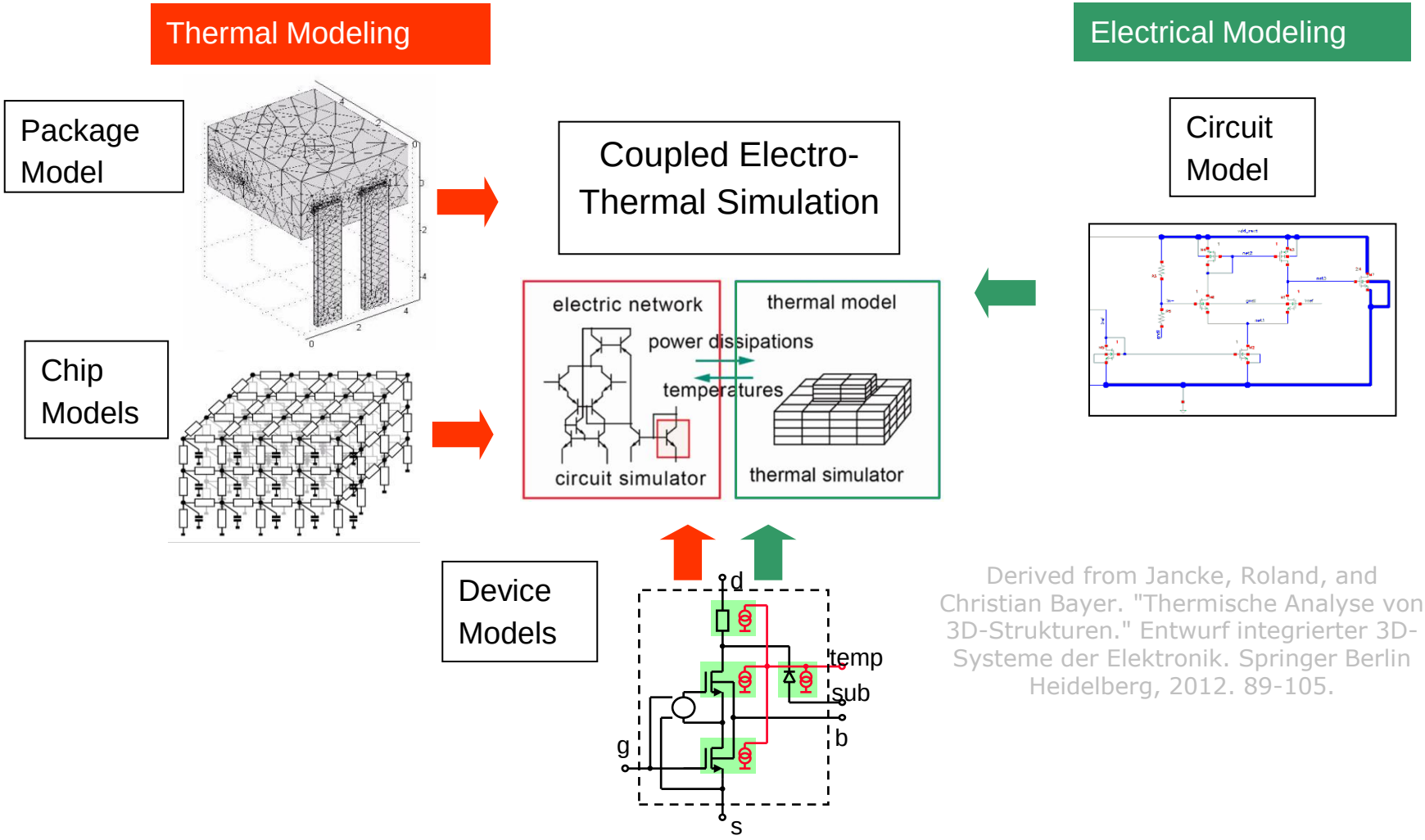
Heinig, A.; Papaioannou, D. & Fischbach, R. Model Abstraction of 3D-Integrated/Interposer-Based High Performance Systems for Faster (Thermal) Simulation Proc. Therm. Thermomech. Phenom. Electr. Syst. Conf., 2016, 230-237



Yang, Z. & Srivastava, A. Physical co-design for micro-fluidically cooled 3D ICs Proc. Therm. Thermomech. Phenom. Electr. Syst. Conf., 2016, 1373-1380

Thermal Modeling and Simulation

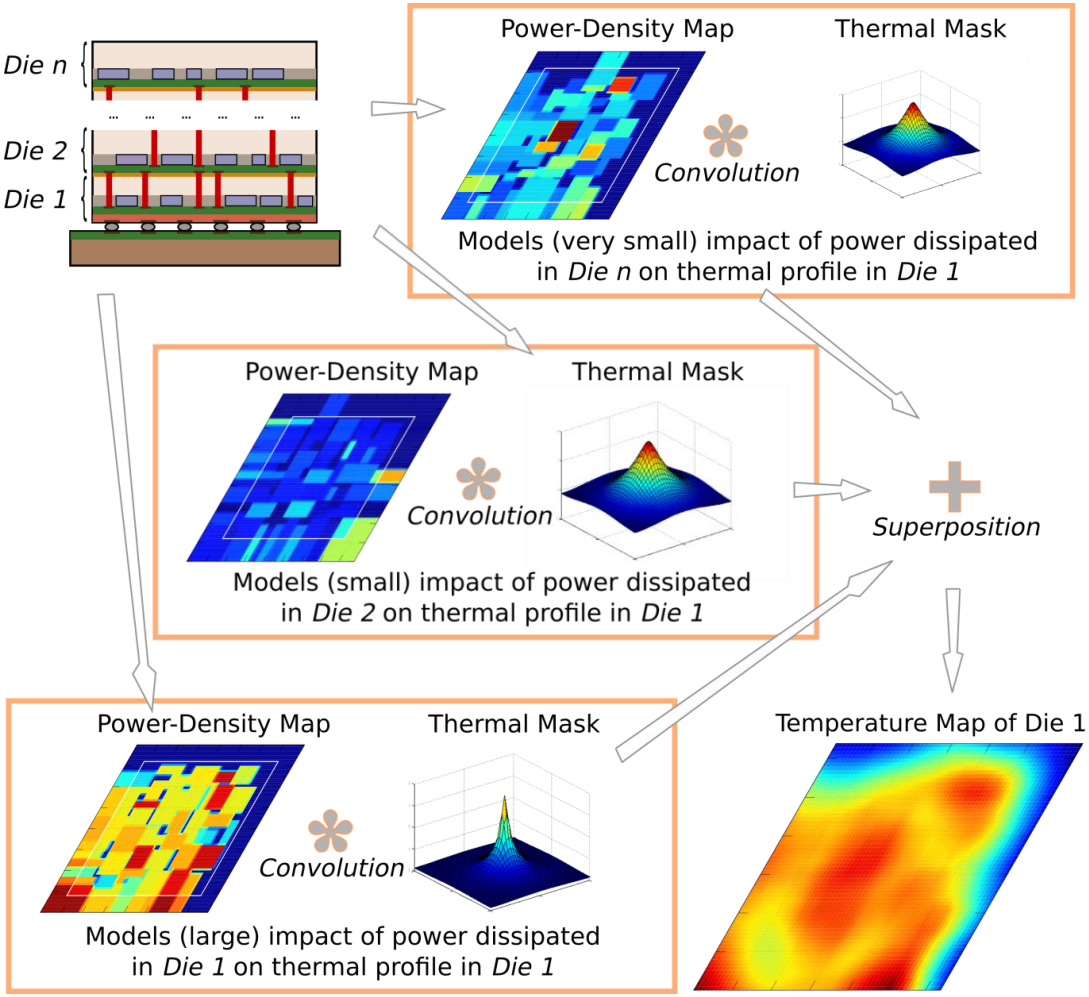
- Thermal simulation: network simulation, can be coupled



Derived from Jancke, Roland, and Christian Bayer. "Thermische Analyse von 3D-Strukturen." Entwurf integrierter 3D-Systeme der Elektronik. Springer Berlin Heidelberg, 2012. 89-105.

Thermal Modeling and Simulation

- Thermal simulation: fast analytical simulations, e.g. power blurring

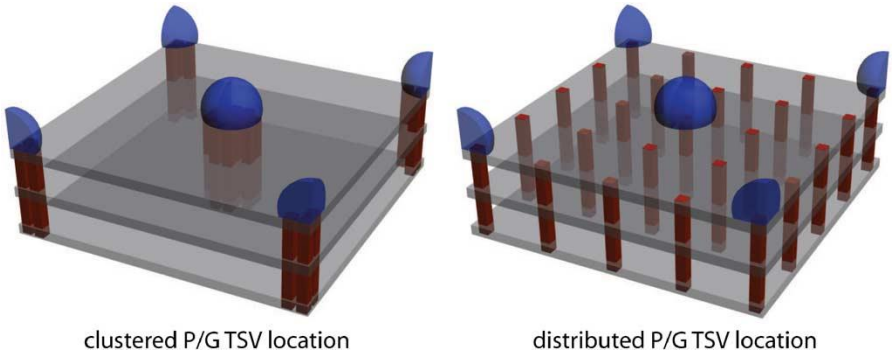


Knechtel, J.; Young, E. & Lienig, J. Planning Massive Interconnects in 3-D Chips Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 1808-1821

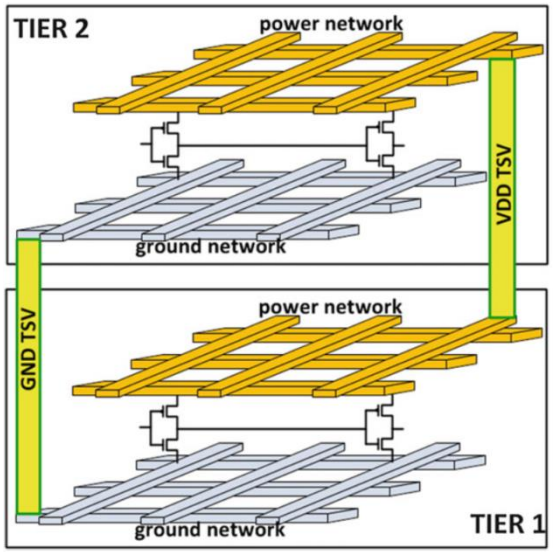
Power Delivery

- For *d* dies, approx. *d*-fold power density than 2D chips
  - Large current to be delivered without excessive noise
  - PDN to be connected and designed across all dies

- Decap dies, multiple power supplies, etc.
- TSVs: multiple, distributed and stacked
- Need for flexible and scalable modeling and simulation



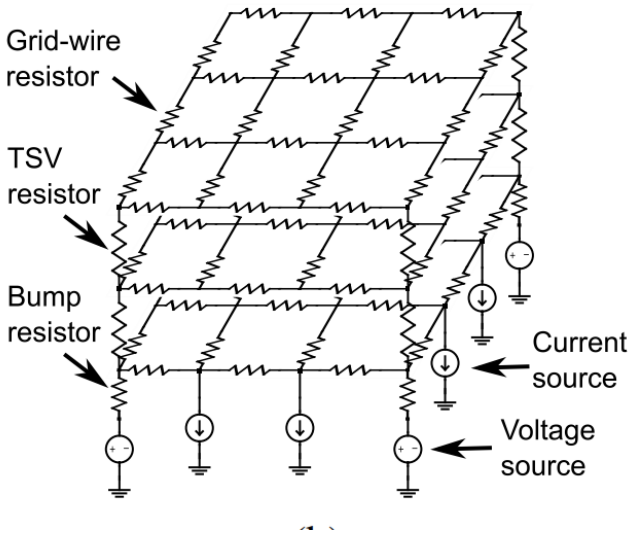
Healy, M. B. & Lim, S. K. "Distributed TSV Topology for 3-D Power-Supply Networks" Trans. VLSI Syst., 2012, 20, 2066-2079



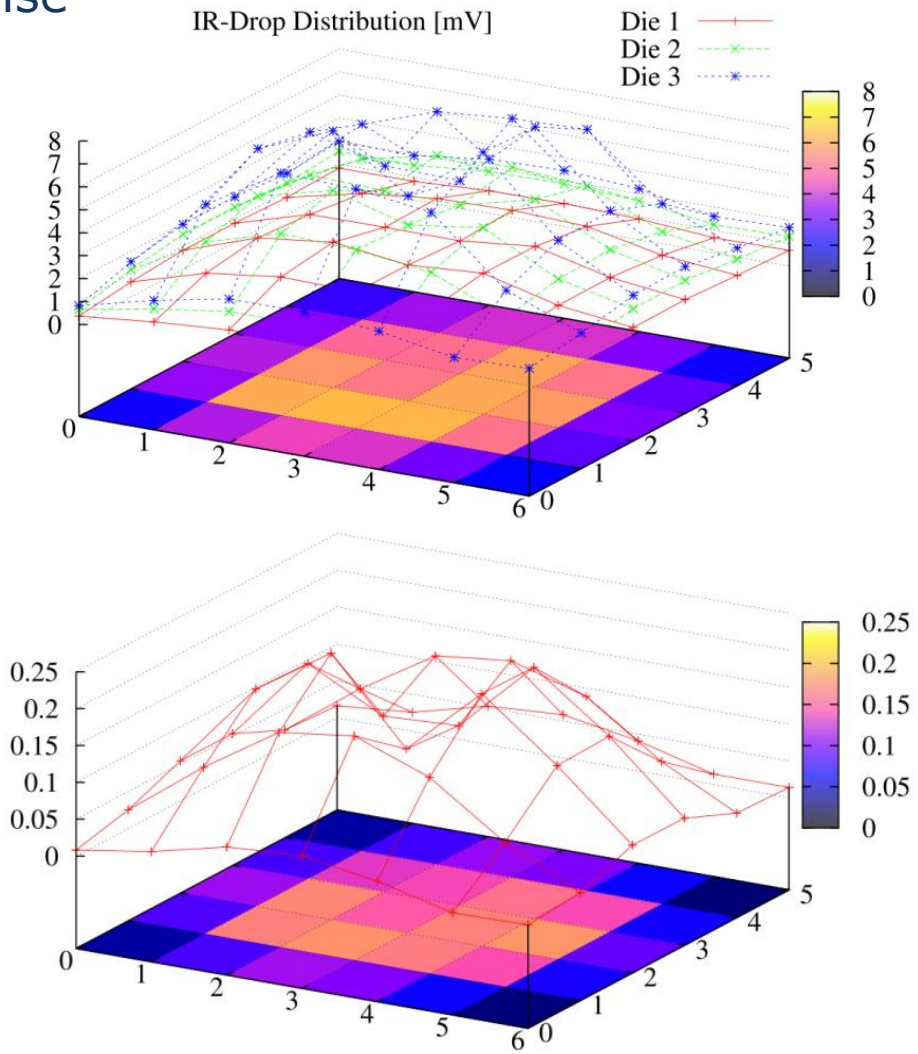
Todri-Sanial, A.; Dijon, J. & Maffucci, A. (Eds.) Carbon Nanotubes for Interconnects Springer International Publishing, 2017

Power Delivery

- Modeling and simulation of PDN noise
  - Similar as with thermal behavior
  - – Equivalent RC networks
  - – Fast analytical models, e.g., superposed 2D Gauss functions

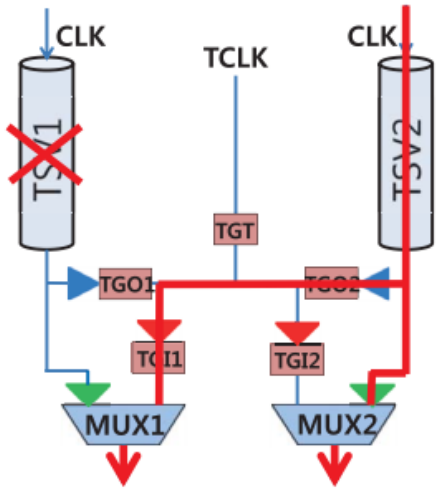


Knechtel, J.; Markov, I. L.; Lienig, J. & Thiele, M. Multiobjective Optimization of Deadspace, a Critical Resource for 3D-IC Integration Proc. Int. Conf. Comp.-Aided Des., 2012, 705-712



Clock Delivery

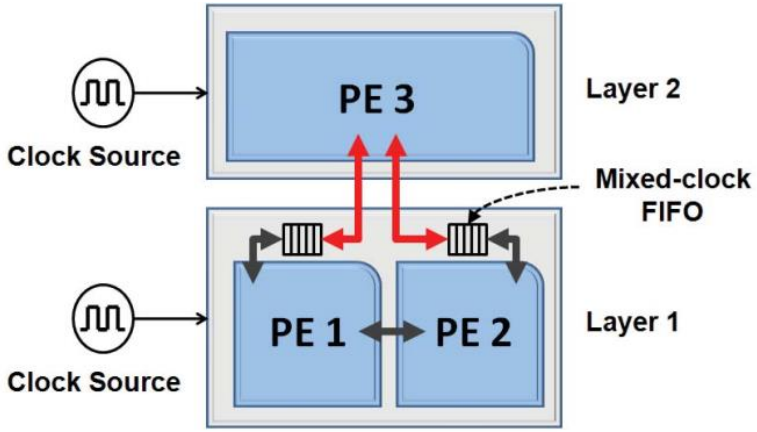
- Reliable, uniform and high-speed delivery across multiple dies
  - Reliability and parametric variations of TSVs
  - Inter-die variations become 1st order problem



Park, H. & Kim, T. Synthesis of TSV Fault-Tolerant 3-D Clock Trees Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 266-279

- Multiple clock TSVs, distributed or in arrays
  - Redundancy architectures
  - Also helps with variations

- Multiple clock domains
  - Mitigates inter-die variations and impact from TSVs
  - Enables KGD testability
  - Essential for larger stacks and interposer stacks

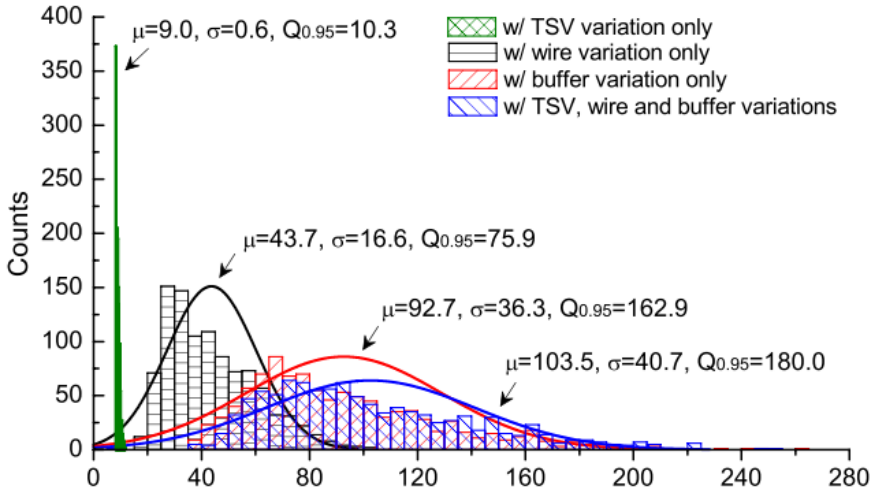


Garg, S. & Marculescu, D. "Mitigating the Impact of Process Variation on the Performance of 3-D Integrated Circuits" Trans. VLSI Syst., 2013, 21, 1903-1914

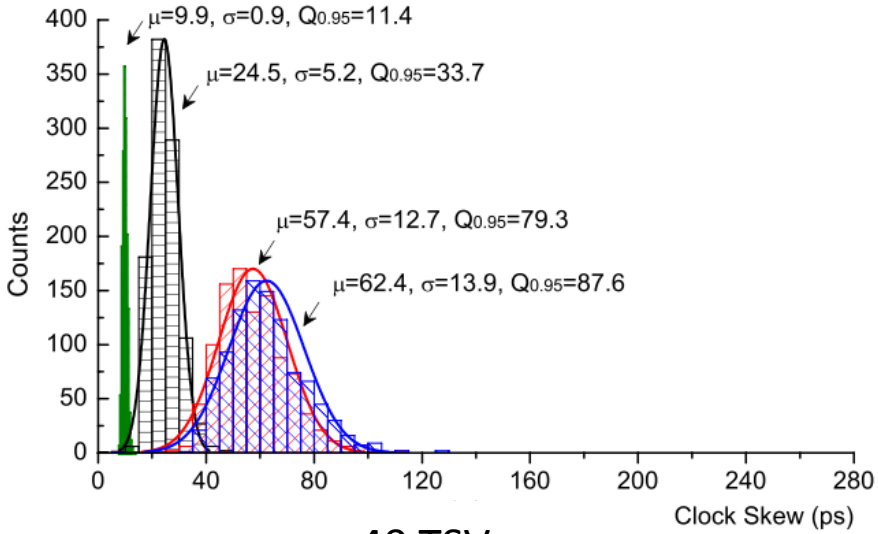
Clock Delivery

- Reliable, uniform and high-speed delivery across multiple dies

- Full-stack 3D clock-network synthesis
  - 3D extension of effective techniques such as MMM and DME
  - Account for variations (inter-die, intra-die, TSVs)
  - Multiple TSVs



1 TSV



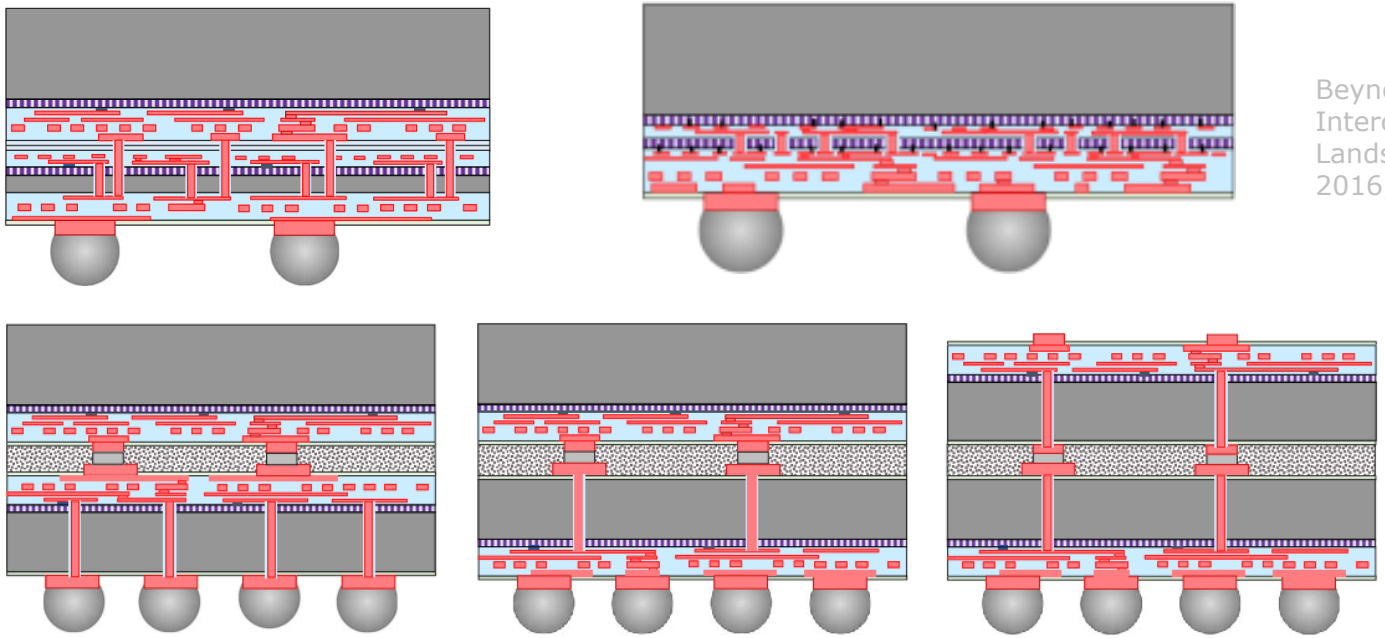
40 TSVs

Zhao, X.; Mukhopadhyay, S. & Lim, S. K. Variation-tolerant and low-power clock network design for 3D ICs Proc. Elec. Compon. Technol. Conf., 2011, 2007-2014

Partitioning and Floorplanning

- Large impact of technology and stacking configuration
- Large correlation/coupling among blocks
- High computational complexity for 2.5D/3D design (NP-complete)

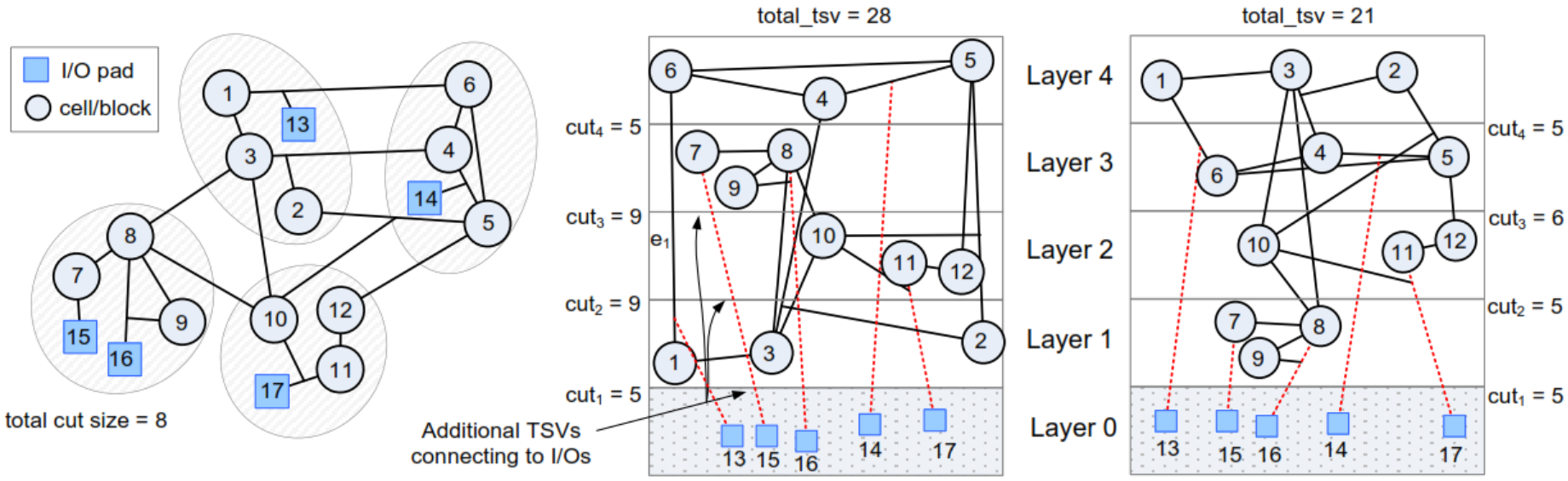
- Need for stacking- and technology-aware approaches
  - Account for different interfaces and interconnect technologies



Beyne, E. The 3-D Interconnect Technology Landscape Design & Test, 2016, 33, 8-20

Partitioning and Floorplanning

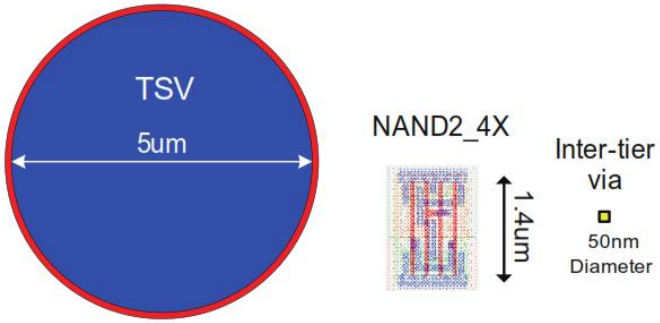
- Account for different interfaces and interconnect technologies
  - Extended min-cut partitioning: ordering of stacked (TSV-based) dies



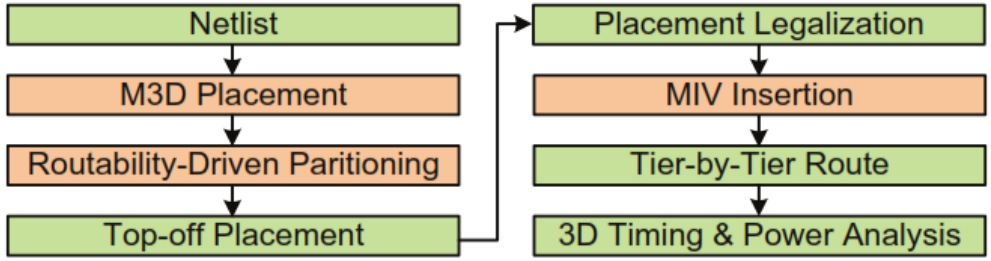
Huang, Y.-S.; Liu, Y.-H. & Huang, J.-D. Layer-Aware Design Partitioning for Vertical Interconnect Minimization ISVLSI, 2011, 144-149

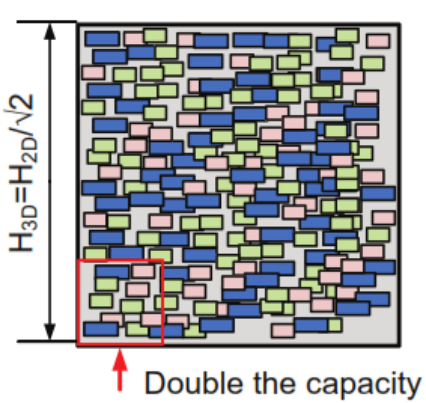
Partitioning and Floorplanning

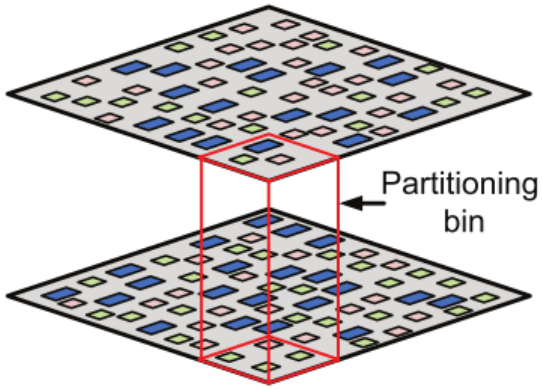
- Account for different interfaces and interconnect technologies
  - Min-cut inappropriate for monolithic 3D stacks; many cuts desired
  - Placement-driven and routing-aware partitioning



Liu, C. & Lim, S. K. A Design Tradeoff Study with Monolithic 3D Integration Proc. Int. Symp. Quality Elec. Des., 2012



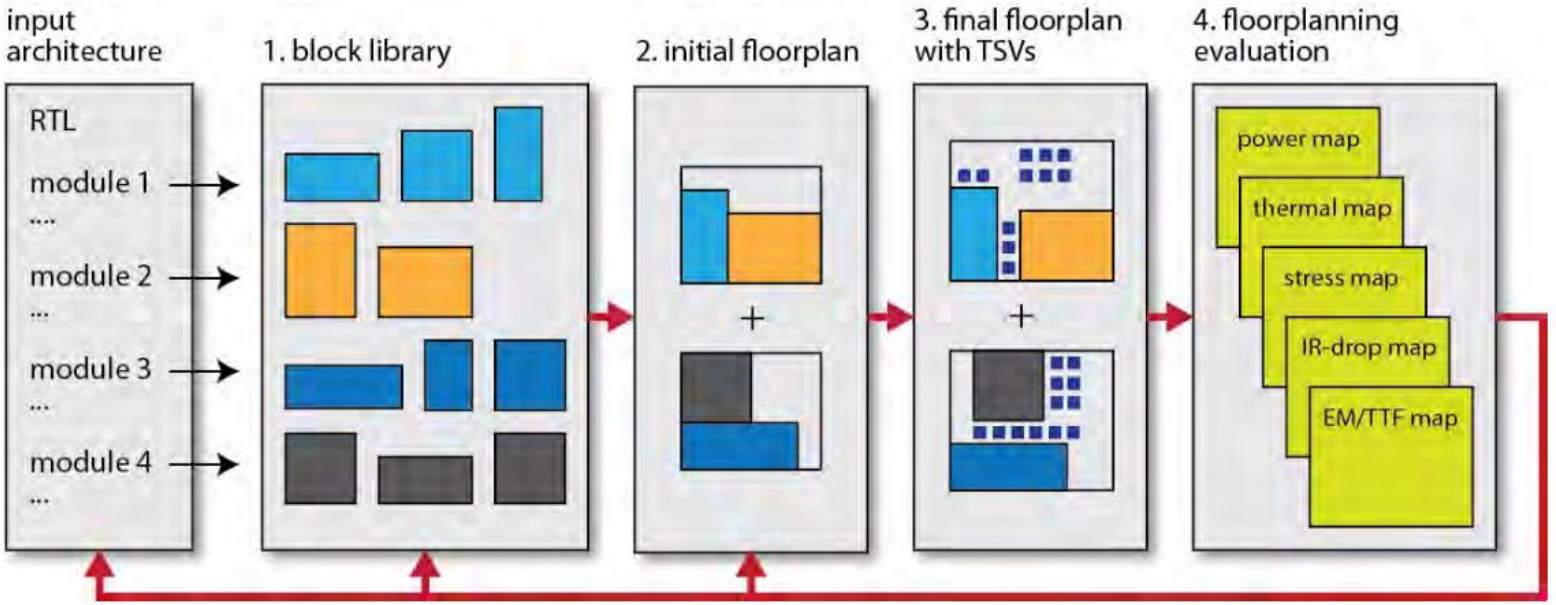




Panth, S.; Samadi, K.; Du, Y. & Lim, S. Placement-Driven Partitioning for Congestion Mitigation in Monolithic 3D IC Designs Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 540-553

Partitioning and Floorplanning

- Multi-objective, fast and scalable yet accurate tools
  - Thermal management
  - PDN-noise management
  - Stress management
  - Interconnects-aware timing (wires, TSVs)
  - Co-arrangement of modules and global interconnects (wires, TSVs)
  - Folding/splitting modules

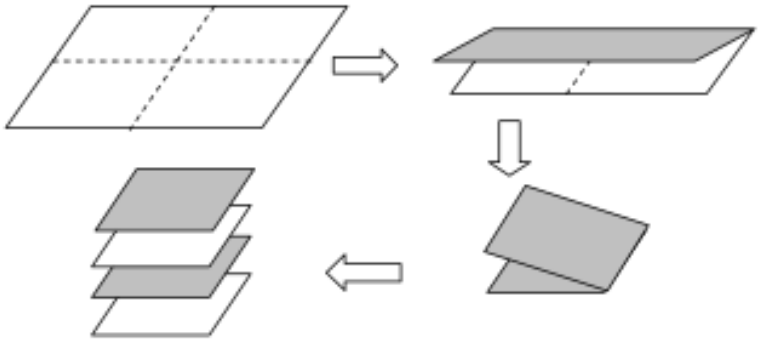


Lim, S. K. Research Needs for TSV-Based 3D IC Architectural Floorplanning J. Inf. Commun. Converg. Eng., 2014, 12, 46-52

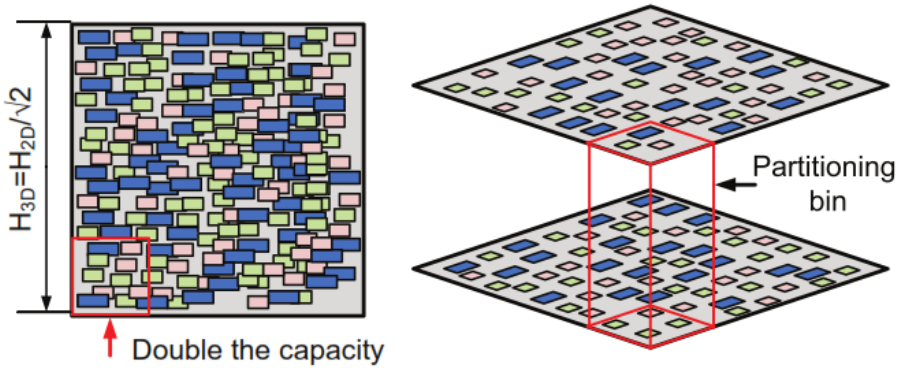
Placement

- High complexity and large correlation/coupling among blocks
  - Need for flexible and scalable placement techniques

- Folding- or partitioning-based placement
  - Reuse of 2D tools/know-how
  - Limited consideration of interconnects/interfaces
  - Practical for monolithic ICs



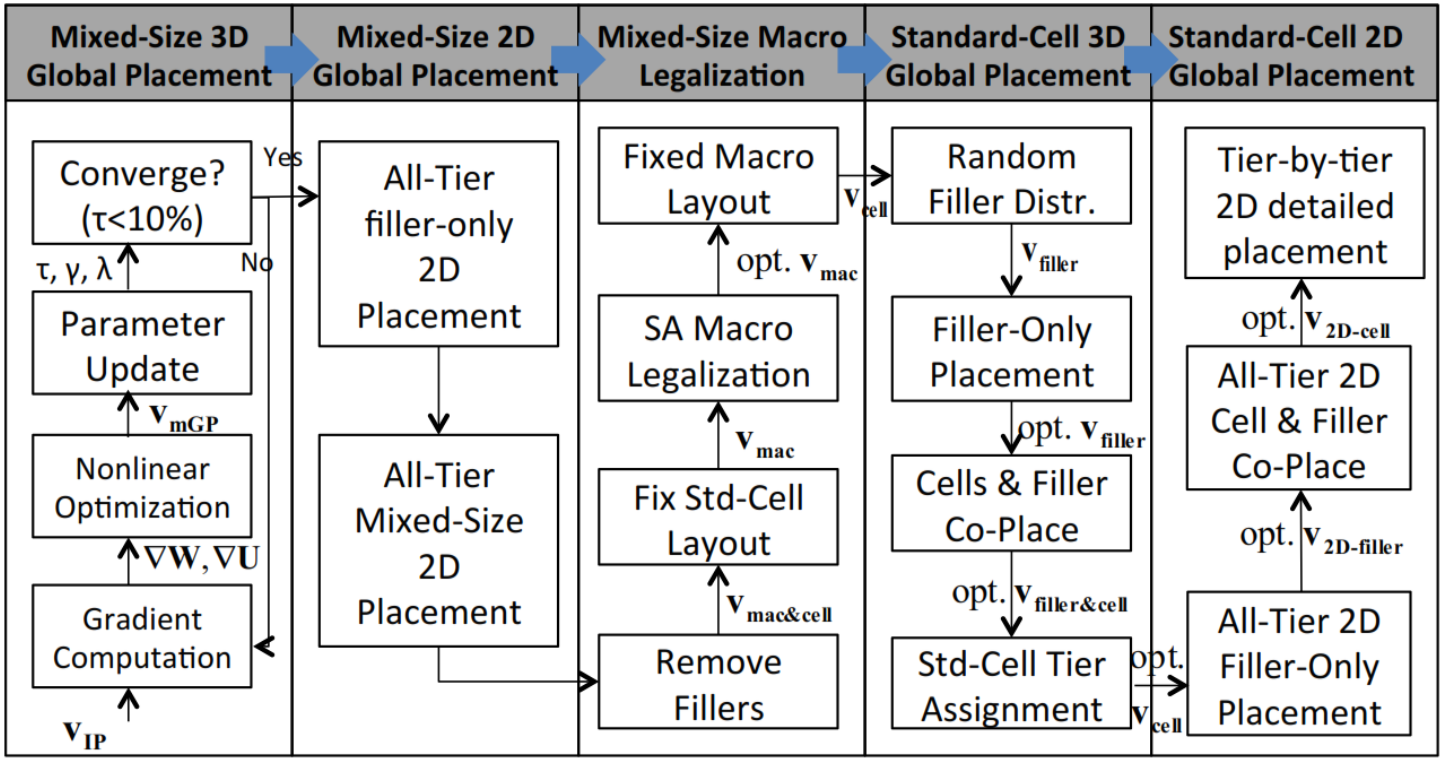
Cong, J.; Luo, G.; Wei, J. & Zhang, Y. "Thermal-Aware 3D IC Placement Via Transformation" Proc. Asia South Pacific Des. Autom. Conf., 2007, 780-785



Panth, S.; Samadi, K.; Du, Y. & Lim, S. Placement-Driven Partitioning for Congestion Mitigation in Monolithic 3D IC Designs Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 540-553

Placement

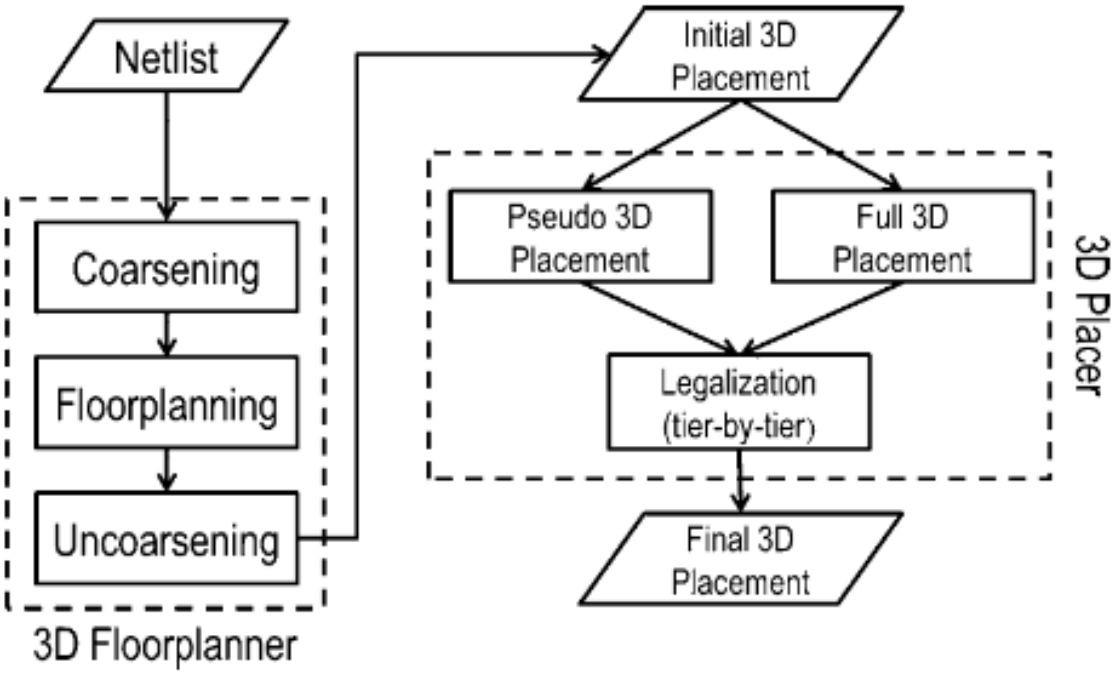
- Analytic placement
  - Motivated by recent progress for 2D placement
  - "Natural" arrangement of cells in 2.5D/3D domain
  - Complex; requires clustering and coarsening, global smoothing, etc.



Lu, J.; Zhuang, H.; Kang, I.; Chen, P. & Cheng, C.-K. ePlace-3D: Electrostatics Based Placement for 3D-ICs Proc. Int. Symp. Phys. Des., 2016, 11-18

Placement

- Hierarchical placement
  - A framework for GP, DP, legalization
  - Not flat; includes floorplanner
  - Not restrictive; analytic placer engine(s) or others

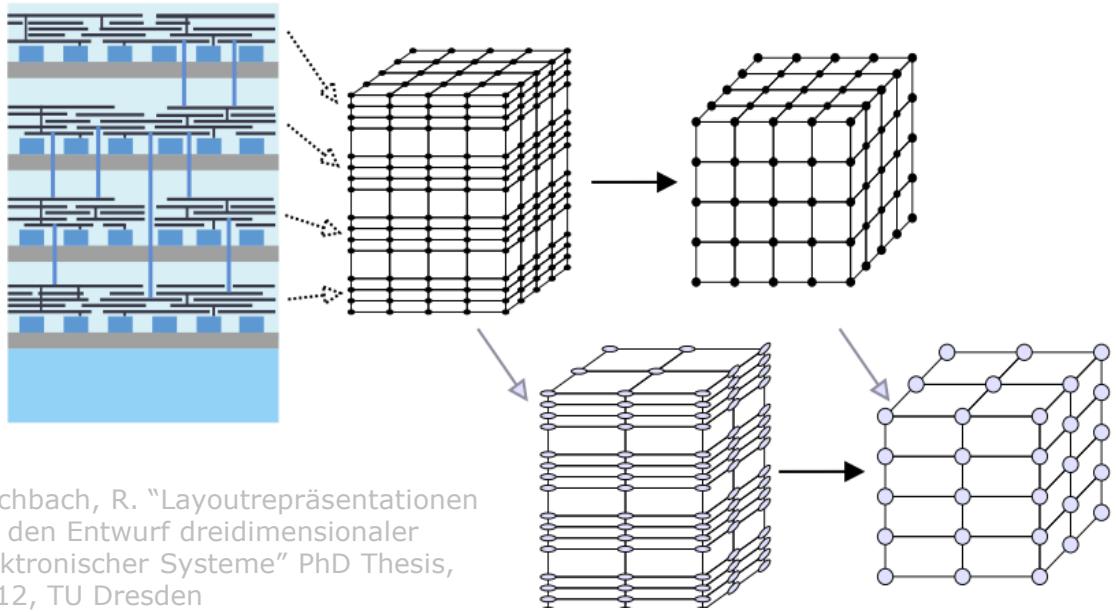


Luo, G.; Shi, Y. & Cong, J. "An Analytical Placement Framework for 3-D ICs and Its Extension on Thermal Awareness" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 510-523

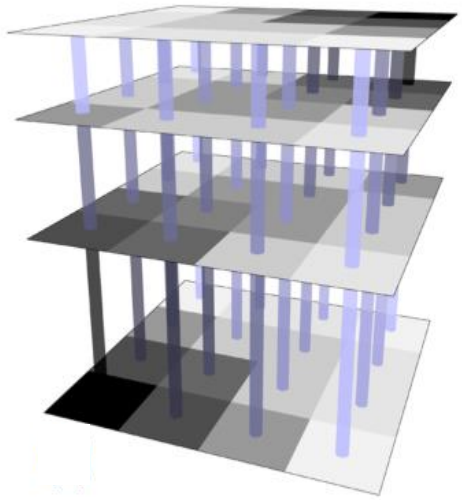
Routability Estimation and Routing

- Heterogeneous, large-scale interconnect topologies
  - Need for routability estimation and adapted routing

- Routability estimation: stacking- and technology-aware
  - Interconnects distribution models, with TSVs, buffers etc.
  - 3D HPWL and 3D routing graphs
  - Probabilistic or heuristic routing models



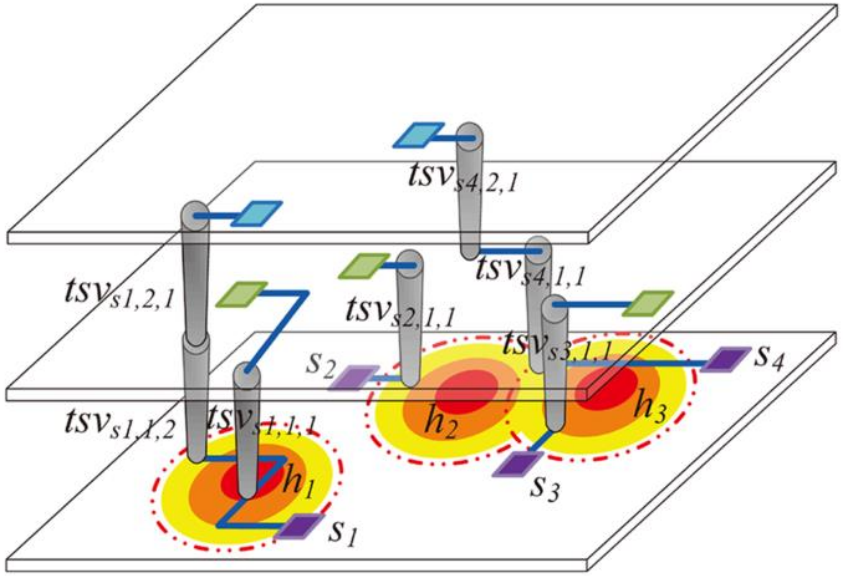
Fischbach, R. "Layoutrepräsentationen für den Entwurf dreidimensionaler elektronischer Systeme" PhD Thesis, 2012, TU Dresden



Routability Estimation and Routing

- Heterogeneous, large-scale interconnect topologies
  - Need for routability estimation and adapted routing

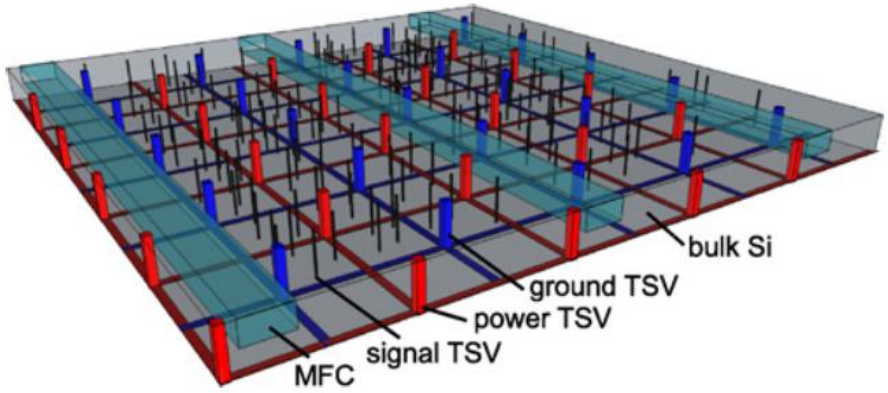
- Detailed routing: not fundamentally different than in 2D ICs
- Global routing: leverage on 3D routing for 2D ICs
  - Extend classical techniques, e.g., 3D Steiner trees
  - Thermal-, power-, and delay-aware tree construction



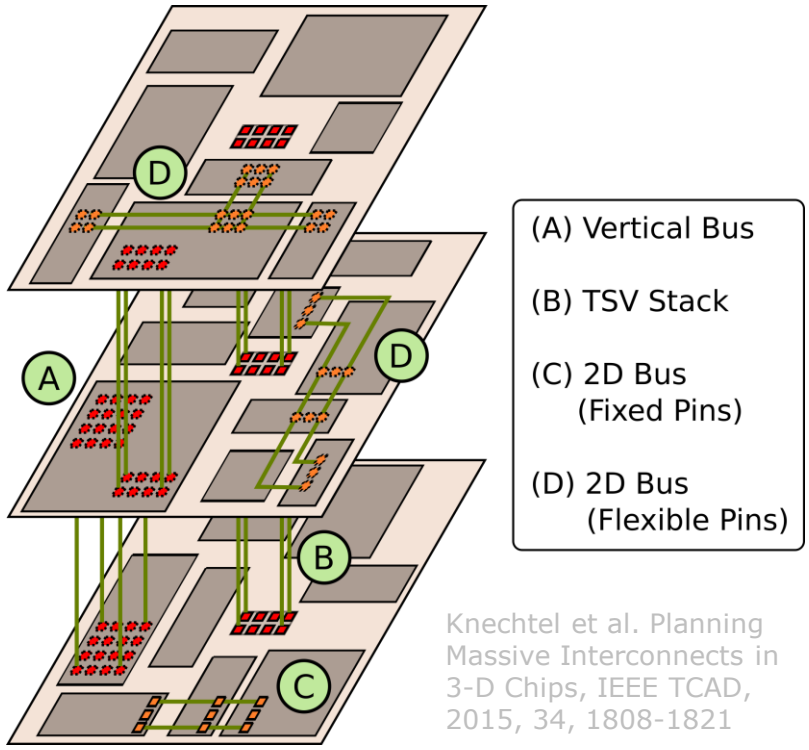
Hsu et al., Stacking Signal TSV for Thermal Dissipation in Global Routing for 3-D IC, IEEE TCAD, 2014, 33, 1031-1042

Routability Estimation and Routing

- Heterogeneous, large-scale interconnect topologies
  - Need for routability estimation and adapted routing
- Global routing: different types of TSVs and global interconnects
  - Synchronize with power delivery, floorplanning, placement, routing etc.



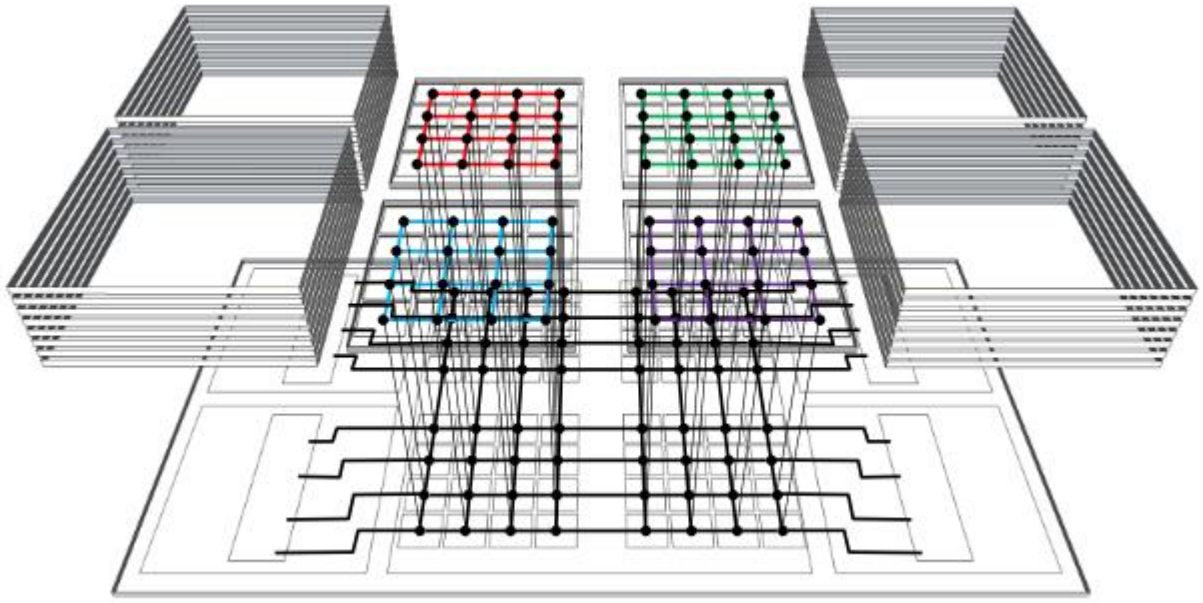
Lee, Y.-J. & Lim, S. K. Co-Optimization and Analysis of Signal, Power, and Thermal Interconnects in 3-D ICs Trans. Comp.-Aided Des. Integr. Circ. Sys., 2011, 30, 1635-1648



Knechtel et al. Planning Massive Interconnects in 3-D Chips, IEEE TCAD, 2015, 34, 1808-1821

Routability Estimation and Routing

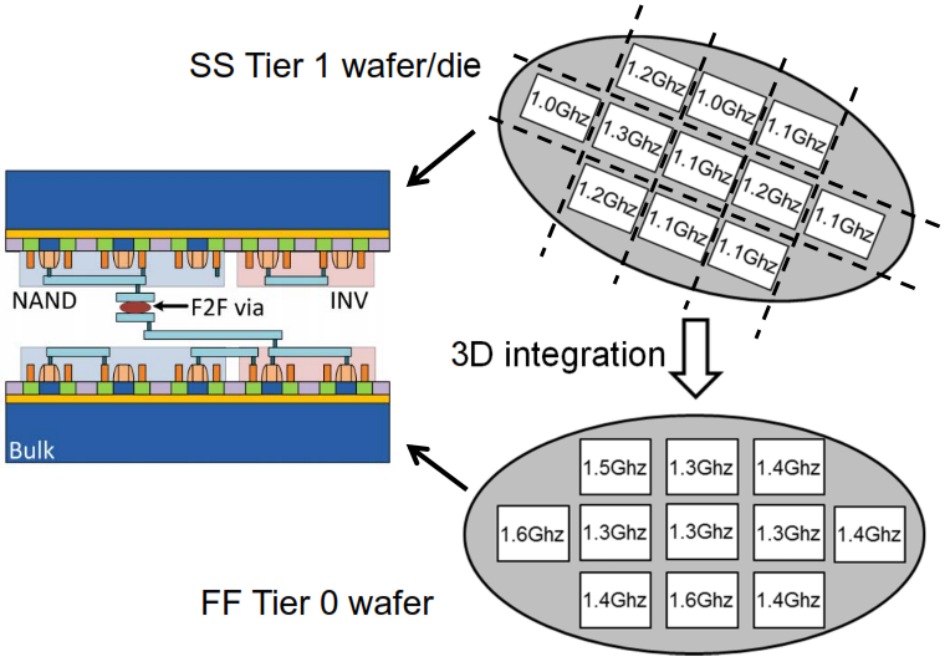
- Heterogeneous, large-scale interconnect topologies
  - Need for routability estimation and adapted routing
- Global routing: 3D NoC design
  - Synchronized design of distributed and partial NoCs
  - Exploration of various topology, technology and architectural options

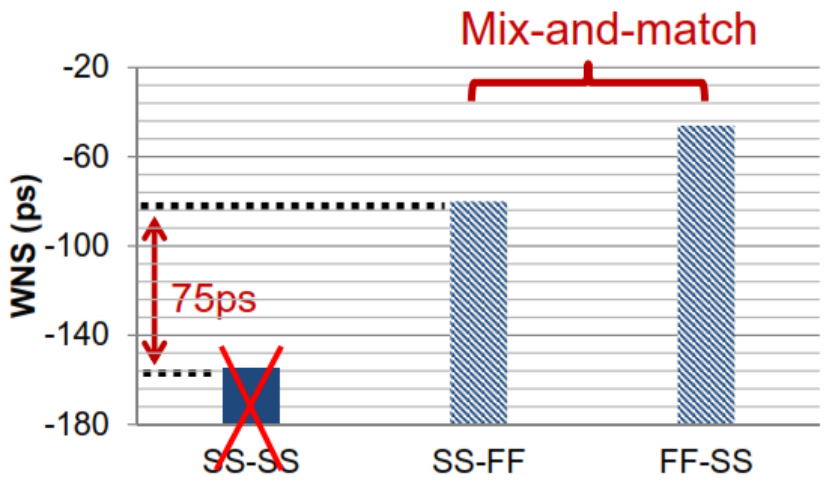


Loh, G. H.; Jerger, N. E.; Kannan, A. & Eckert, Y. "Interconnect-Memory Challenges for Multi-chip, Silicon Interposer Systems" Proc. MEMSYS, 2015, 3-10

Timing Closure

- Intra- and inter-die variations
- Stacking of properly matched dies
  - SS/SS or FF/FF not to be stacked; no need to consider for design corners
  - Match SS/FF or FF/SS



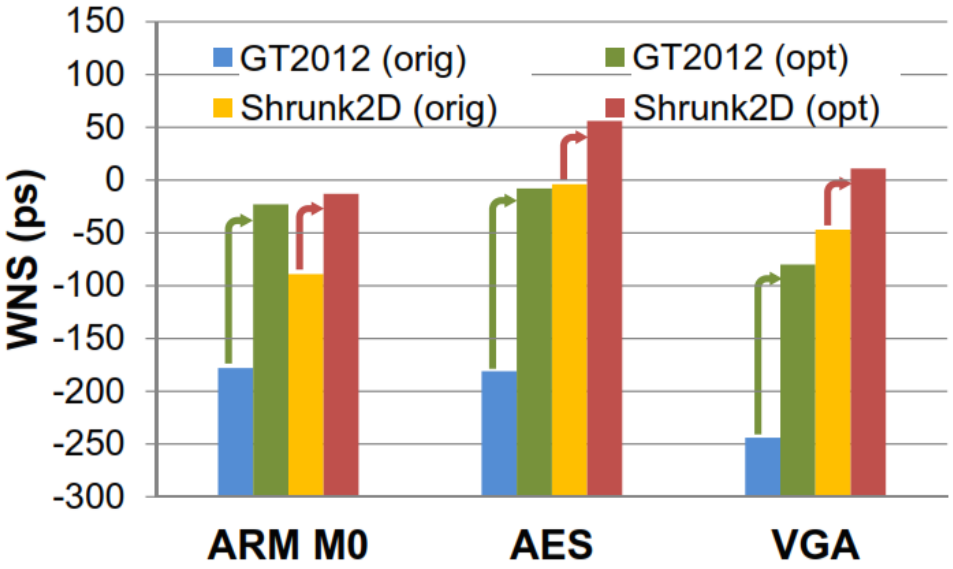


A. B. Kahng, In Search of Lost Time, TAU-2016 Keynote

Timing Closure

- Intra- and inter-die variations

- Stacking of properly matched dies
  - Cut timing paths such that delays are balanced
  - Reduces overhead and improves timing



Technology: 28FDSOI

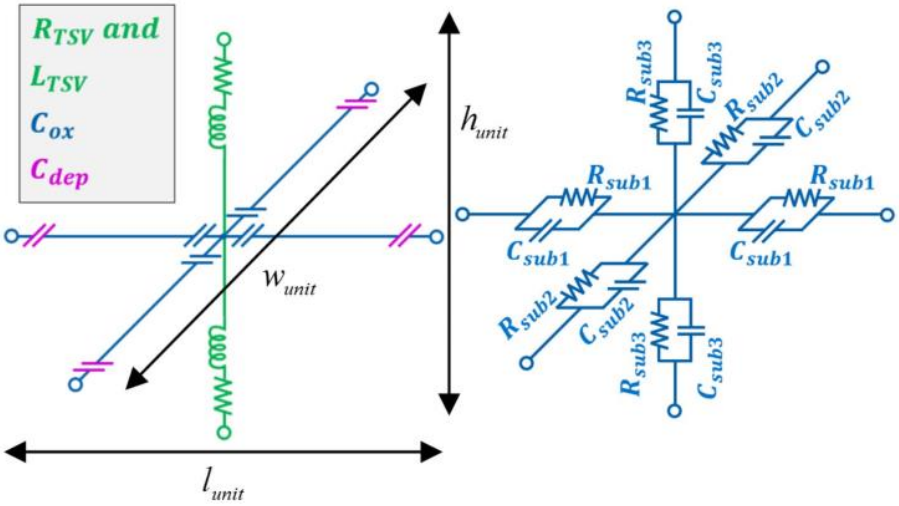
Design	Clk period
M0	1.2ns
AES	1.1ns
VGA	1.0ns

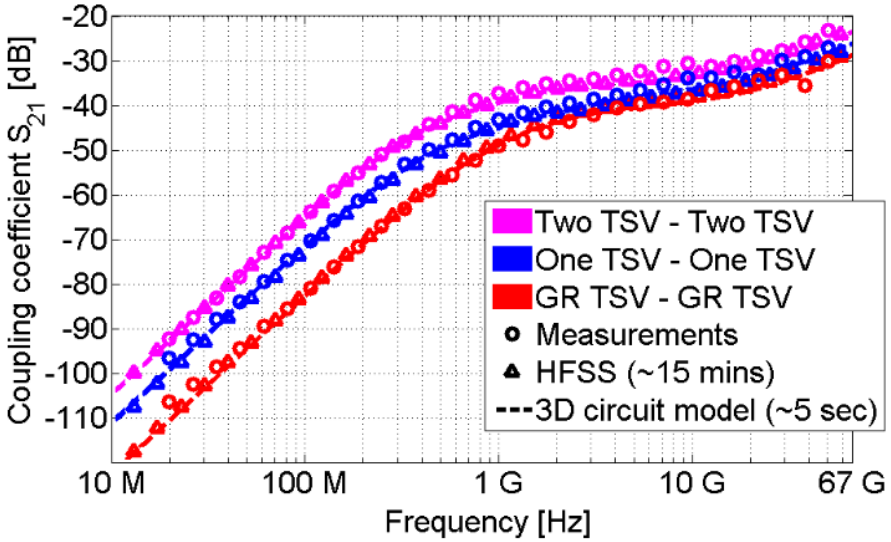
A. B. Kahng, In Search of Lost Time, TAU-2016 Keynote

Timing Closure

- Intra- and inter-die variations
- TSVs induce cross-coupling and timing variations

- TSV coupling: models
  - Equivalent networks, verified against FEM simulations



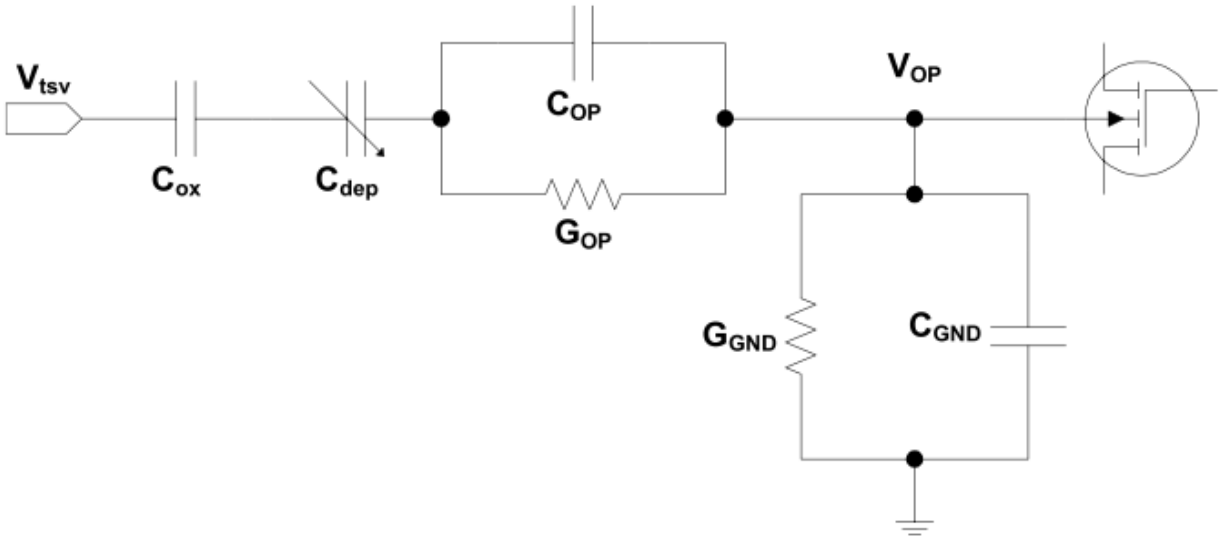


Rack et al., Fast and Accurate Modelling of Large TSV Arrays in 3D-ICs Using a 3D Circuit Model Validated Against Full-Wave FEM Simulations and RF Measurements Proc. Elec. Compon. Technol. Conf., 2016, 966-971

Timing Closure

- Intra- and inter-die variations
- TSVs induce cross-coupling and timing variations

- TSV coupling: models
  - Equivalent networks, verified against FEM simulations
  - Can also account for coupling into transistors

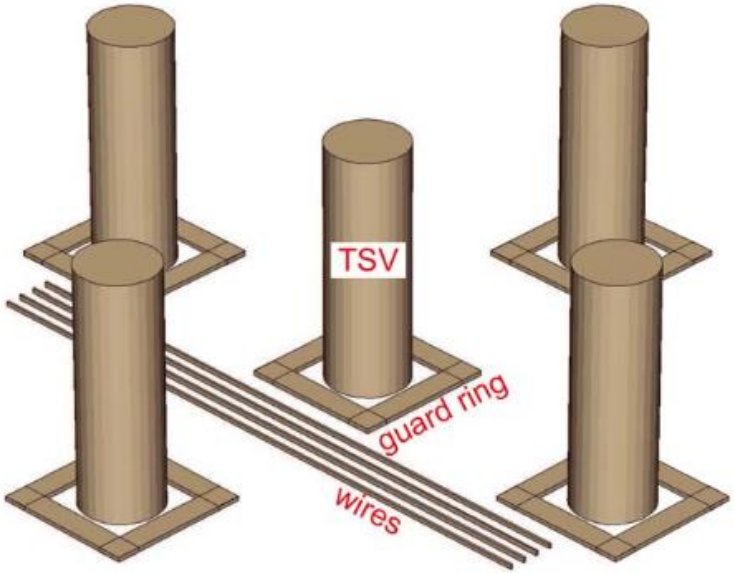


Gaynor, B. & Hassoun, S. Simulation Methodology and Evaluation of Through Silicon Via (TSV)-FinFET Noise Coupling in 3-D Integrated Circuits Trans. VLSI Syst., 2015, 23, 1499-1507

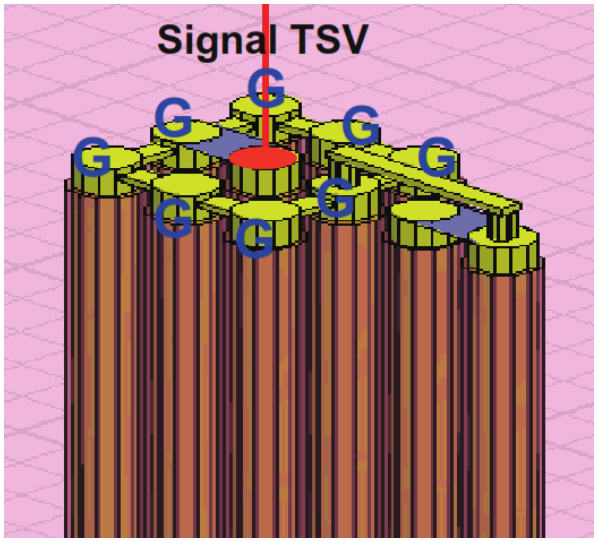
Timing Closure

- Intra- and inter-die variations
- TSVs induce cross-coupling and timing variations

- TSV coupling: countermeasures
  - TSV arrangement and/or shielding



Peng, Y.; Petranovic, D. & Lim, S. K. Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-Wire Coupling Trans. Comp.-Aided Des. Integr. Circ. Sys., 2015, 34, 1964-1976

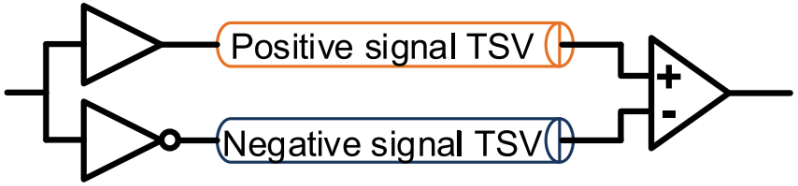


Liu, C.; Song, T.; Cho, J.; Kim, J.; Kim, J. & Lim, S. K. Full-Chip TSV-to-TSV Coupling Analysis and Optimization in 3D IC Proc. Des. Autom. Conf., 2011

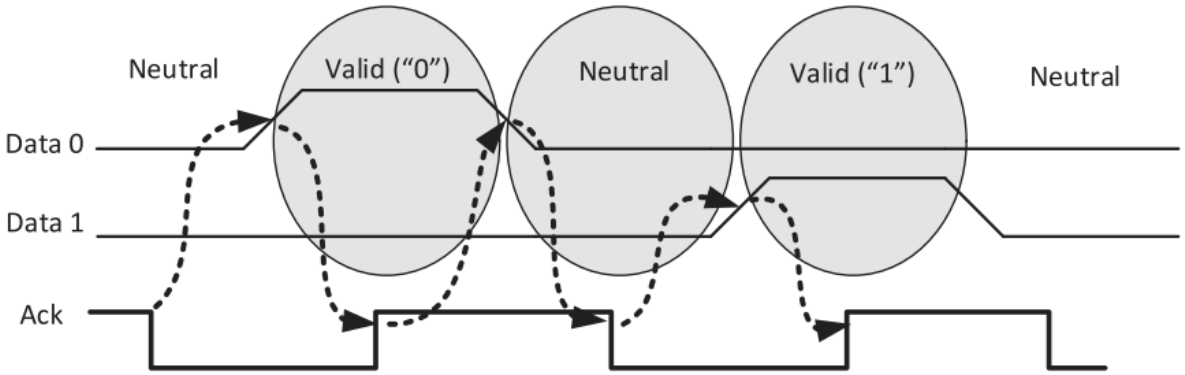
Timing Closure

- Intra- and inter-die variations
- TSVs induce cross-coupling and timing variations

- TSV coupling: countermeasures
  - TSV arrangement and/or shielding
  - Differential transmission or dual-rail encoding



Peng, Y.; Song, T.; Petranovic, D. & Lim, S. K. Silicon Effect-Aware Full-Chip Extraction and Mitigation of TSV-to-TSV Coupling Trans. Comp.-Aided Des. Integr. Circ. Sys., 2014, 33, 1900-1913

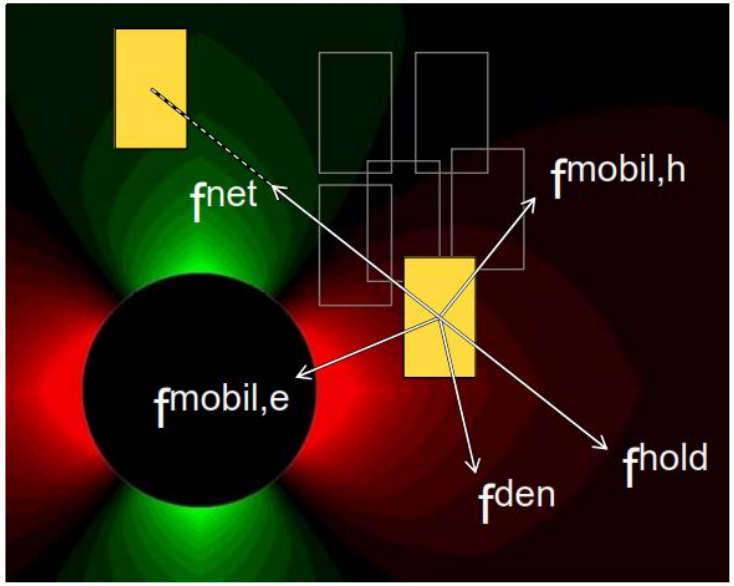


Yaghini, P. M.; Eghbal, A.; Yazdi, S. S.; Bagherzadeh, N. & Green, M. M. Capacitive and Inductive TSV-to-TSV Resilient Approaches for 3D ICs Trans. Comp., 2016, 65, 693-705

Timing Closure

- Intra- and inter-die variations
- TSVs induce cross-coupling and timing variations

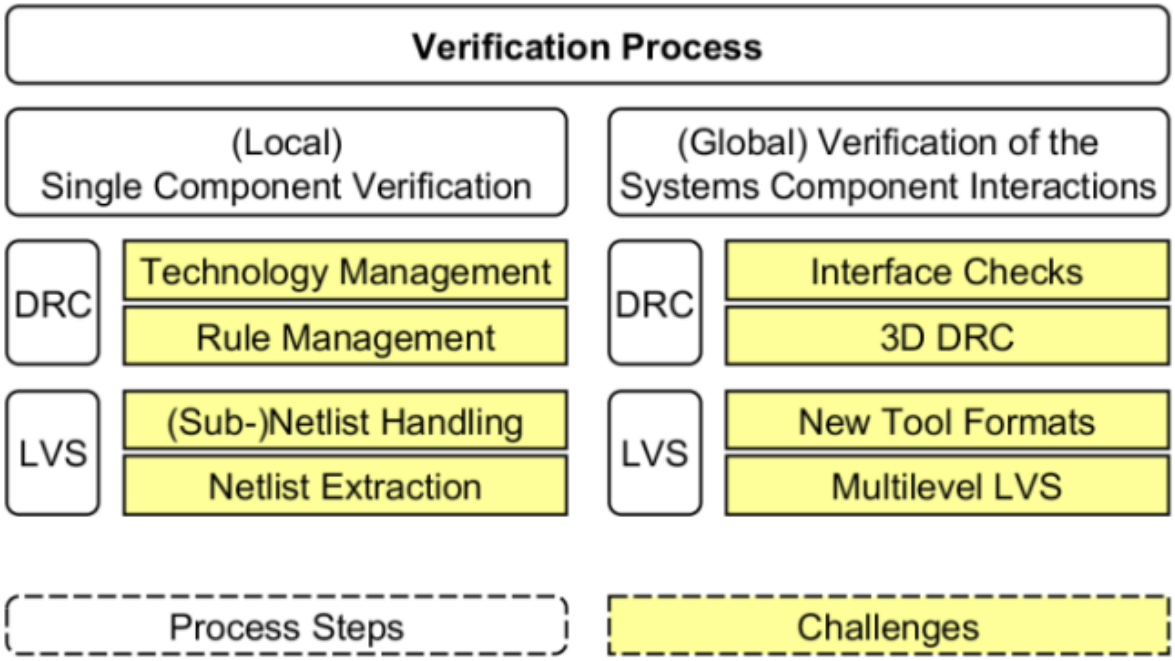
- TSV coupling: countermeasures
  - TSV arrangement and/or shielding
  - Differential transmission or dual-rail encoding
  - Stress-aware (electron, hole mobility) DP or placement post-processing (stress modeling discussed later)



Athikulwongse et al., Stress-driven 3D-IC placement with TSV keep-out zone and regularity study Proc. Int. Conf. Comp.-Aided Des., 2010, 669-674

Physical Verification

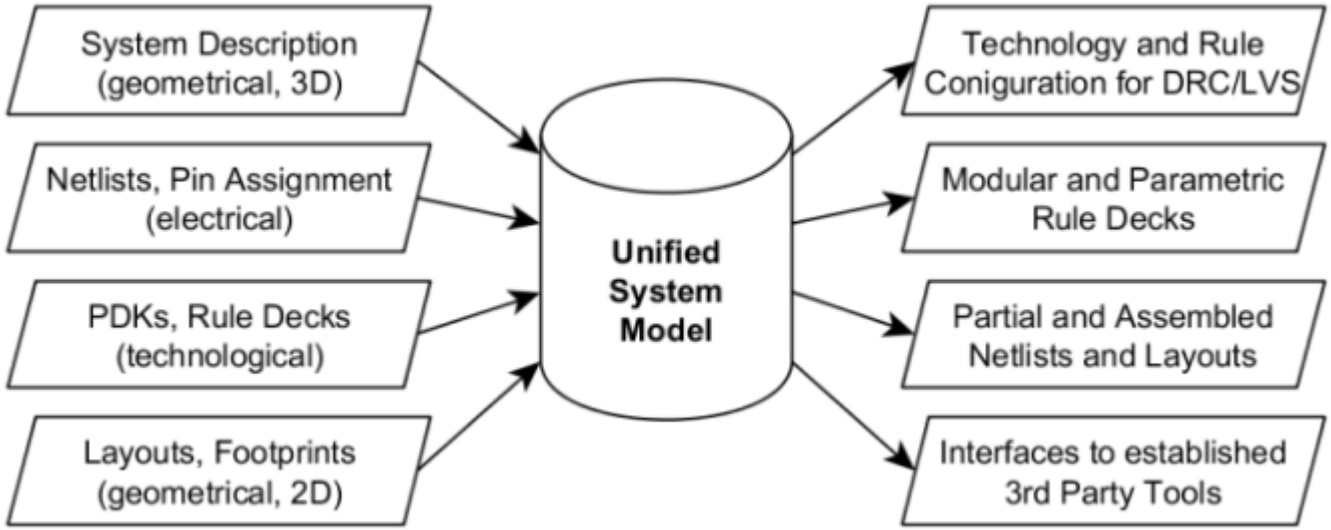
- Multitude of components, various levels for DRC and LVS
  - Novel physical and architectural components
  - Verification on all levels: package-, chip-, gate-, and transistor-level



Fischbach, R.; Heinig, A. & Schneider, P. Design rule check and layout versus schematic for 3D integration and advanced packaging Proc. 3D Sys. Integr. Conf., 2014, 1-7

Physical Verification

- Multitude of components, various levels for DRC and LVS
- Shared database, with converter capabilities and interfaces
  - For example, assembly design kit (ADK)

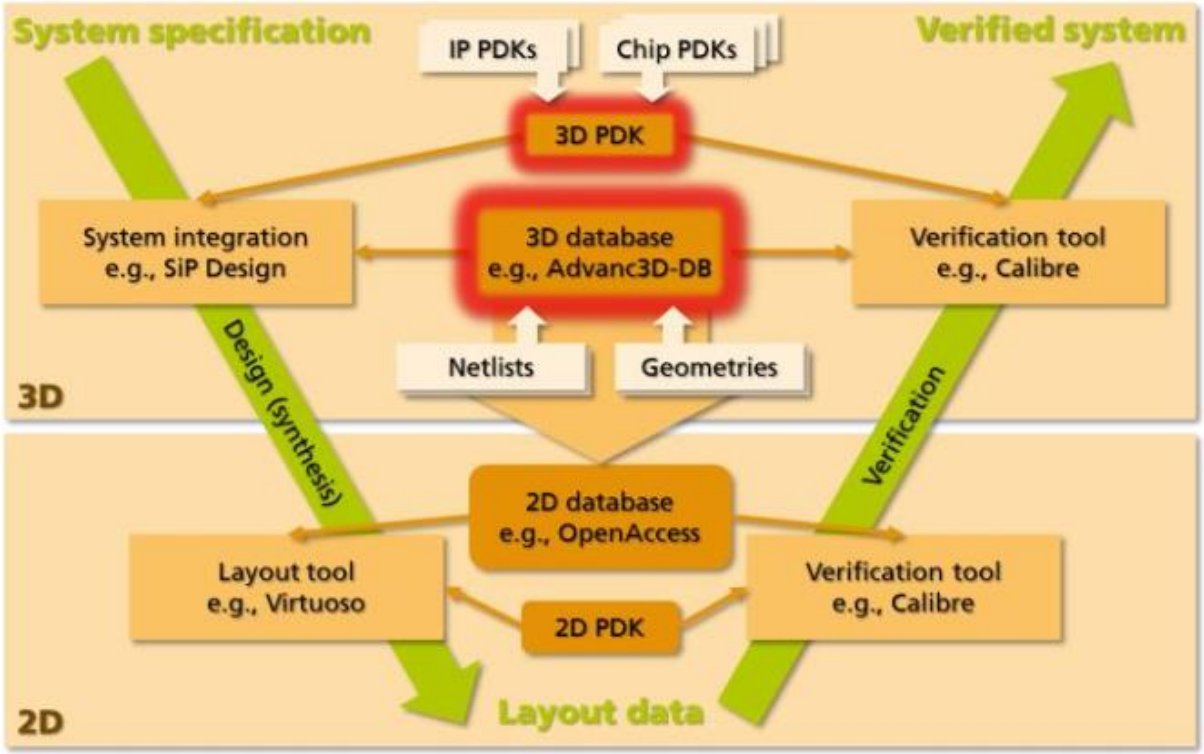


Fischbach, R.; Heinig, A. & Schneider, P. Design rule check and layout versus schematic for 3D integration and advanced packaging Proc. 3D Sys. Integr. Conf., 2014, 1-7

Physical Verification

- Multitude of components, various levels for DRC and LVS

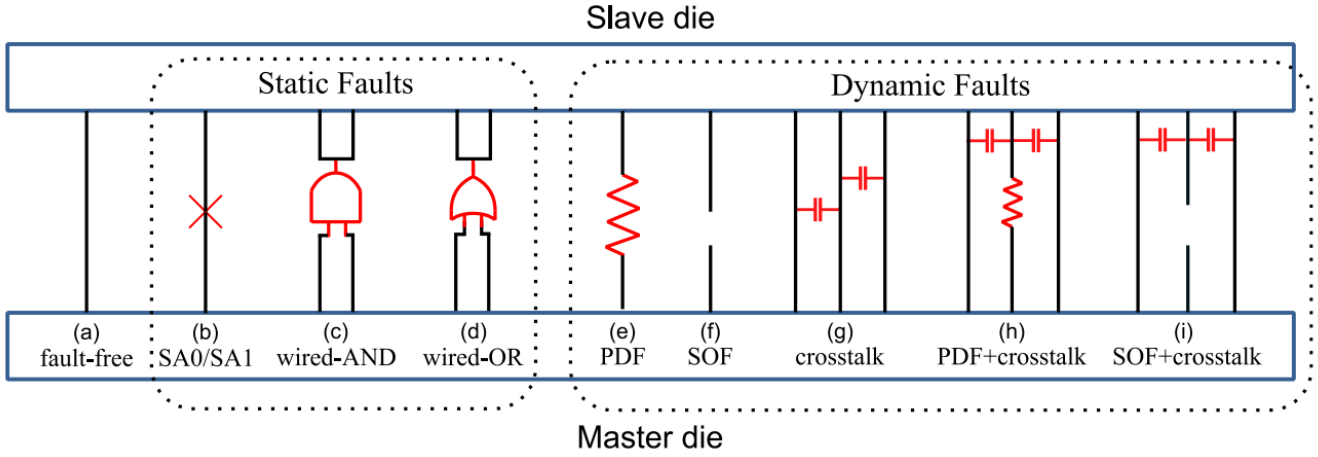
- Unified and hierarchical verification framework
  - Delegate verification to available and new tools



Fischbach, R.; Heinig, A. & Schneider, P. Design rule check and layout versus schematic for 3D integration and advanced packaging Proc. 3D Sys. Integr. Conf., 2014, 1-7

Design for Testability

- Multiple testing requirements
  - Faults and symptomatic impact (e.g., delay) of wires and TSVs
  - Pre-bond, mid-bond, post-bond and final package testing



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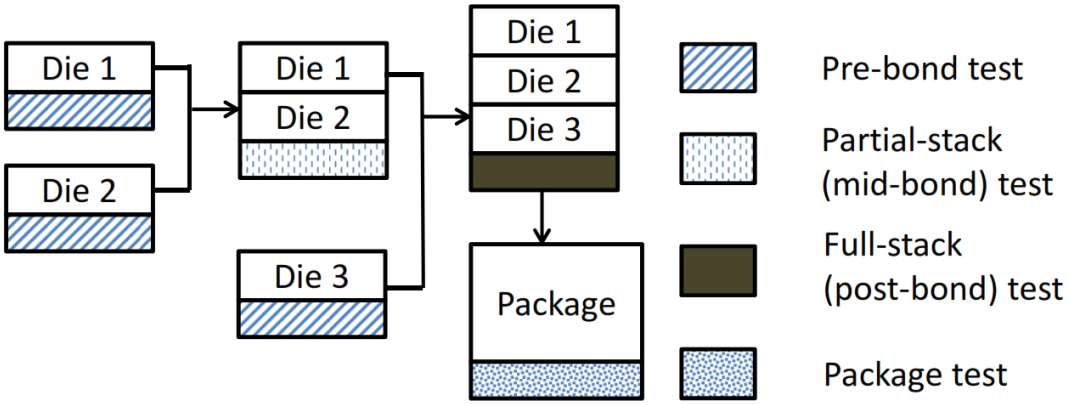

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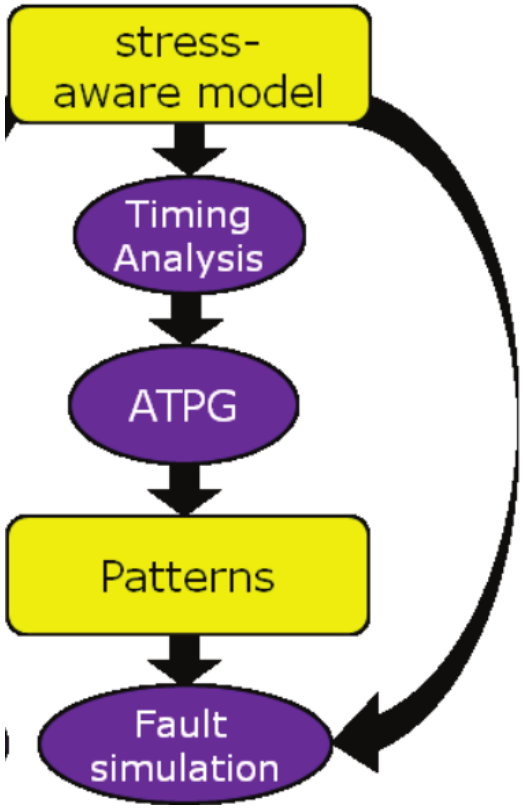
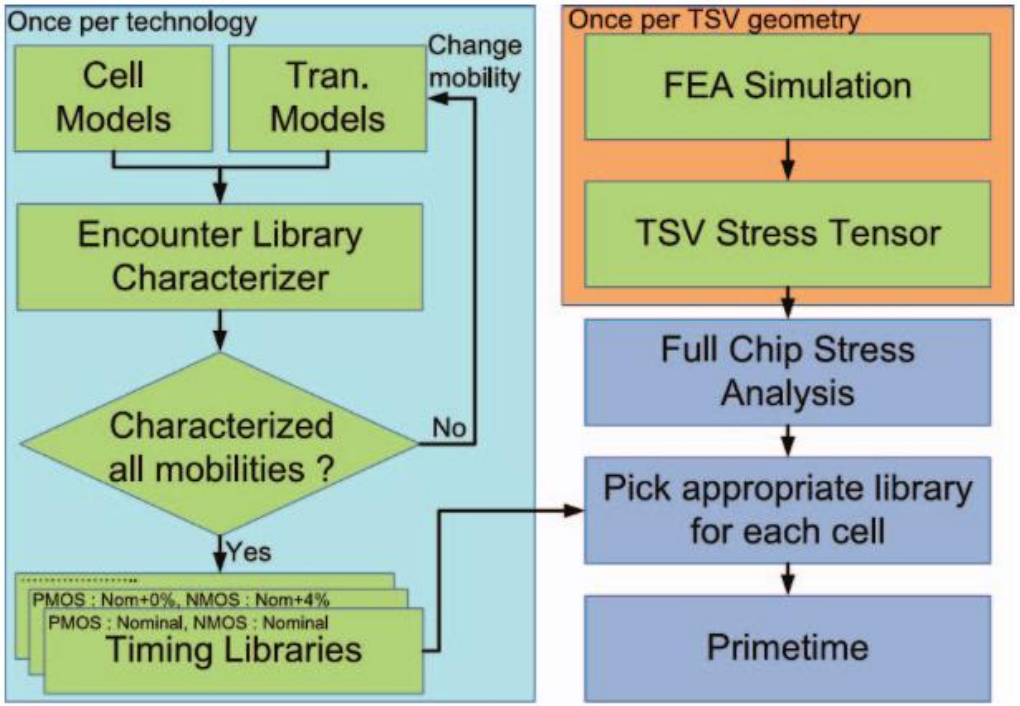
Design for Testability

- Multiple testing requirements
  - Faults and symptomatic impact (e.g., delay) of wires and TSVs
- Tailored fault models, e.g., ATPG considering stress and timing impact

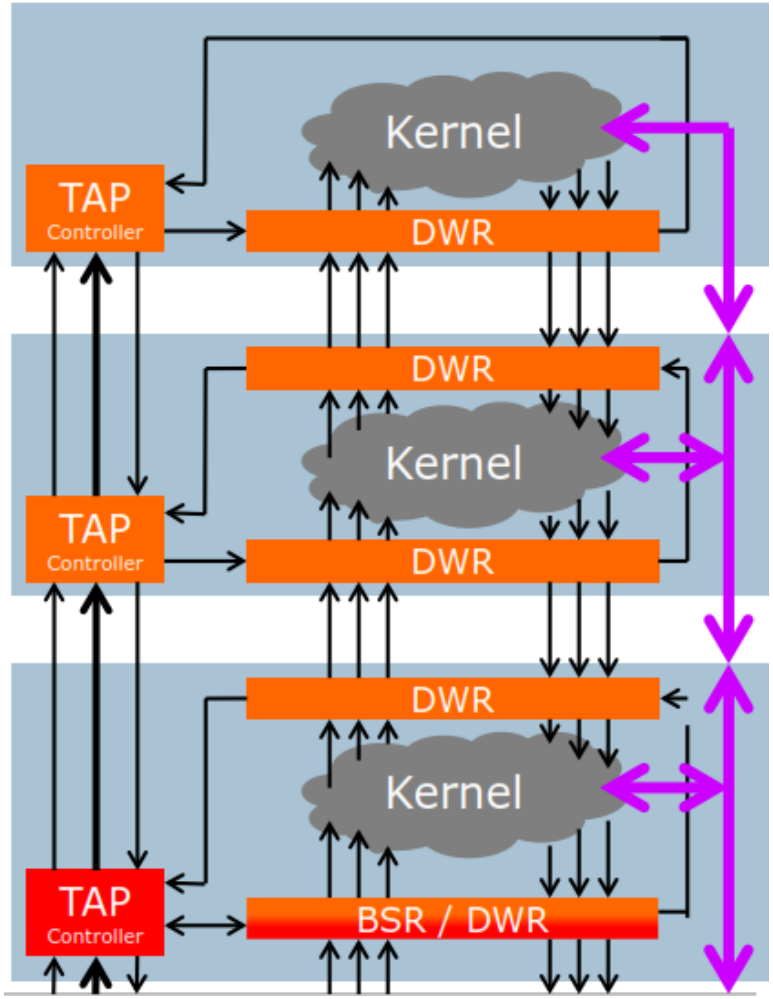




Deutsch, S.; Chakrabarty, K.; Panth, S. & Lim, S. K. TSV Stress-Aware ATPG for 3D Stacked ICs Proc. Asian Test Symp., 2012, 31-36

Design for Testability

- Multiple testing requirements
  - Faults and symptomatic impact (e.g., delay) of wires and TSVs
  - Pre-bond, mid-bond, post-bond and final package testing
- WIP IEEE P1838: DfT architecture
  - Support for different test stages
  - Compatibility across different chips and stacking parties
  - Test access based on IEEE 1149.1
  - Die wrapper register like IEEE 1500
  - Internal debugging via IEEE P1687



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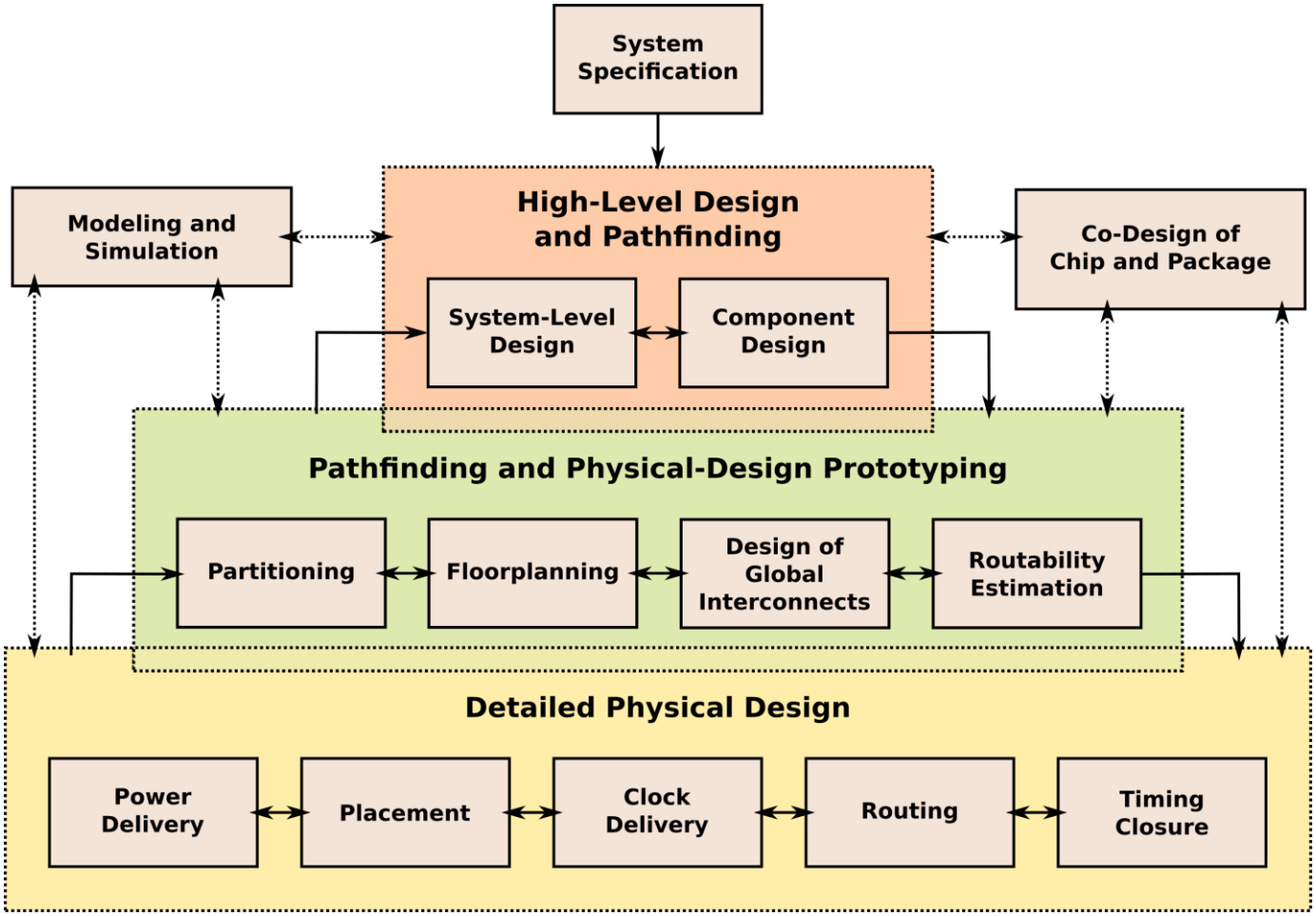
Outline

1. Motivation, Flavors, and Examples of 3D Chip Stacks
2. Classical Challenges – Aggravated but Solvable
3. Novel Design Challenges and Emerging Solutions
4. Summary Part 1 and Introduction Part 2

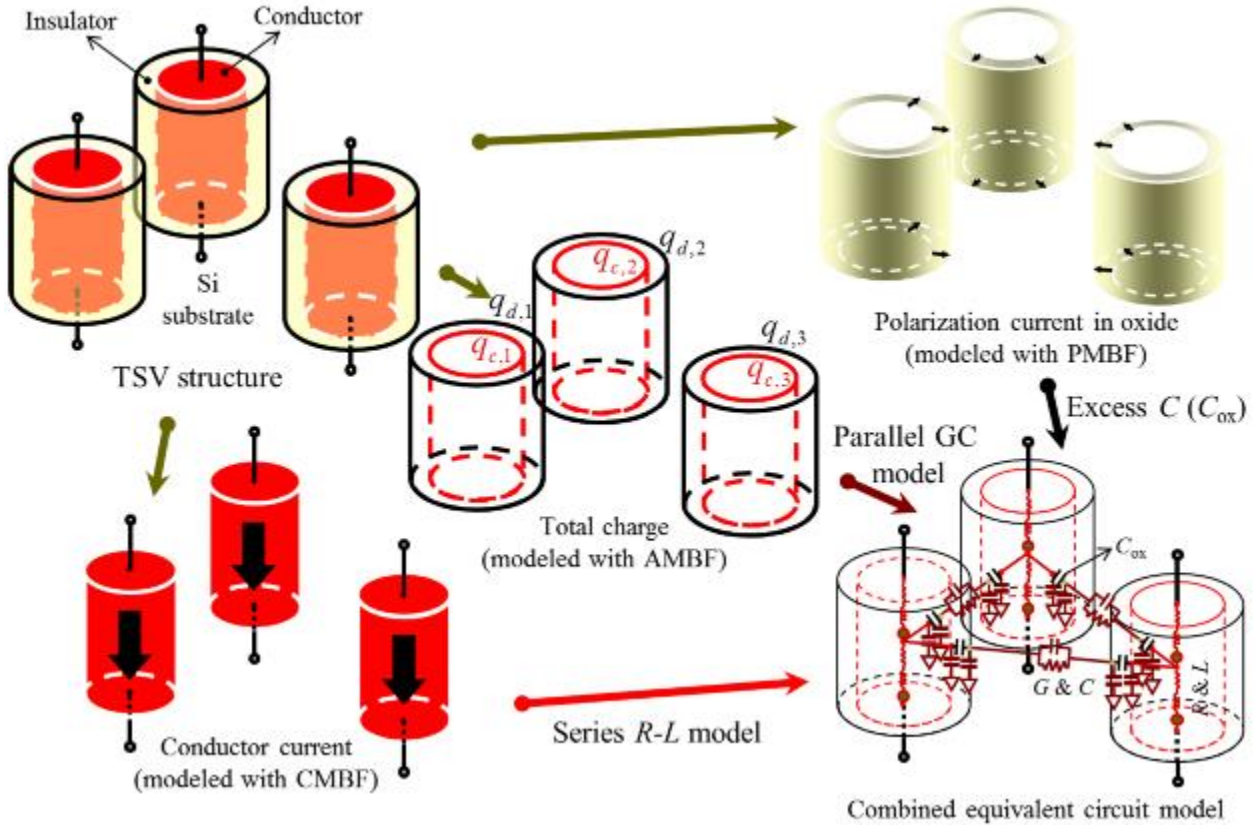
High-Level Design and Pathfinding

1. High-level design: derive components from high-level descriptions
2. Pathfinding: generate and evaluate "coarse" layouts



High-Level Design and Pathfinding

1. High-level design: derive components from high-level descriptions
   - Abstracted, modular components, e.g., RTL modules
   - Parameterizable multi-port components for TSVs, bumps, etc.



Martin, B.; Han, K. & Swaminathan, M. "A Path Finding Based SI Design Methodology for 3D Integration" Proc. Elec. Compon. Technol. Conf., 2014, 2124-2130

High-Level Design and Pathfinding

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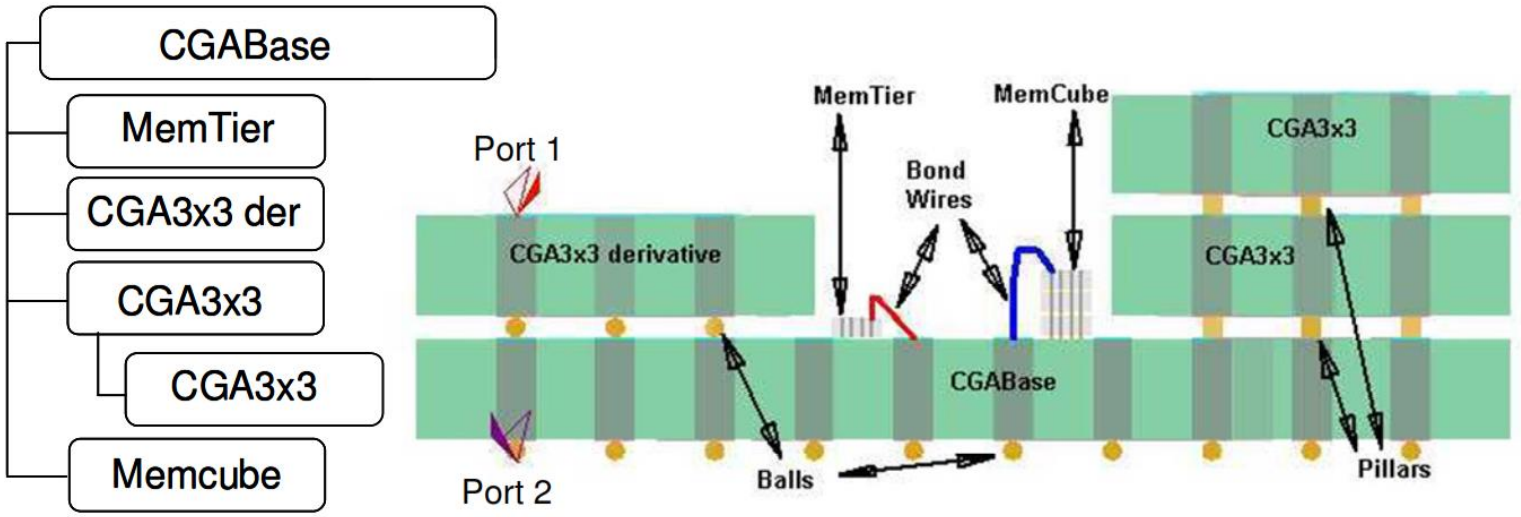
   - Abstracted, modular components, e.g., RTL modules
   - Parameterizable multi-port components for TSVs, bumps, etc.

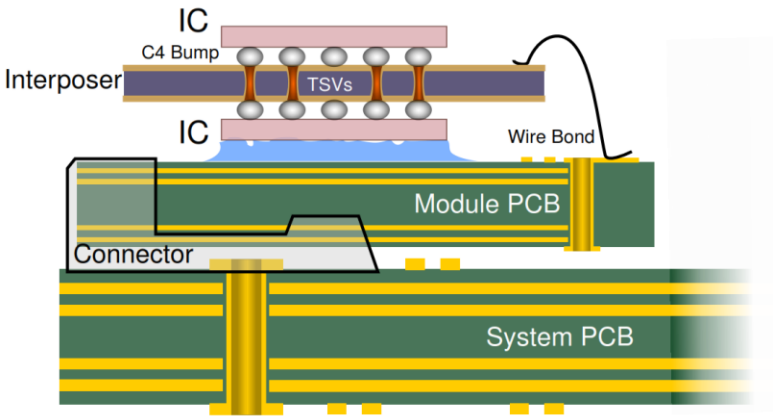
2. Pathfinding: generate and evaluate "coarse" layouts
   - "Plug-and-play" of components, explore stacking and technology options
   - Annotate stacks with design and simulation feedback



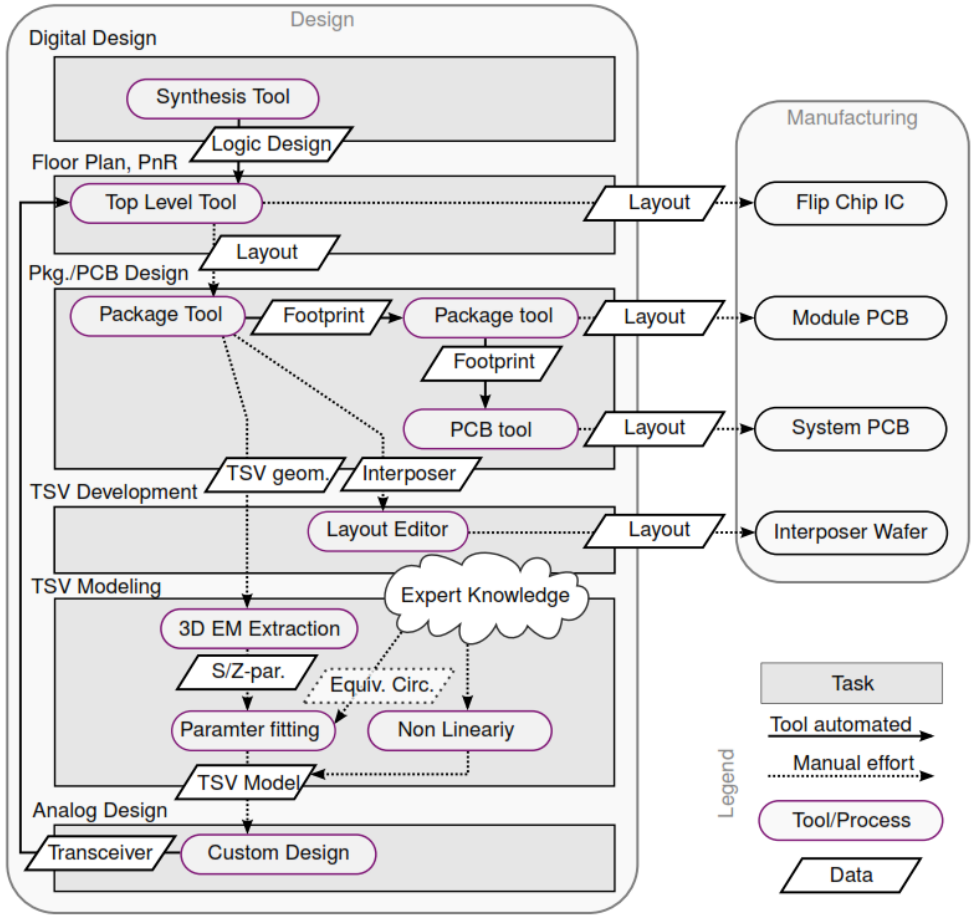
Martin, B.; Han, K. & Swaminathan, M. "A Path Finding Based SI Design Methodology for 3D Integration" Proc. Elec. Compon. Technol. Conf., 2014, 2124-2130

Chip-Package Co-Design

- Design of 3D stacks is team effort, possibly using different tools
- Interfaces require orchestration of physical and functional design



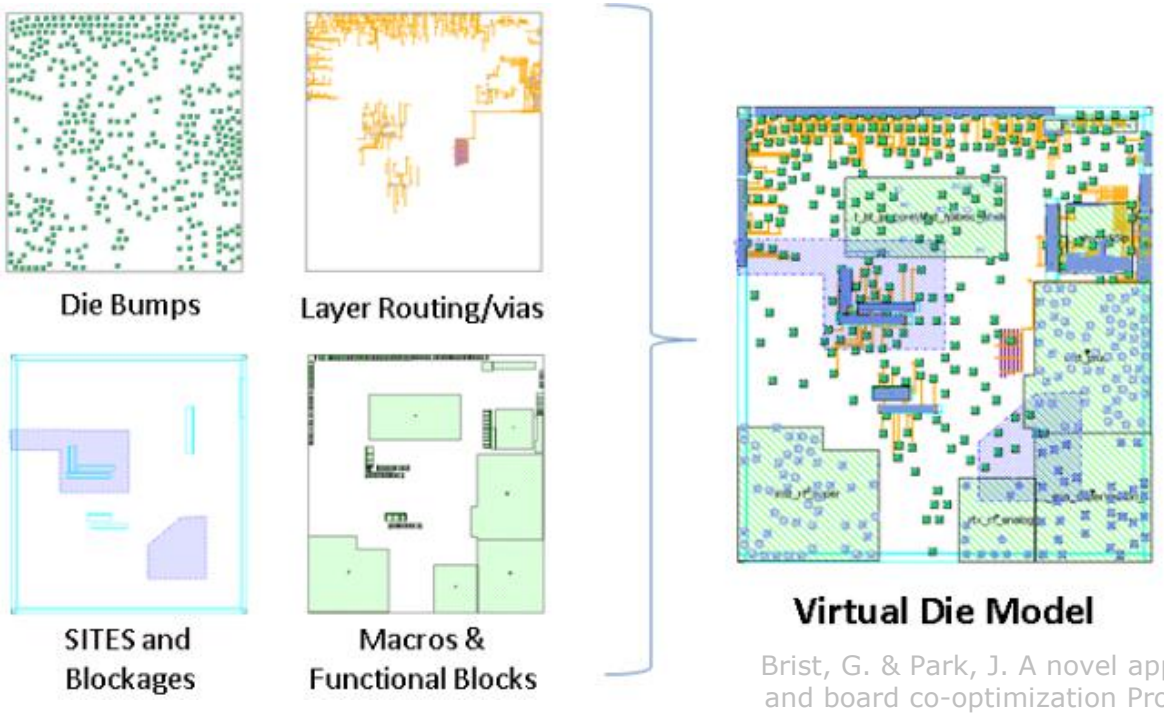
L. Cederström, "EDA environments for 3D chip stacks," in 3D Stacked Chips – From Emerging Processes to Heterogeneous Systems, I. A. M. Elfadel and G. Fettweis, Eds. Springer, 2016, ch. 9



Chip-Package Co-Design

- ⚠ Design of 3D stacks is team effort, possibly using different tools
- ⚠ Interfaces require orchestration of physical and functional design

- ➔ Use of a shared, unified database such as an ADK
- ➔ Design abstraction with data propagation; "virtual die model"

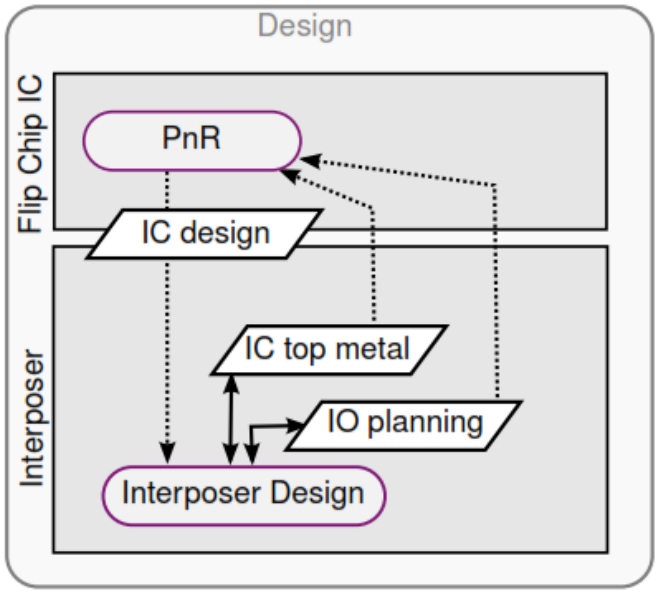


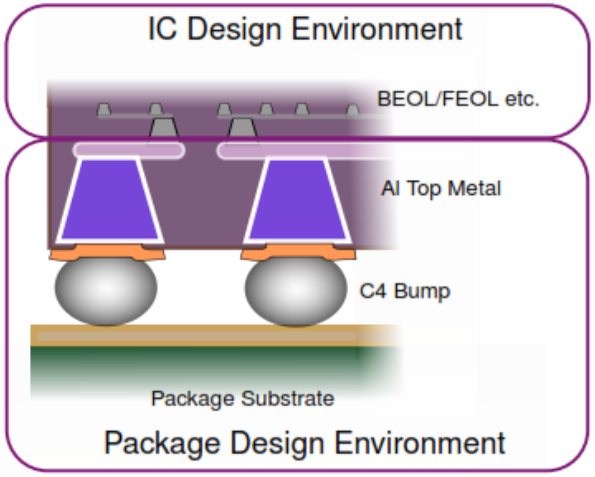
Brist, G. & Park, J. A novel approach to IC, package and board co-optimization Proc. Int. Symp. Quality Elec. Des., 2015, 512-518

Chip-Package Co-Design

- ⚠ Design of 3D stacks is team effort, possibly using different tools
- ⚠ Interfaces require orchestration of physical and functional design

- Use of a shared, unified database such as an ADK
- Design abstraction with data propagation; "virtual die model"
- Shared physical interfaces: designer and tools hand-over points





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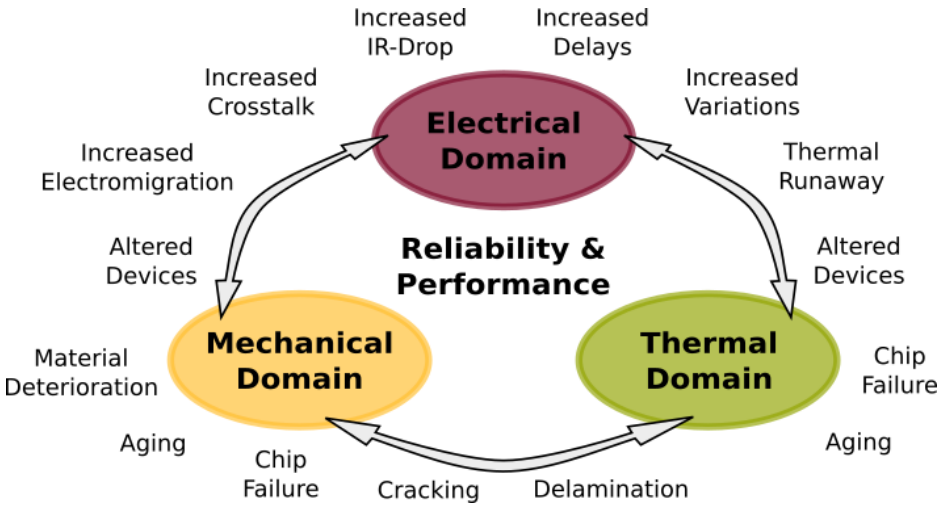
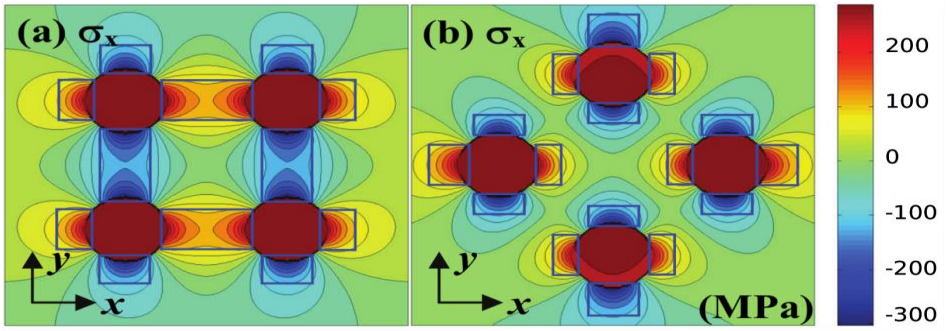
Multi-Physics Modeling and Simulation

- Strong coupling of physical domains in 3D stacks
  - For example, thermo-mechanical stress induced by TSVs
- Need for techniques crossing physical domains and design levels

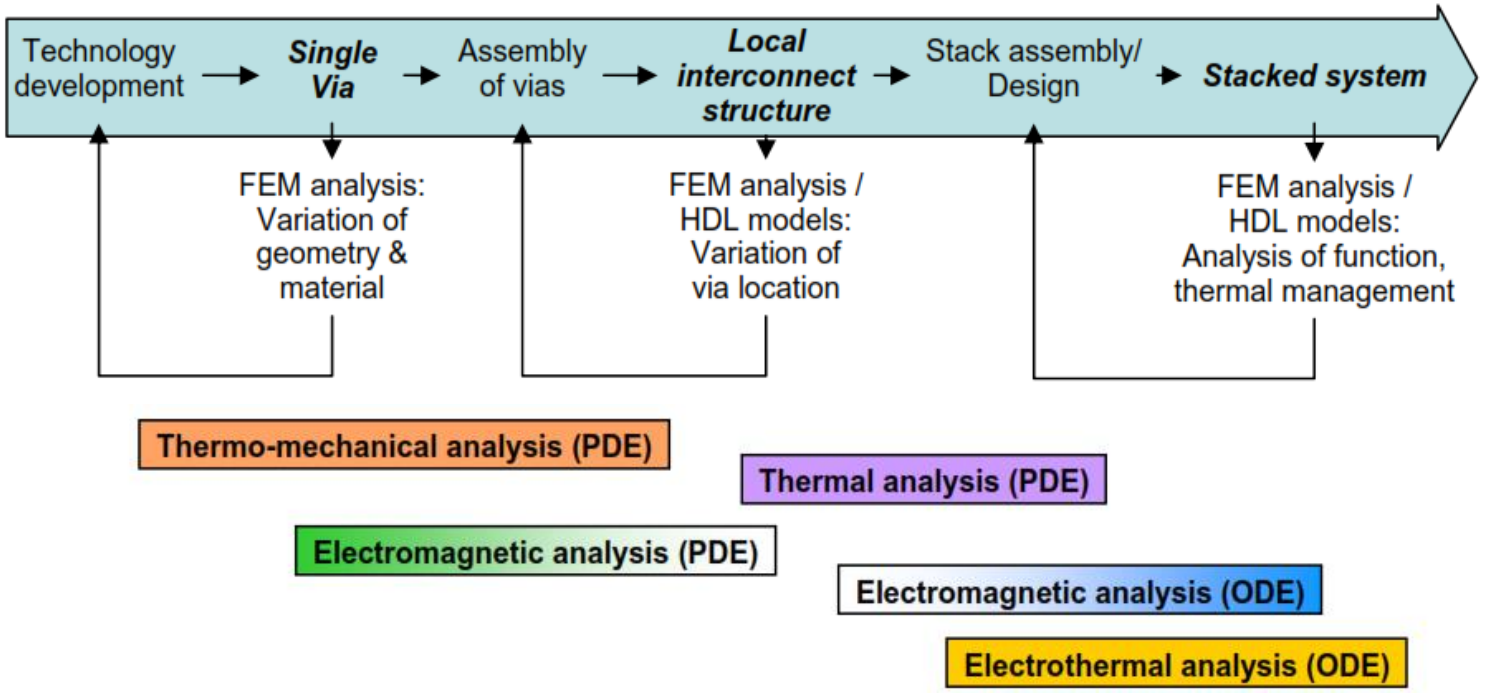




Lu, K. H. et al. Thermo-mechanical reliability of 3-D ICs containing through silicon vias Proc. Elec. Compon. Technol. Conf., 2009, 630-634

Multi-Physics Modeling and Simulation

- Need for techniques crossing physical domains and design levels
- Fine-grain, detailed to abstracted, high level modeling and simulation



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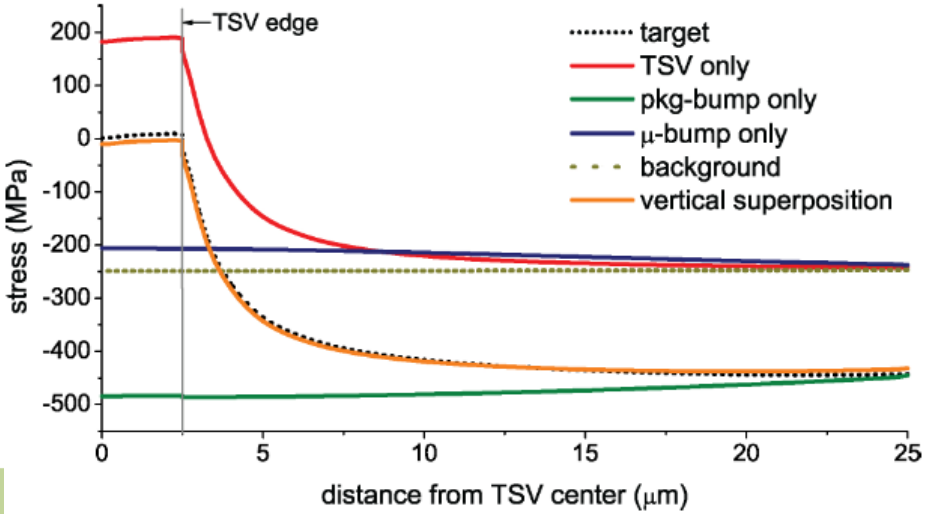
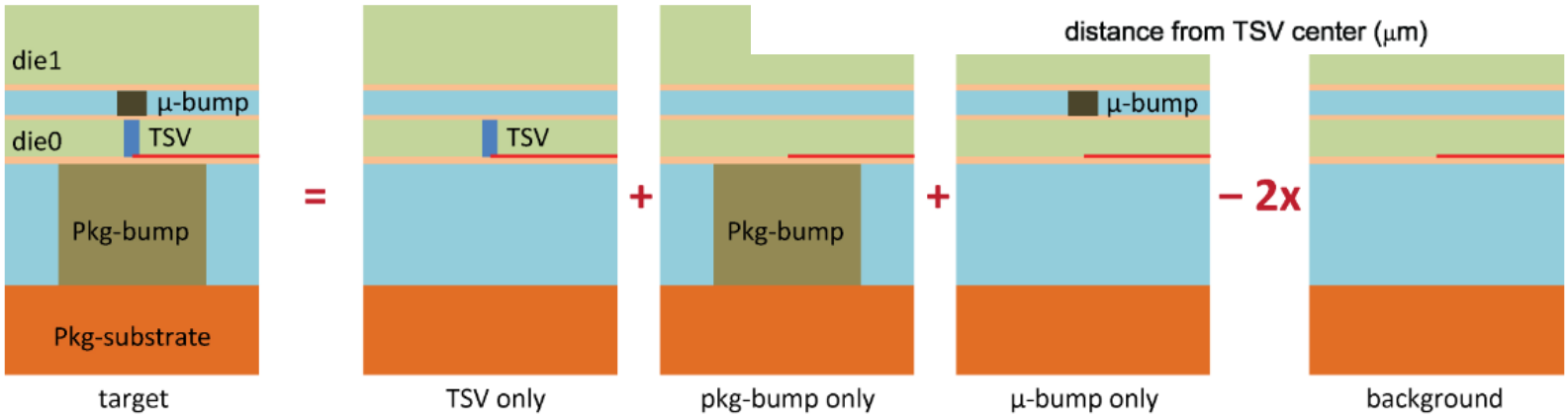
Multi-Physics Modeling and Simulation

- Need for techniques crossing physical domains and design levels
- Fast analytical models, here with local and global superposition

Jung, M.; Pan, D. Z. & Lim, S. K. "Chip/Package Mechanical Stress Impact on 3-D IC Reliability and Mobility Variations" Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 1694-1707





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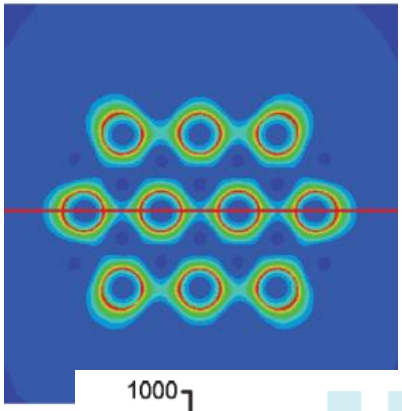

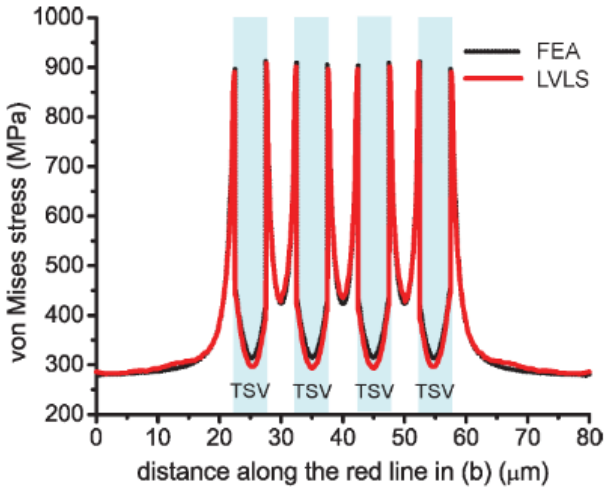

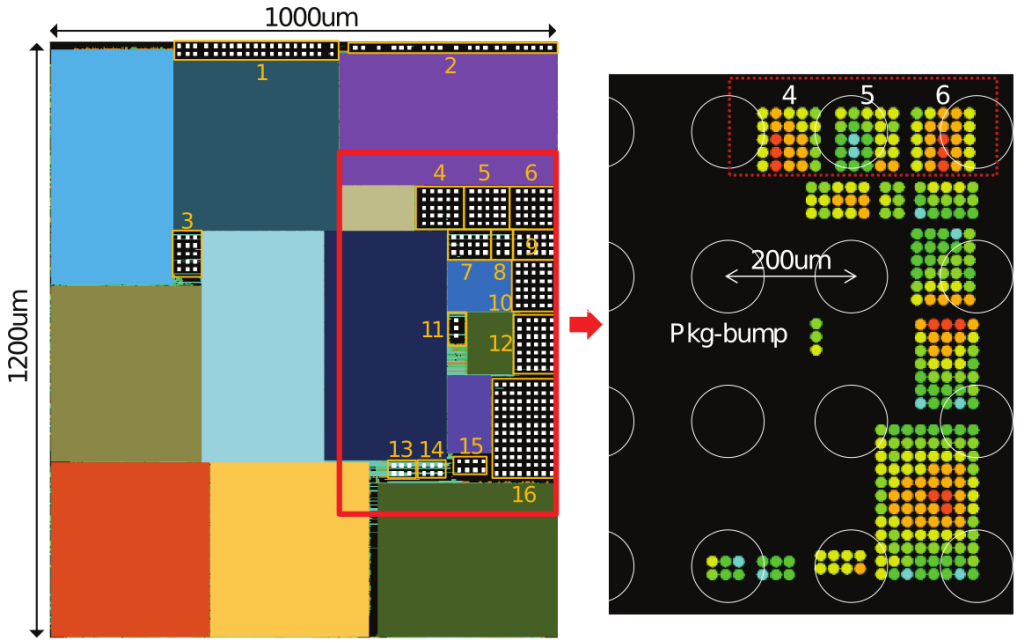

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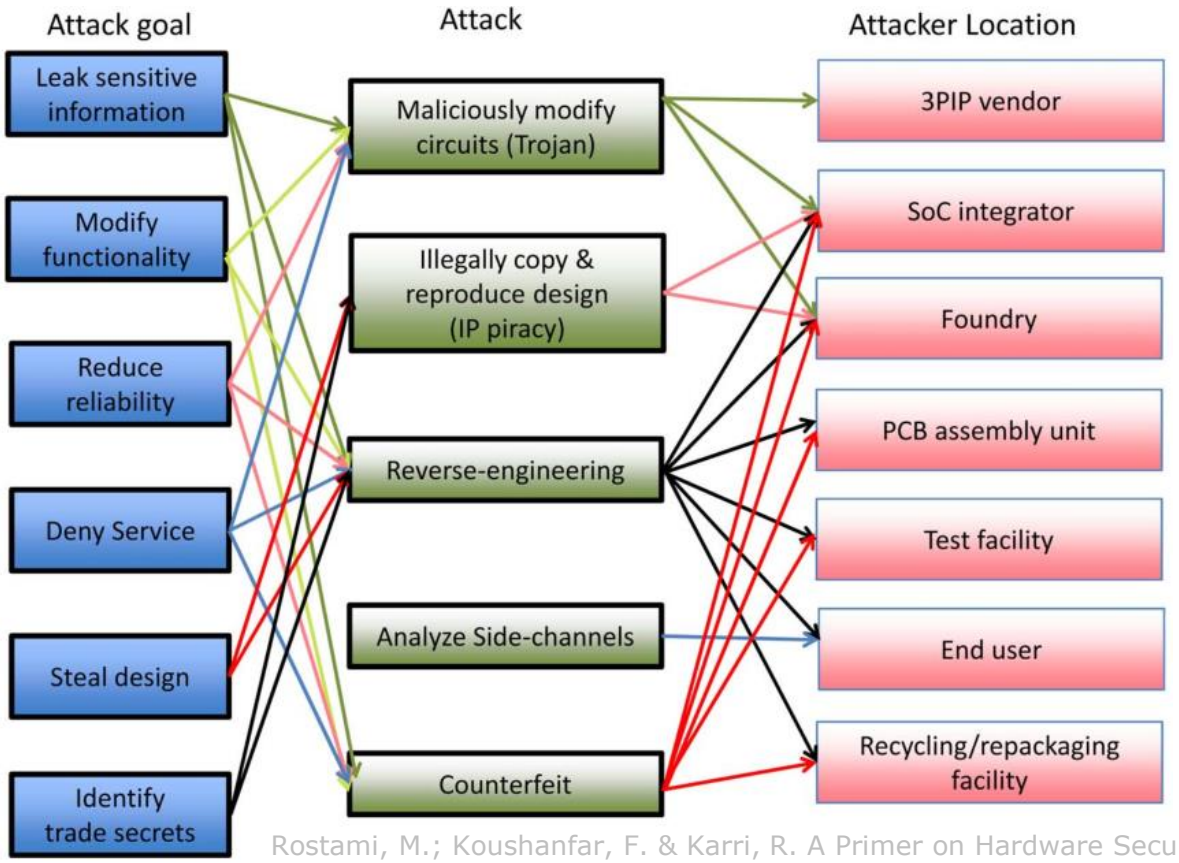
Security and Trustworthiness

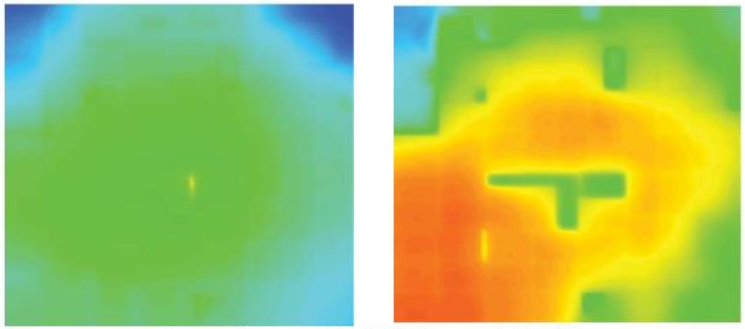
- Hardware as root of trust; many potential attacks and attackers
- 3D chips: more distributed design and manufacturing landscape
  - Potentially higher threat exposure than 2D chips



Rostami, M.; Koushanfar, F. & Karri, R. A Primer on Hardware Security: Models, Methods, and Metrics Proc. IEEE, 2014, 102, 1283-1295

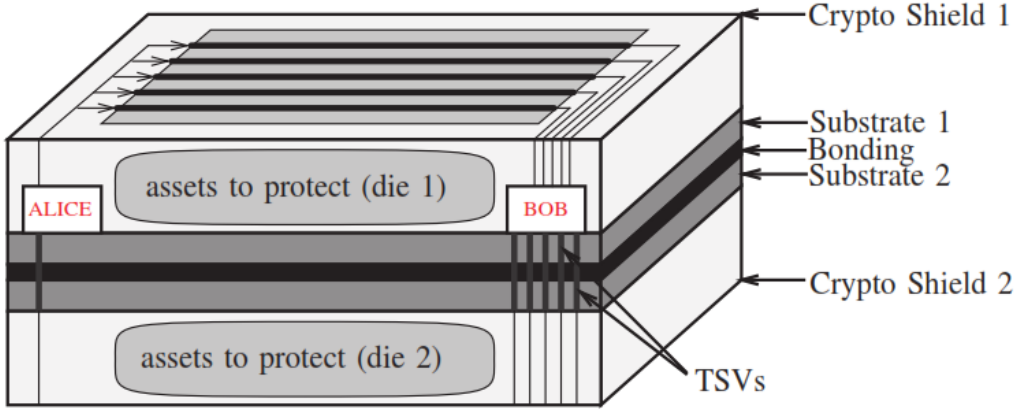
Security and Trustworthiness

- 3D chips: benefits on physical and design level for security
- Nature of vertically stacked dies/layers and high integration density
  - Complicates side-channel analysis and reverse engineering



thermal maps for TSV-based 3D IC

Samal, S. K.; Panth, S.; Samadi, K.; Saeidi, M.; Du, Y. & Lim, S. K. Adaptive Regression-Based Thermal Modeling and Optimization for Monolithic 3-D ICs Trans. Comp.-Aided Des. Integr. Circ. Sys., 2016, 35, 1707-1720

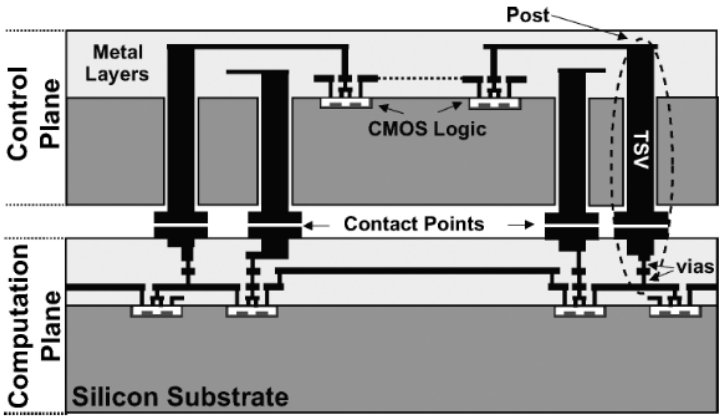


Cioranesco, J. M.; Danger, J. L.; Graba, T.; Guilley, S.; Mathieu, Y.; Naccache, D. & Ngo, X. T. Cryptographically secure shields Proc. Int. Symp. Hardware-Orient. Sec. Trust, 2014, 25-31

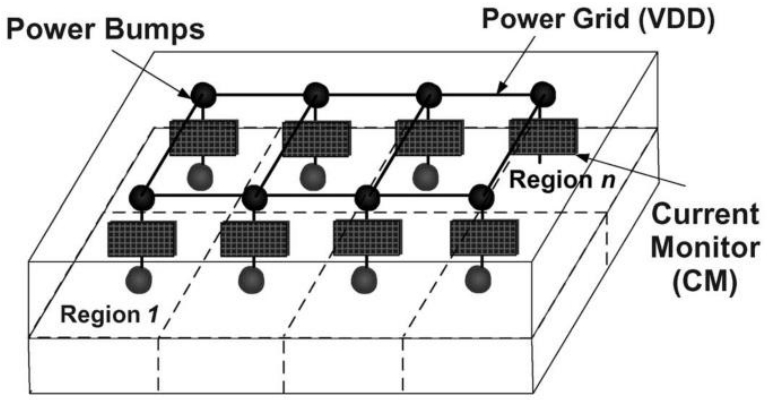
Security and Trustworthiness

- 3D chips: benefits on physical and design level for security

- Nature of vertically stacked dies/layers and high integration density
  - Complicates side-channel analysis and reverse engineering
  - Supports trusted monitors and trusted system integration



Valamehr et al., A 3-D Split Manufacturing Approach to Trustworthy System Development Trans. Comp.-Aided Des. Integr. Circ. Sys., 2013, 32, 611-615



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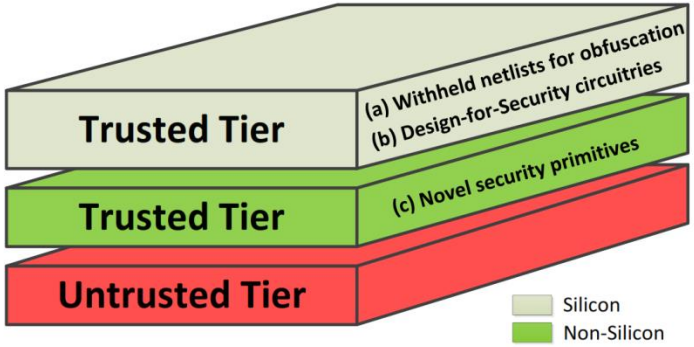

Xie et al., Security and Vulnerability Implications of 3D ICs Trans. Multi-Scale Comp. Sys., 2016, 2, 108-122

Security and Trustworthiness

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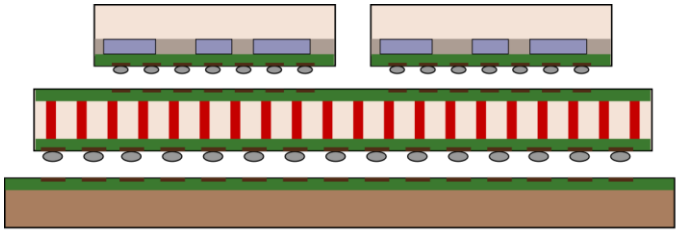
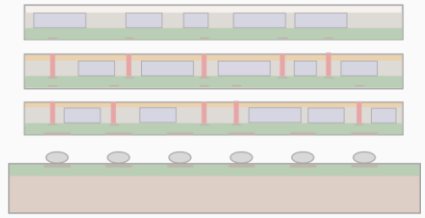
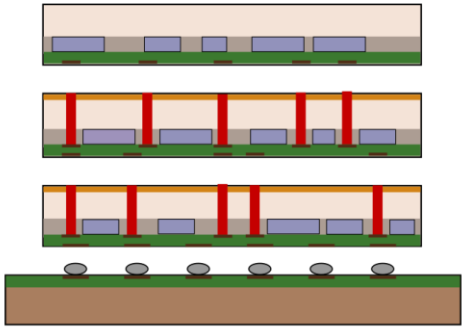
  - Supports trusted monitors and trusted system integration
  - Supports concept of split manufacturing



Interposer Stack



Monolithic 3D IC



TSV-based 3D IC

Security and Trustworthiness

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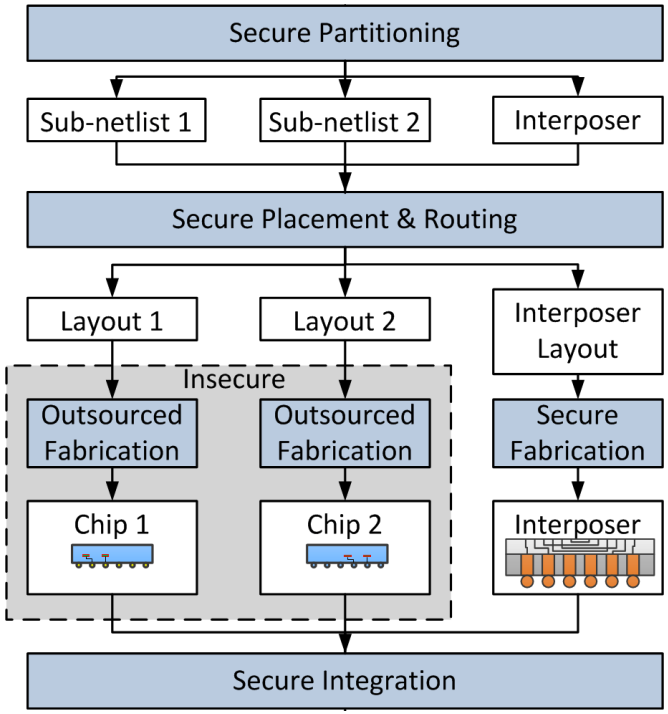

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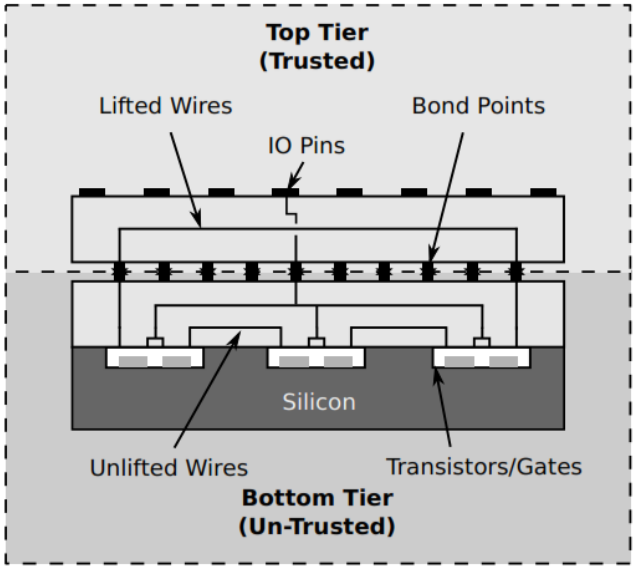

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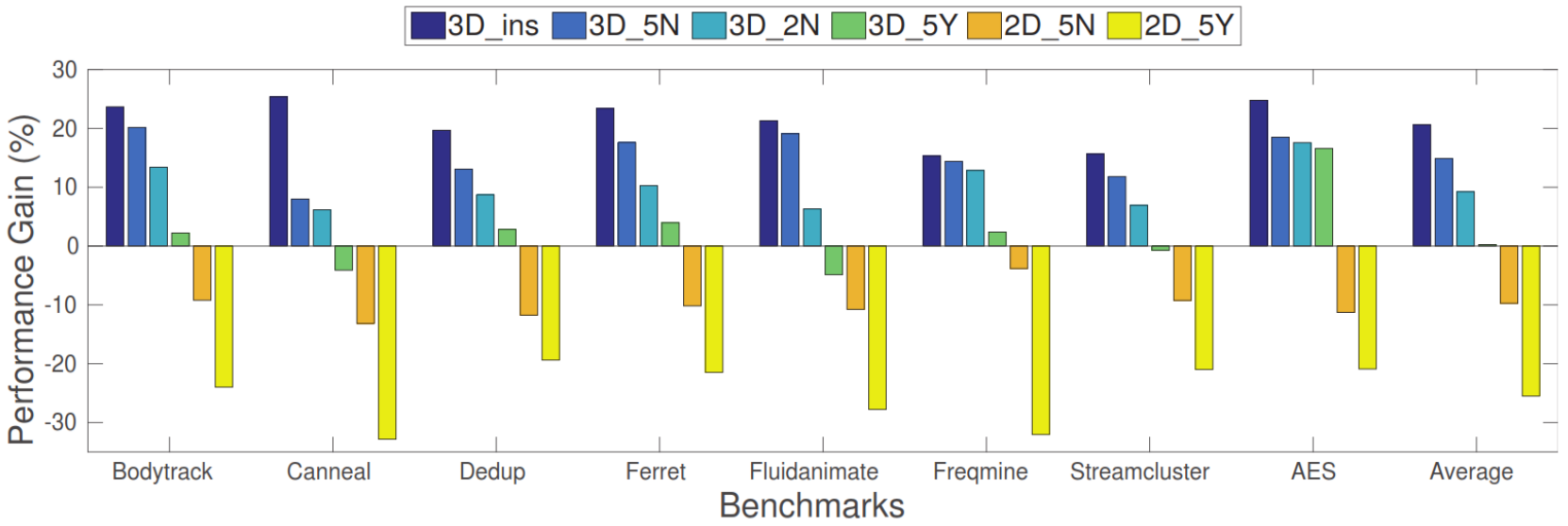
Security and Trustworthiness

- 3D chips: benefits on physical and design level for security

- Nature of vertically stacked dies/layers and high integration density
- Higher performance and bandwidth: enable costly security primitives
  - Memory protection, e.g., random eviction and heterogeneous latencies



Bao, C. & Srivastava, A. 3D Integration: New opportunities in defense against cache-timing side-channel attacks Proc. Int. Conf. Comp. Des., 2015, 273-280

Security and Trustworthiness

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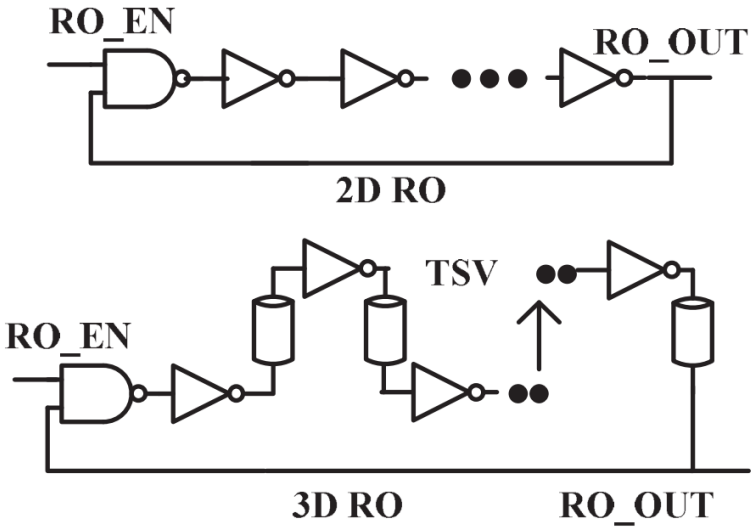
- Higher performance and bandwidth: enable costly security primitives
- Heterogeneous components for security primitives, e.g., TSV-PUF



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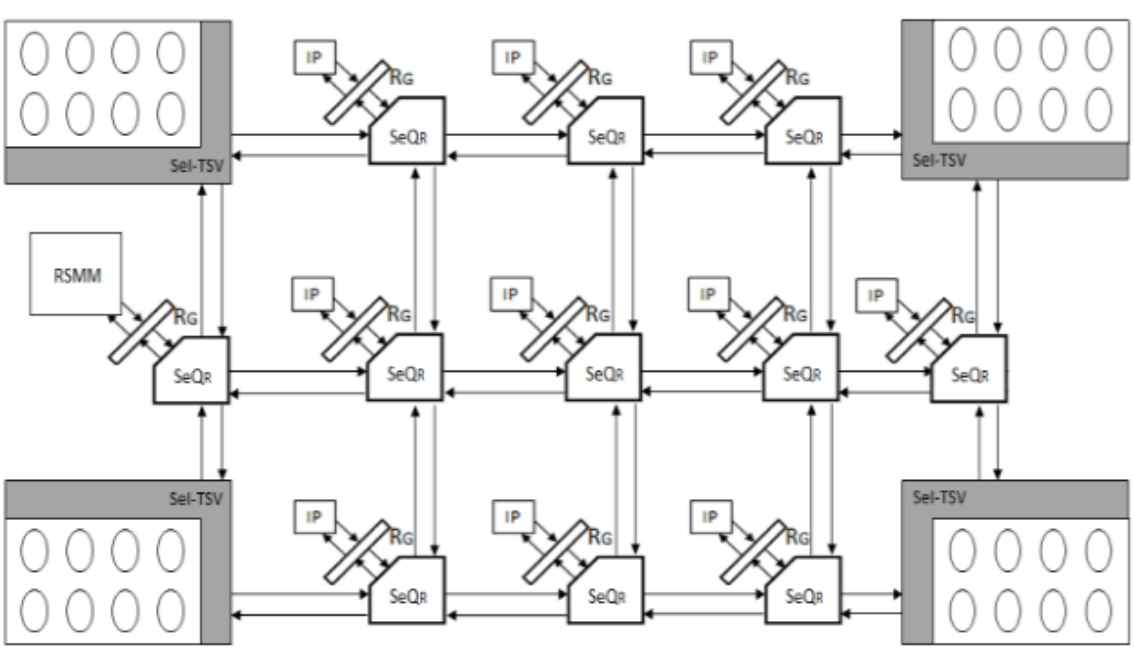
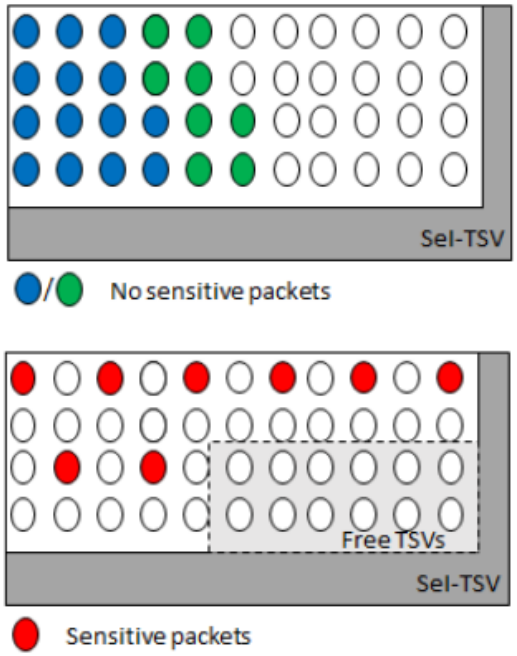
Security and Trustworthiness

- 3D chips: threats/risks on physical and design level for security
- Malicious TSV coupling or manufacturing: denial of service, data leakage, data injection
  - TSV shielding and TSV testing
  - 3D NoC with access control and decoupled, redundant TSV transmission





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Security and Trustworthiness

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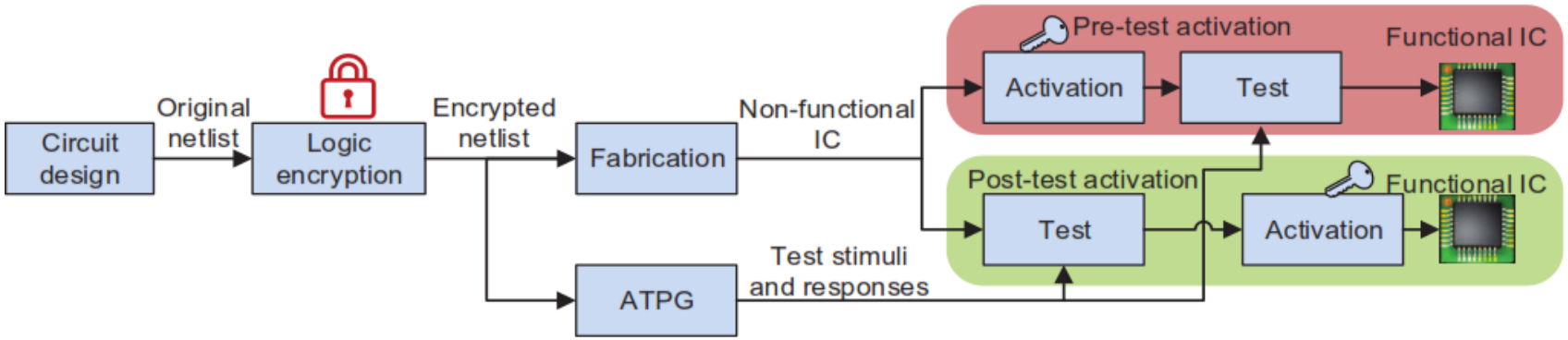
- Malicious TSV coupling or manufacturing: denial of service, data leakage, data injection
- Malicious access to modules "buried too deep in stack" via testing
  - Recent progress in design for secure testability, e.g., to protect IP
  - OSAT shall access and test only encrypted dies



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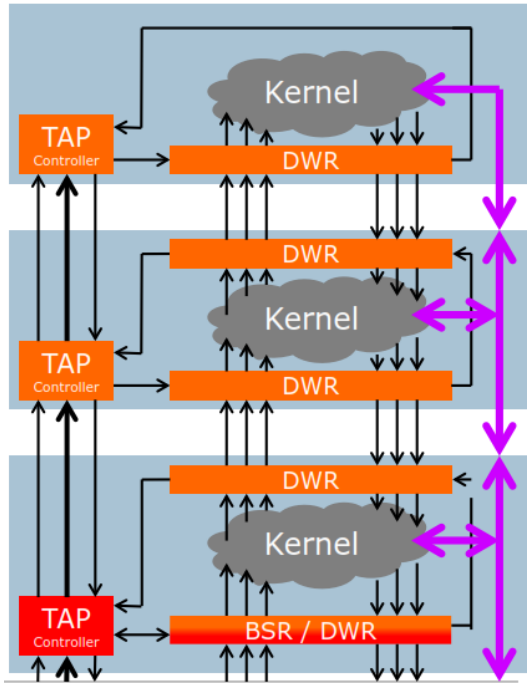
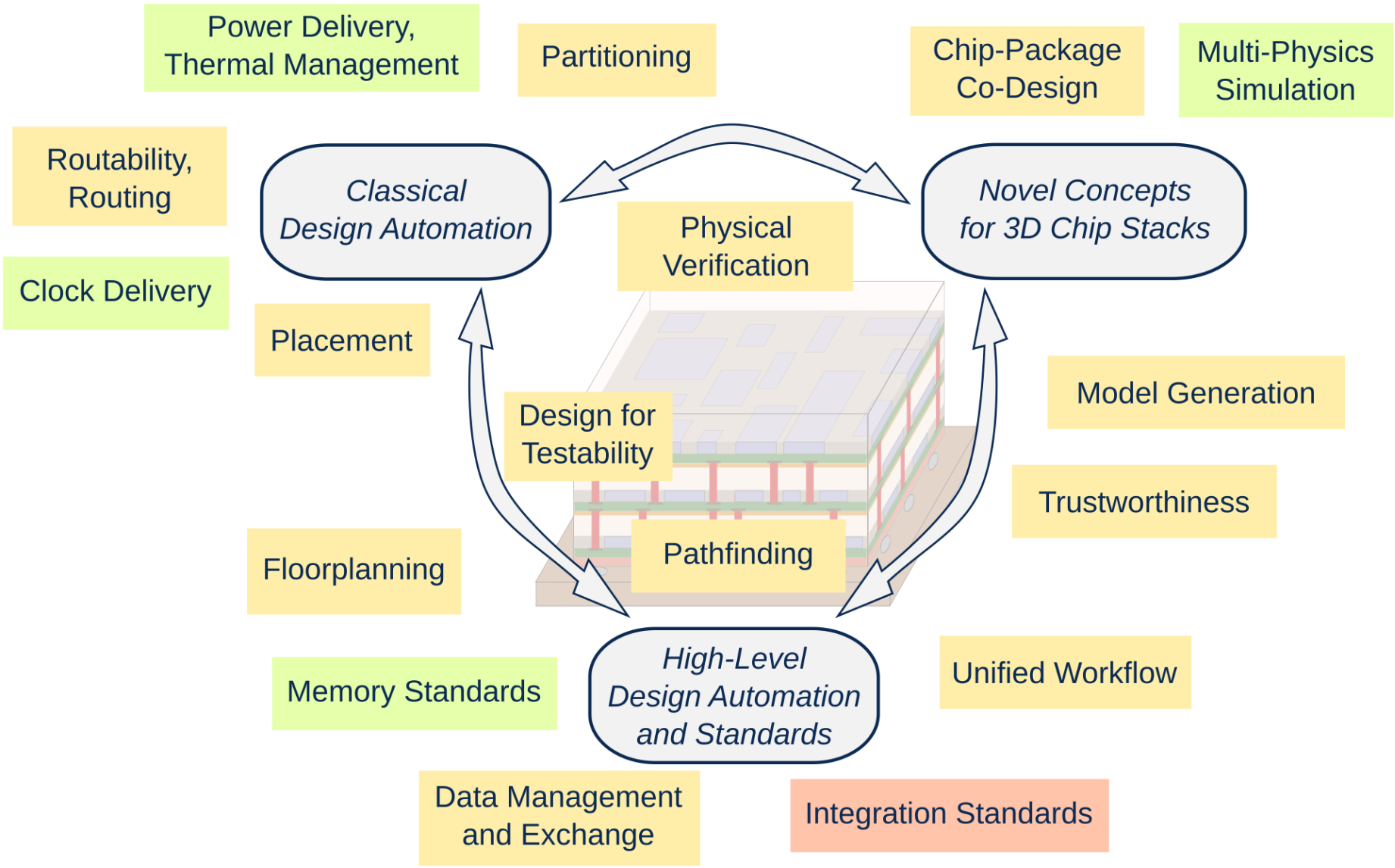
  - Recent progress in design for secure testability, e.g., to protect IP
  - OSAT shall access and test only encrypted dies
  - Secure testing to be extended for 3D stacks
  - Test access based on IEEE 1149.1
  - Die wrapper register like IEEE 1500
  - Internal debugging via IEEE P1687



Marinissen, E. J. "Status Update of IEEE Std P1838" Proc. Int. Workshop Testing 3D Stack. Integr. Circ., 2014

Outline

1. Motivation, Flavors, and Examples of 3D Chip Stacks
2. Classical Challenges – Aggravated but Solvable
3. Novel Design Challenges and Emerging Solutions
4. Summary Part 1 and Introduction Part 2


Power Delivery, Thermal Management
Partitioning
Chip-Package Co-Design
Multi-Physics Simulation
Routability, Routing
Classical Design Automation
Novel Concepts for 3D Chip Stacks
Physical Verification
Clock Delivery
Placement
Model Generation
Design for Testability
Trustworthiness
Floorplanning
Pathfinding
Memory Standards
High-Level Design Automation and Standards
Unified Workflow
Data Management and Exchange
Integration Standards

Further Reading Material

- See handout: J. Knechtel, J. Lienig "Physical Design Automation for 3D Chip Stacks – Challenges and Solutions," Proc. ISPD'16, pp. 3-10, April 2016 http://dx.doi.org/10.1145/2872334.2872335

- H. Reiter, eda2asic and the Electronic System Design Alliance "Multi-die IC User Guide 2016.6. 1" http://www.esd-alliance.org/initiatives/committees/SystemScaling/MultiDieICDesign_2016.6

- Elfadel, I. A. M. & Fettweis, G. (Eds.) "3D Stacked Chips – From Emerging Processes to Heterogeneous Systems Springer," 2016, http://www.springer.com/us/book/9783319204802

- Lim, S. K. "Design for High Performance, Low Power, and Reliable 3D Integrated Circuits Springer," 2013, http://dx.doi.org/10.1007/978-1-4419-9542-1