

X-Volt: Joint Tuning of Driver Strengths and Supply Voltages Against Power Side-Channel Attacks

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ABSTRACT

Power side-channel (PSC) attacks are well-known threats to sensitive hardware like advanced encryption standard (AES) crypto cores. Given the significant impact of supply voltages (VCCs) on power profiles, various countermeasures based on VCC tuning have been proposed, among other defense strategies. Driver strengths of cells, however, have been largely overlooked, despite having direct and significant impact on power profiles as well.

For the first time, we thoroughly explore the prospects of jointly tuning driver strengths and VCCs as novel working principle for PSC-attack countermeasures. Toward this end, we take the following steps: 1) we develop a simple circuit-level scheme for tuning; 2) we implement a CAD flow for design-time evaluation of ASICs, enabling security assessment of ICs before tape-out; 3) we implement a correlation power analysis (CPA) framework for thorough and comparative security analysis; 4) we conduct an extensive experimental study of a regular AES design, implemented in ASIC as well as FPGA fabrics, under various tuning scenarios; 5) we summarize design guidelines for secure and efficient joint tuning.

In our experiments, we observe that runtime tuning is more effective than static tuning, for both ASIC and FPGA implementations. For the latter, the AES core is rendered $>11.8x$ (i.e., at least 11.8 times) as resilient as the untuned baseline design. Layout overheads can be considered acceptable, with, e.g., around +10% critical-path delay for the most resilient tuning scenario in FPGA.

We release source codes for our methodology, as well as artifacts from the experimental study in [13].

CCS CONCEPTS

• **Security and privacy** → **Side-channel analysis and countermeasures**; • **Hardware** → **Power and energy**; *Methodologies for EDA; Integrated circuits; Reconfigurable logic and FPGAs.*

KEYWORDS

Power side-channel (PSC), correlation power analysis (CPA), driver strength, supply voltage, application-specific integrated circuit

(ASIC), field-programmable gate array (FPGA), computer-aided design (CAD), power simulation, power measurement

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1 INTRODUCTION

Background: To protect sensitive data handled within integrated circuits (ICs), the use of cryptographic (crypto) modules is widely adopted. Such modules are based on provably secure algorithms for encryption/decryption of data. Still, once attackers have access to ICs, direct or even only remote/indirect, they can monitor the runtime behaviour and physical interactions with the environment, e.g., via measurements (direct) or via software interfaces to embedded sensors (remote/indirect). Such observations enable so-called *side-channel attacks* [22], which can serve to infer the secret key used for crypto modules, etc.

Limitation of Prior Art: Power side-channel (PSC) attacks are a well-known and effective type of side-channel attacks [3, 18]. Thus, a plethora of PSC countermeasures have been proposed, e.g., masking and hiding [12], voltage switching [8, 21], noise injection [2], etc. Given the direct impact of supply voltages (VCCs) on power profiles, various countermeasures are based on some kind of VCC tuning. Driver strengths of cells, however, have been largely overlooked, despite significant impact on power profiles as well.

Motivation – Impact of Tuning: In Fig. 1, we show the power profiles for a regular advanced encryption standard (AES) core when operating the core under different driver strengths and VCCs. We observe that dynamic tuning—that is, runtime reconfiguration of switching drivers and/or utilized VCCs—results in profiles that largely overlap with the baseline profiles.

Such interspersions of power profiles as shown in Fig. 1 represents a major challenge for PSC attacks as follows. Assuming the same text is processed, using the same key, but under varying tuning settings, a large number of different power values can arise within the resulting power profiles. The reverse also applies: for the same power value observed, a large range of different possible texts and/or different possible keys may be underlining of the crypto

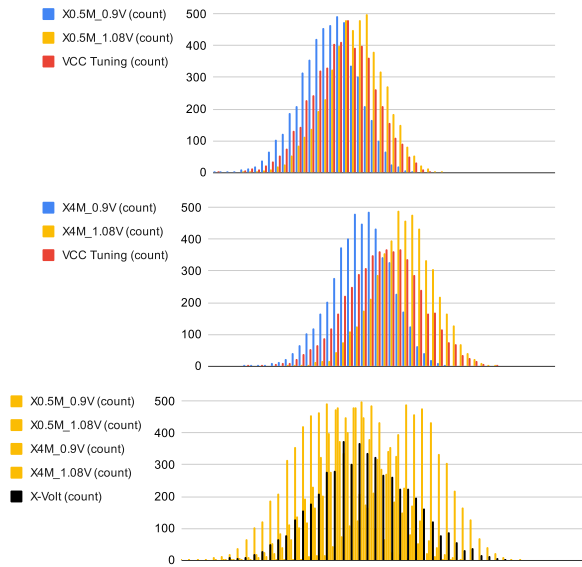


Figure 1: Motivational example for the impact of tuning. Histograms of power profiles, for a regular AES core implemented in a GlobalFoundries 55nm technology. The two “VCC Tuning” scenarios (top) cover two different cases of driver strengths assigned to all AES flip-flops, demonstrating two aspects of tuning: (i) VCC tuning results in general in power profiles (red) that largely overlap with the baseline profiles (blue and yellow) and (ii) the particular overlap of profiles depends on the driver strengths. The “X-Volt” scenario (bottom) demonstrates how joint tuning of driver strengths and VCCs renders the profile more interspersed.

computation. Naturally, such ambiguity can be quite misleading for analytical models that are at the heart of PSC attacks.

Contributions: As indicated, prior art did overlook the potential of jointly tuning driver strengths and VCCs in general, let alone for dynamic runtime modes. In this work, we address this gap. We build up a multi-part methodology to thoroughly study various scenarios for joint tuning of driver strengths and VCCs, applicable for ASIC as well as FPGA fabrics.

We take the following steps:

- (1) We develop a simple circuit-level scheme for tuning, which is applicable for ASIC as well as FPGA fabrics.
- (2) We implement a CAD flow for design-time evaluation of ASIC power profiles at runtime, enabling proper security assessment of ICs before tape-out.
- (3) We implement a correlation power analysis (CPA) framework for a thorough and comparative security analysis of tuning.
- (4) As key contribution of this work, we conduct an extensive experimental study of a regular AES design, implemented in ASIC as well as FPGA fabrics, under various tuning scenarios.
- (5) Finally, we derive design guidelines for secure and efficient joint tuning in ASIC and FPGA fabrics.

We emphasize that our work is not meant to compete with or replace prior art for PSC countermeasures, but rather to extend the landscape of available options at a foundational level. Joint tuning

can be either used as stand-alone measure, as it is done in this work at hand, or to further complement prior countermeasures.

Findings: In our experimental study, we observe the following.

- (1) For the ASIC design based on a GlobalFoundries 55nm technology, we find that a) static design-time tuning may improve the resilience, but only to limited degrees, and can sometimes even counteract it. In contrast, b) dynamic runtime tuning always renders the AES core more resilient, namely up to 235% as resilient as the untuned baseline.¹
- (2) We confirm our key finding—that dynamic runtime tuning is more effective—in the field, using a Sakura-X FPGA board based on a 28nm technology. Here, the AES core is rendered >11.8x (i.e., at least 11.8 times) as resilient.
- (3) Regarding trade-offs for resilience versus layout overheads, we find them reasonable with, e.g., $\approx 10\%$ impact on critical-path delay for the most resilient FPGA tuning scenario.

Release: We release source codes for our methodology, as well as empirical artifacts, in [13].

2 BACKGROUND

2.1 Side-Channel Attacks

Side-channel attacks infer sensitive information by observing and analysing physical channels established by ICs during operation [22]. These channels are leaking some kind of information due to the basic workings of the underlying circuitry, but also due to micro-architectural implementation decisions. For the latter, e.g., timing behavior and speculative execution in modern processors has been demonstrated as vulnerability [14]. For the classical PSC, e.g., it is well-known that the secret key for AES can be inferred by analysing the data-dependent power consumption [3, 18].

Different PSC attacks have been demonstrated, like correlation power analysis (CPA) [3], mutual information analysis [6], or machine learning-based techniques [15]. Furthermore, there are more generic, analytical approaches like test vector leakage assessment (TVLA) [17], architecture correlation [20], etc.

Without loss of generality (w/o.l.o.g.), we focus on the CPA attack in this work. CPA is well-established and used widely throughout the literature. CPA is effective, e.g., CPA requires on average fewer traces than DPA [1, 3, 5]. More details are explained in Sec. 4.3.

2.2 Prior Art for Countermeasures

Various countermeasures against PSC attacks have been proposed over the years, including masking and hiding [12], voltage switching [8, 21], noise injection [2], etc. Essentially, these countermeasures seek to de-correlate the observable power consumption from the sensitive crypto operations.

More specifically, masking and hiding approaches do restructure and reimplement the design such that sensitive operations are decomposed/split at the functional as well as the circuit level. However, the overheads for such schemes can scale quadratically with the related security requirements, making efficient implementations quite challenging [7]. Voltage switching can be enabled by,

¹This quantitative finding is conservative, as it is based on design-time evaluation without impact of layout effects, let alone measurement noises. Thus, for attacks on real hardware, we can assume a larger impact—we confirm this via FPGA implementation.

e.g., multiple voltage domains and related control circuitry, or by integrated voltage regulators (IVRs) [8]. Note that IVRs are commonly available in modern IC designs, as they can enable significant power savings. Noise injection, like interposing random data into redundantly designed register paths [2], is effective but can also incur considerable area and power costs.

Driver strengths, while directly impacting power profiles and thus the resilience against PSC attacks, have been largely overlooked in prior art. To the best of our knowledge, “Karna” [19] is the only recent work that has explicitly studied the role of driver strengths (known as gate sizes in [19]), along with VCCs and threshold voltages. The authors found that varying strengths has also varying impact on the resilience. Tuning of these parameters, however, was limited to static design-time tuning for ASICs.²

3 THREAT MODEL

We consider a stringent threat model for PSC attacks as follows.

Attackers can only act as passive observers. That is, attackers do have direct/indirect access to the ASIC or FPGA, but only for monitoring the power consumption and the cipher-texts. Attackers have no control of plain-texts and no control over the power supply.

We assume that attackers are fully aware of our countermeasure’s working principle. However, given that operation of the tuning implementation (Sec. 4.1) is randomized, randomly switching between different tuning scenarios, and given that power profiles for different tuning scenarios are considerably interspersed (recall Fig. 1), attackers cannot ascertain the specific driver strength and VCC underlying for any particular point in time or operation. Accordingly, attackers cannot explicitly separate the multiple distributions underlying the power profiles, which will hinder any analytical attack model.

4 METHODOLOGY

4.1 Runtime Tuning of Driver Strengths, VCCs

This section outlines implementation options for the key idea of our work, that is dynamic tuning of driver strengths and VCCs. Other options could be devised as well, e.g., toward a more optimized, cell-level integration of different driver strengths.

Registers in general, and those holding AES texts in particular, are most relevant for PSC attacks, since they build up considerable correlation between the processed data and the observable power consumption; see also Sec. 4.2 and Sec. 4.3. Thus, for both ASIC and FPGA implementations, we focus on registers.

Implementation in ASICs: For static driver-strength tuning during design time, we simply reconfigure the strength for each register of choice. We randomly select, w/o.l.o.g., either the lowest or highest available strength. To maintain the selected strengths throughout the design flow, we mark these register as “don’t touch.”

For dynamic tuning of driver strengths, we implement tunable registers as outlined in Fig. 2 and described next. For each register of choice, we replace it with a pair of registers, again w/o.l.o.g. one with lowest and one with highest available strengths, respectively.

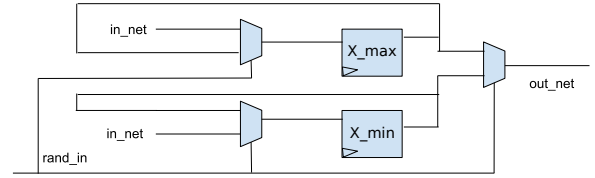


Figure 2: Implementation principle of dynamic tuning of driver strengths.

Register pairs are marked as “don’t touch” such that the strengths are maintained. We reconnect the original register’s nets through two additional multiplexers (MUXes) such that only one of the two registers is randomly selected for operation at a time; the other register is feeding back itself the current data, i.e., is guaranteed to not toggle at that point in time.

For both tuning cases, we re-synthesize afterwards, to meet timing and electrical constraints. For design-time evaluation, VCC tuning is mimicked through cell and library configurations.³

Implementation in FPGAs: Note that common FPGA fabrics do not provide the option for reconfiguring cell driver strengths. However, IO pins can be reconfigured for driver strengths and other parameters. Thus, we implement tuning on FPGAs as follows.

For each register of choice, we additionally connect its output with two IO pins, again w/o.l.o.g. one with lowest and one with highest available IO driver strengths, respectively. Similar to the ASIC implementation, we use additional MUXes to randomly select only one IO pin to be driven at a time.

For static tuning scenarios, we simplify the above implementation by additionally connecting and hard-wiring each register of choice to only one IO pin of lowest/highest IO driver strength.

For VCC tuning, we assume some tuning features are available, like FPGA on-board voltage regulators.

4.2 CAD Flow for Design-Time Evaluation of ASIC Power Profiles

The CAD flow described here serves to investigate the role that joint tuning of driver strengths and VCCs plays against PSC attacks early on, i.e., in a design-time simulation environment. Note that the idea of such CAD-flow-based investigation is not new; similar approaches have been taken in, e.g., [16, 19]. Still, the flow described here has been devised independently of prior art; it is also verified thoroughly within other studies of ours [9, 10].

Our flow (Fig. 3) takes as inputs: (i) the register-transfer level (RTL) code of the design to be evaluated, e.g., a regular AES crypto core, (ii) the standard-cell library of choice, and (iii) sets of plain-texts and keys. The latter can also be randomly generated within the flow itself. The flow provides the zero-delay power values, i.e. power values without any impact of layout effects or noises, for the design’s circuit-level computation as triggered by the plain-text and key inputs. These power values are then utilized for PSC evaluation/security analysis (Sec. 4.3).

²In contrast, we study both static and dynamic tuning, for ASIC as well as FPGA fabrics. We find that static tuning has limited effects; this is in agreement with findings in “Karna.” We also find that static tuning is even counteractive for FPGA implementation, whereas “Karna” did only study ASIC implementation.

³For actual ASIC implementations, we assume IVRs or other tuning features to be available. Note that requirements for such would be reasonable; dynamic VCC tuning is required at most once per full AES round, not every clock cycle. This is because the CPA attack focuses on the last (or first) intermediate round [3].

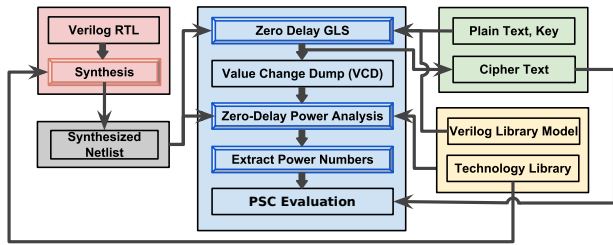


Figure 3: CAD flow for design-time evaluation of zero-delay power profiles of ASICs.

Next, we describe the flow in some more detail. For the implementation, we employ regular commercial tools (Sec. 5.1). We release source codes for our CAD flow in [13].

Step 1: We synthesize the AES core’s RTL. We verify the functionality of the obtained gate-level netlist using a Verilog testbench, with randomized sets of plain-texts and keys. We also confirm the functionality of the design, using software simulation of the crypto operations and cross-checking of the two sets of cipher-texts.

Step 2: We perform zero-delay gate-level simulation of the design, to generate a value change dump (VCD) file. Note that VCD files are well-established for simulation purposes.

Step 3: The VCD file is then used for power simulation of the synthesized gate-level netlist. To limit simulation efforts—without comprising the accuracy for the PSC attack evaluation—we focus only on the relevant time intervals, i.e., the last (or first round) of AES, which are the ones sufficient to attack [3].

Scope of Simulations: Instead of performing full-scale transient simulations, which would also capture noises induced by glitching activities, here we leverage noise-free, zero-delay simulations. For our notion of tuning driver strengths and VCCs, glitches are less relevant; tuning has significant impact on power profiles overall (recall Fig. 1), not only on glitching activities.

For such zero-delay simulation, all power-consuming transitions occur simultaneously for the clock edge. Thus, peak-power values, which are of particular relevance for PSC attacks, can be easily extracted. Further, note that register are generally contributing the largest shares of dynamic power consumption. While the registers holding the secret key itself are not switching, thus not providing any leverage for PSC attacks, other registers do switch. In fact, those register that are holding the texts of intermediate AES rounds incur considerable switching activities by design, due to the confusion and diffusion properties of the AES crypto algorithm, and can thus be well correlated against.

4.3 CPA Framework for Security Analysis

The CPA framework described here serves for an empirical security analysis, yet in a thorough manner and backed by solid analytical formalism. We release source codes in [13].

As indicated, CPA is known to be effective [1, 3, 5]. At the heart of CPA is the linear Pearson correlation coefficient (PCC), used to quantify the relationship between actual power profiles and hypothetical power profiles. The latter are typically built up by enumeration of all byte-wise possible keys [3]. After building up correlation over a number of traces—obtained in any way, e.g., via design-time power simulations using the above CAD flow or via

measurements—the most promising candidates for all bytes are concatenated to form the guess of the correct key.

We take the following steps in our framework.

Step 1: Note that, since registers consume a significant share of dynamic power during signal transitions, the Hamming distance (HD) for the registers’ data before and after switching operations is established as simple, yet effective, *HD power model* [3].

Now, as indicated, sets of hypothetical power values are to be derived for all possible key values. This is done using the HD power model, namely by reverting the AES last-round operation using the observed cipher-texts, and computing and memorizing the HD when considering all possible key values for that reverse operation.

Step 2: Using the PCC formalism, the actual power traces—again, can obtained in any way—are correlated against all hypothetical power profiles. The profile resulting in the highest PCC value across a number of traces is assumed to represent the correct key. As indicated, the correlation analysis can be conducted at the byte level (instead of bit level) [3], which is essential to manage complexity for exploring the search space of all possible keys.

Instead of considering all available traces at once for this correlation analysis, we thoroughly and step-wise explore the range of how many traces are needed at least until disclosure of the correct key with certain confidence. See Sec. 5.1 for more details.

Attack Versus Security Analysis: Acting as designers, we can readily verify the key guess for any CPA run during the security analysis. An attacker, however, has to monitor the progression of PCC values for all the possible key hypotheses throughout a more or less large number of traces; only once the best candidate shows a significant PCC outlier among all other candidates, can the attacker assume to have successfully inferred the correct key.

We take the attacker’s approach for parts of our study as well, namely for realistic pre-processing (i.e., without relying on the actual correct key) of noisy power traces obtained for FPGA measurements. There, any sub-set of traces that does not exhibit a sufficiently significant PCC outlier is rejected as too noisy.

5 EMPIRICAL STUDY: SETUP

5.1 Experimental Setup

Tools: We devise the CAD flow and perform ASIC implementation using standard commercial tools, i.e., Synopsys DC for logic synthesis and Synopsys VCS for gate-level power simulation. We devise custom tcl scripts for the CAD flow integration and bash scripts for data management and processing. We use Xilinx ISE Webpack suite for FPGA implementation. We implement the CPA framework in C++, based on the release in [4].

Design: We utilize a regular AES core, with 128-bit keys and 128-bit texts processed in electronic code book (ECB) mode. We release the RTL in [13].

Implementations: For the ASIC implementation, we employ a commercial 55nm technology by GlobalFoundries, for logic synthesis and zero-delay, gate-level power simulation. For the FPGA implementation, we use a Sakura-X board [11], specifically its Kintex-7 FPGA chip, which is manufactured in a 28nm technology. We set up up a typical FPGA measurement station (Fig. 4), also following the board’s manual [11] for probe connections. We tune VCCs using the on-board core-voltage regulator.

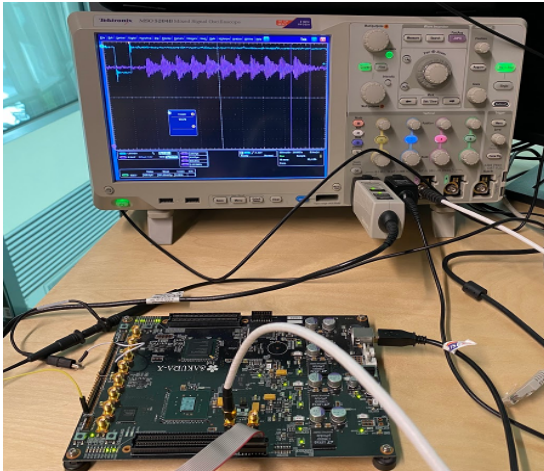


Figure 4: FPGA measurement setup.

Naturally, the ASIC and FPGA implementations differ considerably in terms of (i) available driver strengths and VCCs, (ii) technology nodes and hardware fabrics, and (iii) noise profiles. Such diversity is essential to confirm and generalize our findings.

Metrics and Workflow for Security Analysis: We report the minimal number of traces needed to disclosure as $\#TTD(c\%, t)$, i.e., for a confidence value c across t randomized CPA trials.

Throughout all experiments, we report $\#TTD(90\%, 1k)$ which means that ≥ 900 out of 1,000 randomized CPA trials succeed for the reported number of traces. To determine $\#TTD(90\%, 1k)$ values accurately, we conduct multiple CPA campaigns as follows. Each campaign is run independently in steps, where an increasing number of randomly selected plain-texts and corresponding power traces are made available to the CPA framework. More specifically, for each campaign step, 1,000 randomized CPA trials are conducted on 1,000 different sets of randomly selected texts and corresponding traces. The success rate is tracked and more and more steps are taken, until the point of 90% confidence is reached, i.e., 900/1,000 trials succeed. While such workflow is computationally intensive, it is trivial to parallelize, and essential for a robust security analysis.

For the exploration of different tuning scenarios, we repeatedly conduct CPA campaigns with many trials, as outlined above, all while maintaining the overall sets/pool of plain-texts and keys. Doing so is important for fair comparison across tuning scenarios.

We consider sets of 5k traces for the ASIC implementation and 15k–170k traces for the FPGA implementation.⁴ For each step in any CPA campaign, we increase the number of available traces by 5 and by 15, respectively, for the ASIC and the FPGA implementation.

Metrics and Workflow for Layout Analysis: We report power, performance, and area (PPA) numbers for ASIC and FPGA implementations. For ASIC implementation, performance and area is reported from logic synthesis using DC. Power is reported as average peak power, derived from the same gate-level simulations used for security analysis. For FPGA implementation, performance and

⁴For the FPGA implementation, we observe that 15k traces are sufficient for breaking less resilient scenarios, whereas around 200k traces are still insufficient for breaking the more resilient scenarios. As indicated, we pre-process measurement traces, similar to what an attacker would do, to reject noisy traces. After measuring 200k traces, we split them into 20 by 10k sets, and had to reject three sets; thus, 170k traces remain.

area—the latter in terms of utilization of flip-flops (FFs) and look-up tables (LUTs)—are reported from ISE runs. Power is reported as average peak power from measurements. We also report additional IO pins used for implementing tuning in FPGA.

5.2 Tuning Settings

We consider the following tuning settings for our study. Each setting comprises different scenarios, in terms of static versus dynamic tuning and in terms of driver strengths, VCCs available for tuning in the ASIC versus FPGA implementation.

- (I) All FFs are tuned to the same driver strength and VCC.
 - (Ia) Static tuning only.
 - (Ib) Static and dynamic tuning, covering all combinations of static/dynamic tuning for driver strengths and VCCs.
 - (Ic) Dynamic tuning only.
- (II) FFs holding AES texts versus all other FFs are separated into two groups. Groups of FFs are tuned differently, whereas all FFs within a group are tuned the same. This setting is motivated by the potential need for a more limited and less costly implementation; see also Sec. 7.
 - (IIa) Static tuning only.
 - (IIb) Dynamic tuning of FFs holding AES texts; static tuning of all other FFs.

Note that, for Setting (II), we refrain from considering further possible scenarios, like dynamic tuning of FFs holding AES texts along with different dynamic tuning of all other FFs. This is w/o.l.o.g., due to practical limitations on the number of available IO pins for dynamic tuning on our FPGA of choice.

6 EMPIRICAL STUDY: SECURITY ANALYSIS

6.1 ASIC Implementation

Detailed results are provided in Fig. 5; related observations are presented next. Note that the numbering of scenarios below matches that in Fig. 5. Also note that, in Sec. 6.3, we streamline and summarize findings for both ASIC and FPGA implementations.

- (1) *Untuned Baseline:* The regular AES design, without any tuning. VCC is set to 1.08V for all FFs and all other gates. Driver strengths are set automatically by logic synthesis. Here, 100 CPA campaigns are conducted, resulting in $N = 100$ data points for the $\#TTD(90\%, 1k)$ metric (Sec. 5.1), but recall that many more CPA trials are underlying for a robust analysis.⁵

Tuning Setting (I): For static or dynamic tuning of all FFs, we consider the following scenarios.

- (2) *Static X, VCC:* All combinations for all five available driver strengths, ranging from X0.5 to X4, as well as three available VCCs, ranging from 0.9V to 1.08V, are considered, resulting in 15 tuning configurations and, across three CPA campaigns, in $N = 45$ data points.

⁵As indicated, each campaign progresses in steps of more traces becoming available (w/o.l.o.g., 5 traces for the ASIC implementation), and for each step 1,000 trials are run. To avoid running many trials with too few traces to begin with, we initially conduct some exploratory sampling, to determine a reasonable starting point for all campaigns; we found 600 traces suitable for this scenario. Thus, there are 100 campaigns run, with 16–25 steps per campaign (covering the observed min and max points of 680 and 725 for $\#TTD(90\%, 1k)$, respectively), with 1,000 trials per step, resulting in 1.6–2.5 million CPA trials in total, just for exploring this tuning scenario. All other scenarios are explored in the same thorough manner.

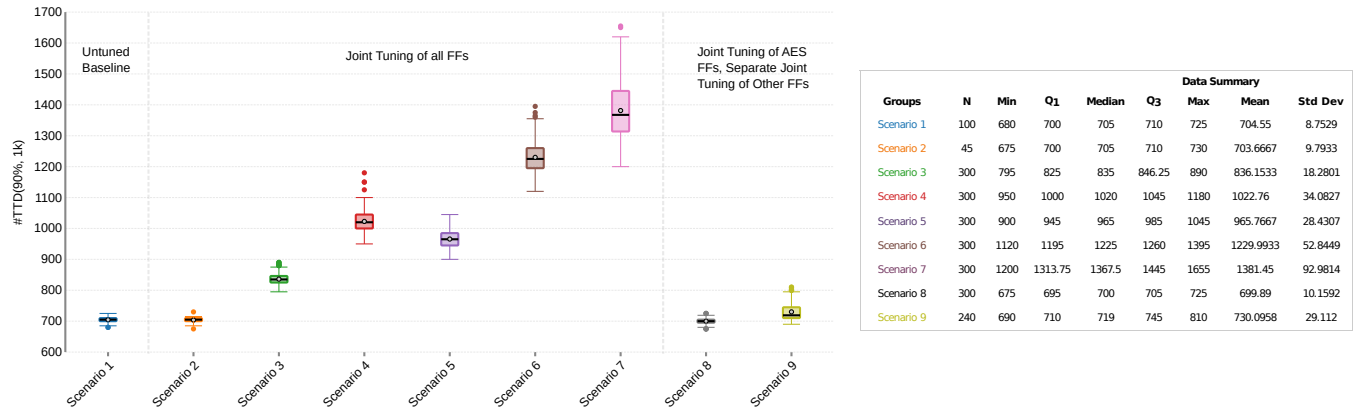


Figure 5: CPA results for the ASIC implementation. See the main text for description of the different scenarios. Also recall that, for each data point underlying each box, there is a robust and thorough sampling process underlying (Sec. 6.1; Footnote 5).

This is the least resilient scenario across Setting (I), with little difference to the untuned baseline. Along with low standard deviation (SD) across all 45 combinations, this indicates that exclusively static tuning is not effective.

- (3) *Static X0.5, Dynamic VCC*: Here, 100 runs for randomized, dynamic VCC tuning across 0.9–1.08V, are considered in three CPA campaigns, resulting in $N = 300$ data points. This scenario is more resilient than static tuning (2), but less resilient than dynamic VCC tuning for higher driver strengths (4), and also less resilient than driver-strength tuning for static VCCs (5), (6). This indicates that dynamic tuning can be beneficial, when applied thoughtfully.
- (4) *Static X4, Dynamic VCC*: Same setup as in (3), except driver strengths are set to X4 for all FFs. As indicated, this scenario is more resilient than VCC tuning for lower driver strength (3). It is also somewhat more resilient than driver-strength tuning for low, static VCC (5). These observations, together with those for (2), imply that high driver strengths can be beneficial and dynamic VCC tuning can be beneficial.
- (5) *Dynamic X, Static 0.9V*: Here, 100 runs for randomized, dynamic driver-strength tuning across X0.5–X4, are considered in three CPA campaigns, resulting in $N = 300$ data points. As indicated, this scenario is on average more resilient than VCC tuning for low driver strength (3), but somewhat less resilient than VCC tuning for high driver strength (4).
- (6) *Dynamic X, Static 1.08V*: Same setup as in (5), except VCCs are set to 1.08V for all FFs. On average, this scenario is more resilient than all prior ones. Considered along with (5), this implies that, for dynamic driver-strength tuning, high VCCs can be beneficial.
- (7) *Dynamic X, Dynamic VCC*: Here, 100 runs for randomized, dynamic driver-strength tuning across X0.5–X4 and dynamic VCC tuning across 0.9–1.08V, are considered in three CPA campaigns, resulting in $N = 300$ data points.

This is the most resilient scenario. This implies that dynamic tuning of both driver strengths and VCCs provides superior resilience, namely on average 196% and up to 235% as resilient as both static tuning and the untuned baseline.

For *Tuning Setting (II)*, separate tuning of FFs holding AES texts versus all other FFs, we consider the following scenarios.

- (8) *Static Only*: For each of the two groups, all combinations of five driver strengths, ranging from X0.5 to X4, as well as two VCCs, 0.9V and 1.08V, are considered, resulting in 100 configurations, $N = 300$ data points for three CPA campaigns. Here, we observe a similarly low resilience as with static-tuning Scenario (2), again with low SD across all different configurations. This re-iterates that static tuning alone is not effective, not even in any particular tuning configuration.
- (9) *Static and Dynamic*: All combinations of two corner-case driver strengths, X0.5 and X4, and VCCs, 0.9V and 1.08V, are considered for static tuning of other FFs. At the same time, all six possible, non-redundant combinations for dynamic tuning using different configurations for driver strengths and VCCs are considered for FFs holding AES texts. In other words, this scenario explores dynamic tuning of FFs holding AES texts, while statically tuning all other FFs. All combinations are explored via ten CPA campaigns, resulting in $N = 4 * 6 * 10 = 240$ data points. Also here, we observe a low resilience, similar to (2) and (8), albeit with a higher SD, implying that some particular configurations are more promising. Still, limiting dynamic tuning to only the FFs holding AES texts is not effective.⁶

6.2 FPGA Implementation

Next, we elaborate on our findings for the FPGA implementation. In Sec. 6.3, we streamline and summarize all findings.

Given that available driver strengths and VCCs, as well as noise profiles, differ vastly from those of the ASIC implementation, quantitative results cannot be compared across these implementations.

⁶While this applies for the ASIC implementation, we observe that, for the FPGA implementation, such limited tuning can still be effective.

More importantly, however, observations are verified across hardware fabrics and even technology nodes, rendering our insights on the prospects of tuning robust.

Detailed results are provided in Fig. 6; related observations are discussed next. The scenario numbering matches that in Fig. 6.

- (1) *Untuned Baseline, 0.955V*: The regular AES design, without any tuning. VCC is set to 0.955V for all FFs.
- (2) *Untuned Baseline, 1.055V*: The regular AES design, without any tuning. VCC is set to 1.055V for all FFs. This scenario is less resilient than (1), suggesting that lower VCCs *can* be beneficial, especially as long as driver strengths are not tuned dynamically; see also the remaining scenarios.

Recall that we use additional IO pins for driver-strength tuning in the FPGA implementation (Sec. 4.1). Since IO pins are limited, we also want/need to limit the number of FFs that are tuned. Thus, counterparts for promising configurations observed for the ASIC implementation, namely Setting (I) in general and the most resilient Scenario (7) in particular—dynamic tuning of both driver strengths and VCCs for all FFs—are impractical for the FPGA implementation.

Accordingly, we skip directly to *Tuning Setting (II)*, separate tuning of FFs holding AES texts versus all other FFs. Again considering limited numbers of IO pins, we do not specifically tune other FFs here, but only FFs holding AES texts. We consider the following resulting scenarios. 30 CPA campaigns are conducted (i.e., $N = 30$ data points) for each scenario unless stated otherwise.

- (3) *Static X4, 0.955V*: This scenario is only slightly more resilient than the untuned baseline for the same VCC, indicating that static tuning with low driver strength is not effective.
- (4) *Static X4, 1.055V*: Here, there is a significant *drop* in resilience. Considering together with (3) and the remaining scenarios for static tuning, i.e., (5) and (6), this indicates that static tuning is most often counterproductive, due to increased information leakage incurred via toggling IO pins according to AES texts held in the related FFs.
- (5) *Static X16, 0.955V*
- (6) *Static X16, 1.055V*
- (7) *Dynamic X, Static 0.955V*: This scenario represents a strong turning point. On average, when compared to the corresponding untuned and statically-tuned baselines, resilience is increased to 199% and 197–297%, respectively. This indicates that dynamic driver-strength tuning is effective. Unlike with static tuning, where any related changes in power profiles can still be well correlated against, such dynamic tuning significantly interrupts the correlation working principle, by interspersing power profiles *in a randomized manner* such that different texts may well be related to the same power values and vice versa, as motivated in Sec. 1.
- (8) *Dynamic X, Static 1.055V*: This scenario represents another turning point, as in high a VCC notably improving resilience again, unlike for the untuned baselines or static-tuning scenarios. This implies that high VCCs can be beneficial in combination with dynamic driver-strength tuning.
- (9) *Dynamic X, Dynamic VCC*: This is the most resilient scenario by far. Here, we consider even 100 CPA campaigns for robust sampling, and find that none can break the tuning-induced resilience, even when considering all 170k available traces

Table 1: Layout Analysis for ASIC Implementations

Design	Avg. Peak Power [mW] 0.9V / 1.08V	Critical-Path Delay [ns] 0.9V / 1.08V	Std.-Cell Area [μm^2] 0.9V / 1.08V
Baseline	2.709 / 3.100	9.64 / 9.79	54,928 / 43,639
All FFs Tunable	3.134 / 3.764 (+15.69% / +21.42%)	14.13 / 11.86 (+46.68% / +21.14%)	67,873 / 57,300 (+23.57% / +31.30%)
AES-Text FFs Tunable	2.779 / 3.237 (+02.58% / +04.42%)	14.13 / 11.68 (+46.68% / +19.31%)	57,272 / 46,324 (+04.27% / +06.15%)

Table 2: Layout Analysis for FPGA Implementations

Design	Avg. Peak Power [mW] 0.9V / 1.08V	Critical-Path Delay [ns]	FFs / LUTs Util. [# / #]
Baseline	0.969357 / 1.07049	9.052	952 / 3,137
Static X4	0.972771 / 1.07352 (+00.35% / +00.28%)	10.352 (+14.36%)	965 / 3,118 (+01.37% / -00.61%)
Static X16	0.971117 / 1.07347 (+00.18% / +00.27%)	10.352 (+14.36%)	965 / 3,118 (+01.37% / -00.61%)
Dynamic	0.973676 / 1.07214 (+00.45% / +00.15%)	9.994 (+10.41%)	1,028 / 3,183 (+07.98% / +01.47%)

at once.⁷ This implies that resilience is increased by *at least* 11.8x over the untuned baseline (1). This clearly shows that joint dynamic tuning is by far most resilient.

6.3 Summary

Our findings for both the ASIC and FPGA implementations are:

- (1) Dynamic VCC tuning is promising, but limited on its own;
- (2) Dynamic driver-strength tuning, along with high VCCs or dynamic VCC tuning, is most effective;
- (3) Tuning of all FFs is promising, but is also limited in practice (by available IO pins for the FPGA implementation and by overheads for the ASIC implementation; see Table 1 below);
- (4) Static tuning is least effective in general and even counterproductive for the FPGA implementation (where implicit masking by environmental noises can be nullified when using high VCCs and/or high driver strengths for tuning).

7 EMPIRICAL STUDY: LAYOUT ANALYSIS

ASIC Implementation: See Table 1. Naturally, layout costs are larger when all FFs are tunable, whereas costs are reasonable if only FFs holding AES texts are tunable.

We argue that costs may well be amortized for large-scale ASIC designs with many modules. In contrast, to study upper limits of overheads, here we consider a stand-alone AES core. Besides, some optimized cell-level integration of different driver strengths and tuning peripherals may be attainable in future work.

FPGA Implementation: See Table 2. Note that, for both static-tuning designs, critical-path delays and utilization are the same; this is because only the driver-strength configurations for the additional IO pins differs here, whereas the core circuitry remains the same.

⁷Accordingly, there are no corresponding #TTD(90%, 1k) data points included in Fig. 6.

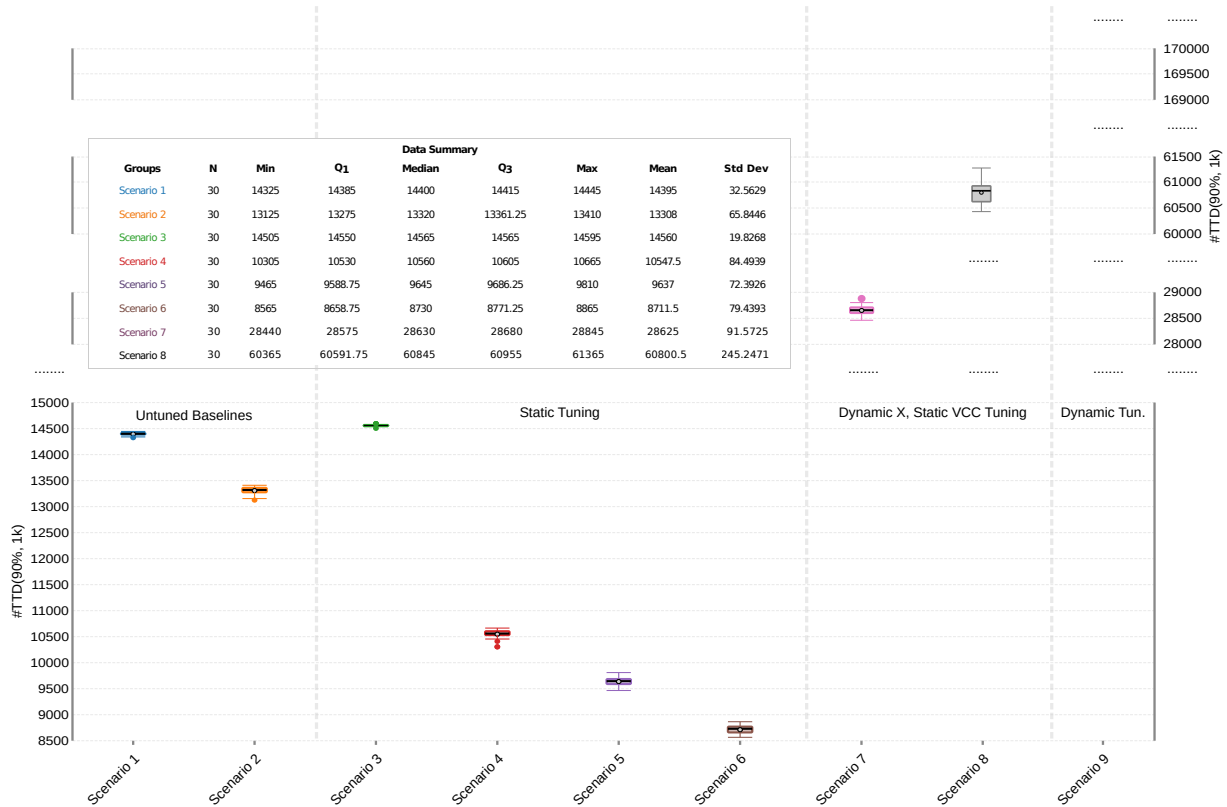


Figure 6: CPA results for the FPGA implementation. See the main text for description of the different scenarios. Note the varying ranges for #TTD(90%, 1k) across the different tuning scenarios. Also recall that, for each data point underlying each box, there is a robust and thorough sampling process underlying (Sec. 6.1; Footnote 5).

Overall, we observe marginal impact on power as well as utilization, along with some overheads for delays.

Delay overheads are due to large-scale changes imposed on placement and routing, after connecting the circuitry to the additional IO pins used for tuning, as we have observed via ISE PlanAhead. An iterative design strategy might reduce overheads;⁸ currently, we assign from available IO pins arbitrarily to FFs to be tuned.

8 DESIGN GUIDELINES FOR TUNING

Recall the key findings for the security analysis, summarized in Sec. 6.3. Considering these together with the layout analysis in Sec. 7, we propose the following design guidelines.

Static tuning is discouraged. Joint dynamic tuning should be applied whenever possible; else, dynamic tuning of driver strengths is preferred as simple, yet effective, alternative over VCC tuning.⁹ Tuning of all FFs can be considered (i) for ASIC implementation once the relatively high layout overheads become acceptable, which would be true for larger system-on-chip ASICs where crypto cores form only a small part, and (ii) for FPGA implementation as long

⁸For example, the strategy could be (i) placement and routing, (ii) selection of nearby IO pins for assignment to tuned FFs, (iii) evaluation of layout overheads, and (iv) repeated selection/assignment of IO pins, guided by worst-case timing overheads, etc.

⁹This is because (i) VCC tuning requires some IVR or other tuning features, whereas driver-strength tuning can be implemented at circuit level at its own, and (ii) dynamic driver-strength tuning is more resilient.

as sufficient IO pins are available. Otherwise, tuning only the FFs that are holding AES texts is still more promising than untuned baselines, especially in the field where noise is coming into play as well (as demonstrated through the FPGA results).

9 CONCLUSIONS AND FUTURE WORK

In this paper, we have explored joint tuning of driver strengths and VCCs as countermeasure against PSC attacks. Toward this end, we have proposed a simple implementation scheme, devised a CAD flow for design-time exploration of ASICs, devised a CPA framework for thorough and robust security analysis, and conducted a comprehensive experimental study considering both ASIC and FPGA fabrics under various tuning scenarios. We find that dynamic tuning is particularly effective, increasing resilience considerable for ASIC and FPGA fabrics along with acceptable overheads.

For future work, we plan to study joint tuning in more detail as follows. First, we shall explore more efficient means for tuning, e.g., circuit-level primitives for ASIC implementations and/or an iterative strategy for IO-pin assignment for FPGA implementations. Second, we shall study tuning also in the context of leakage-power attacks, given that driver strengths and VCCs do impact leakage-power profiles as well. Third, besides using a CPA attack, we shall also utilize generic approaches for security assessment, e.g., TVLA, to more rigorously study possible limitations for tuning.

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